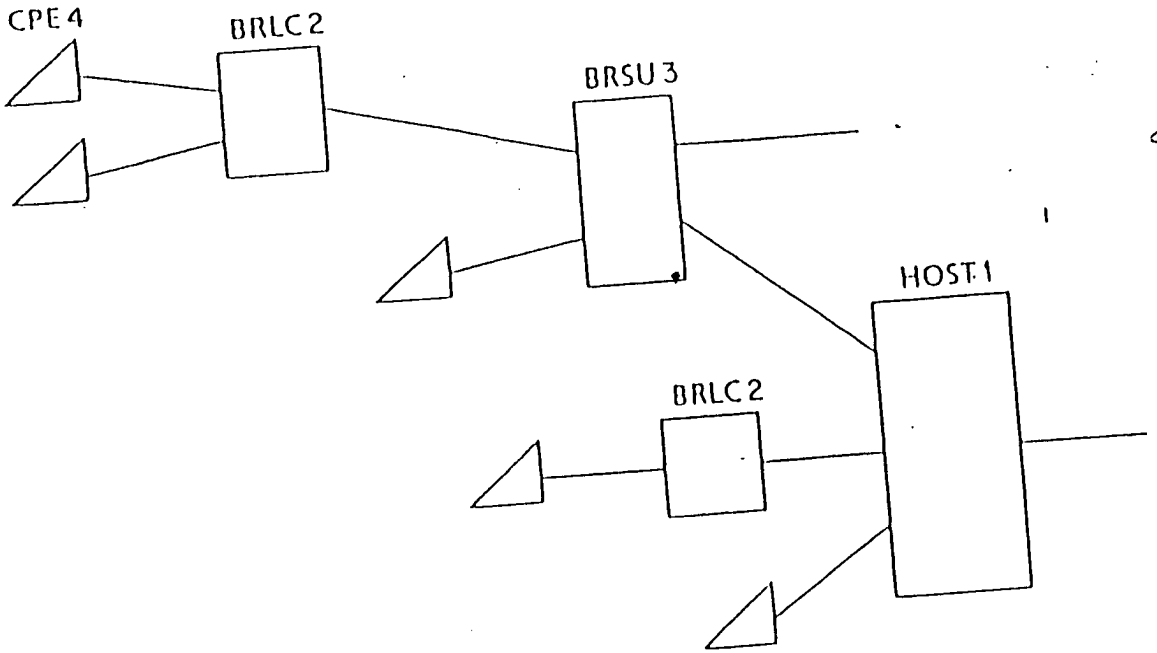
APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

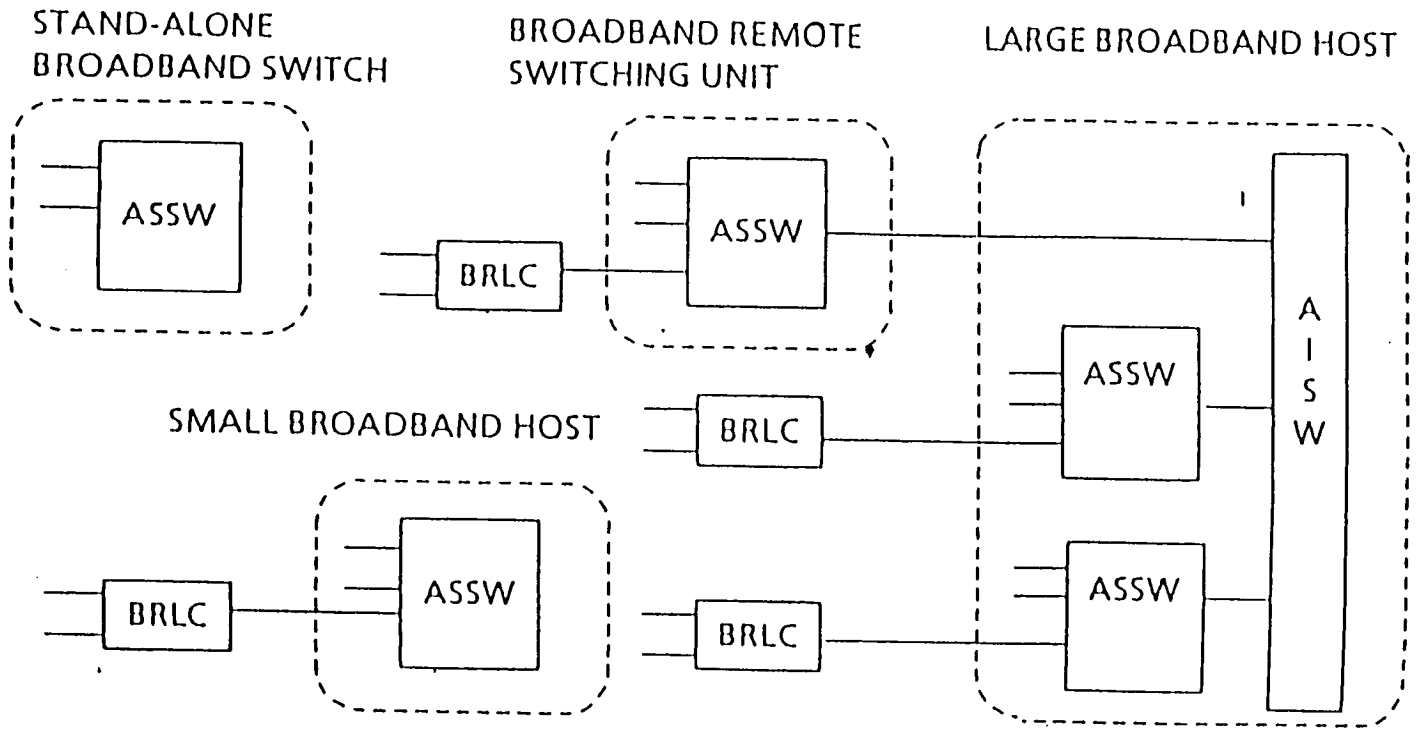


BRLC : Broadband Remote Line Concentrator
BRSU : Broadband Remote Switching Unit
CPE : Customer Premises Equipment
HOST : Broadband Host Switch

FIG. 1

6695E0* ET27260

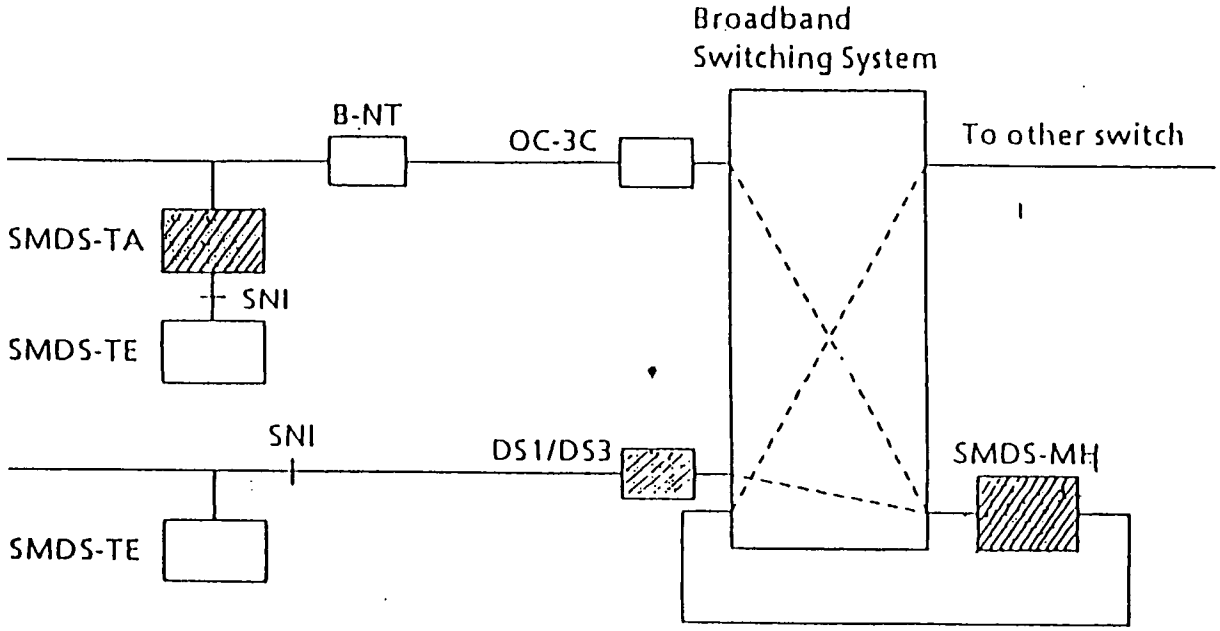
APPROVED
BY
DRAFTSMAN
CLASS
SUBCLASS
U.S. PKG.



ASSW ATM Subscriber Switch
AISW ATM Interconnection Switch
BRLC Broadband Remote Line Concentrator

FIG. 2

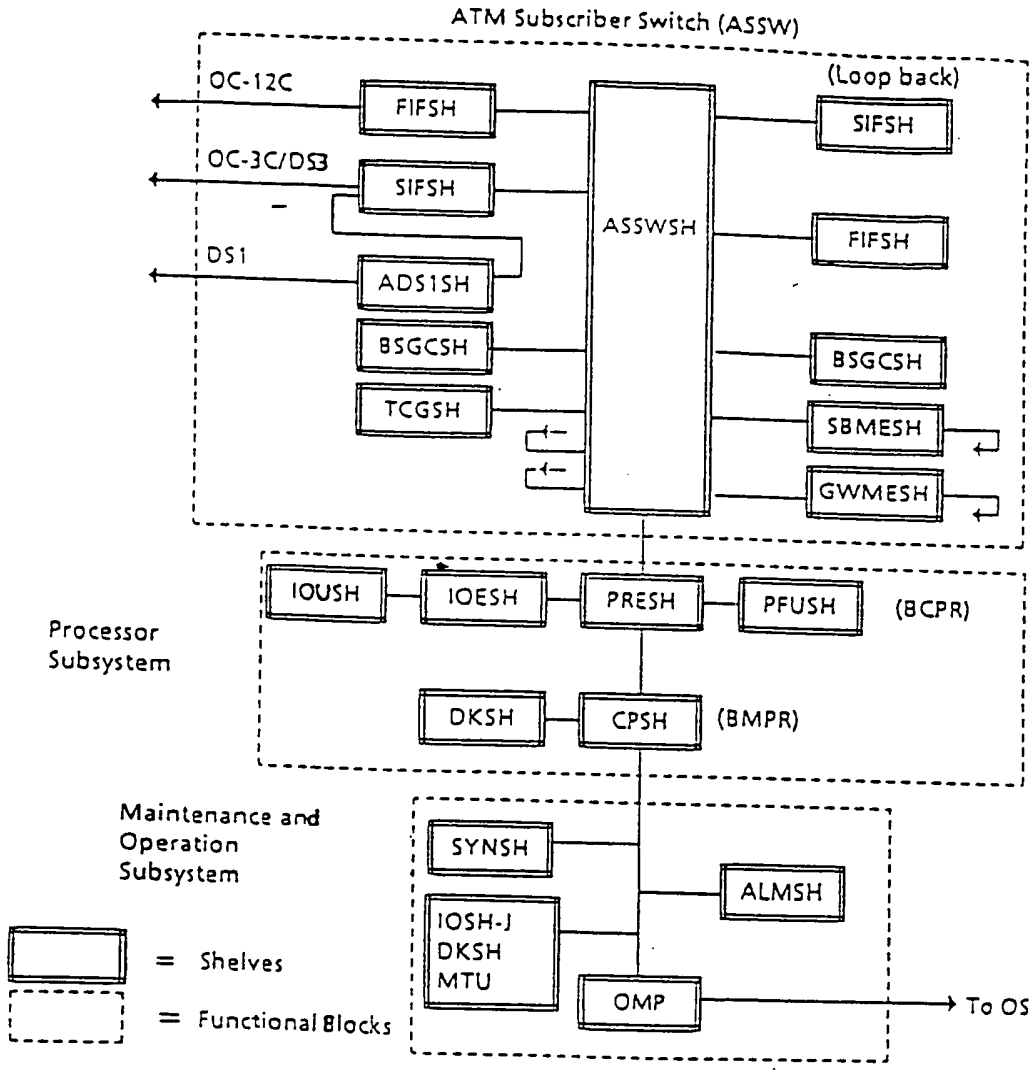
APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



B-NT : Broadband Network Termination
SMDS-MH: SMDS Message Handler
SMDS-TA : SMDS Terminal Adapter
SMDS-TE : SMDS Terminal Equipment

FIG. 3

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



CP: Central Processor
CPR: Call Processor
DK: Disk
FR: Frame Relay

FIG. 4

6698601 "EP2726B

BY
DRAFTSMAN
CLASS
SUBCLASS

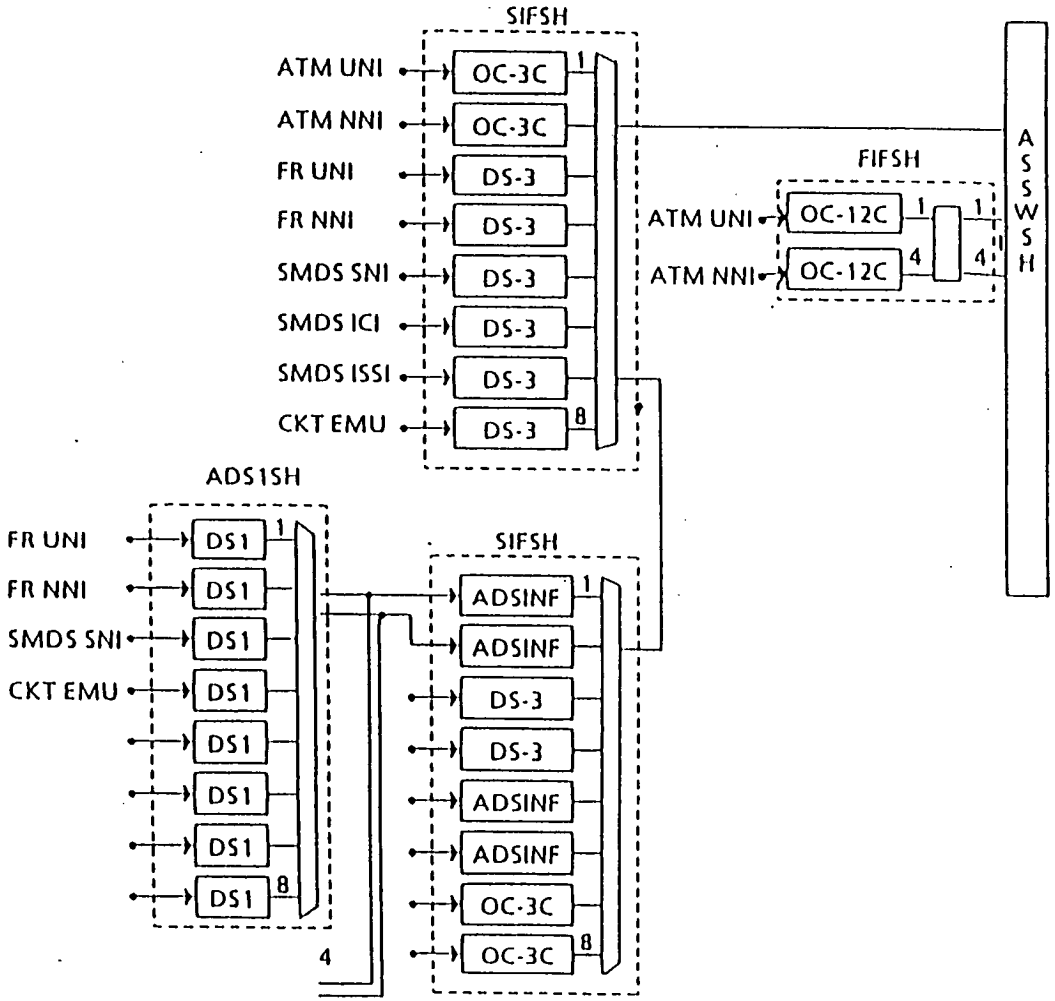
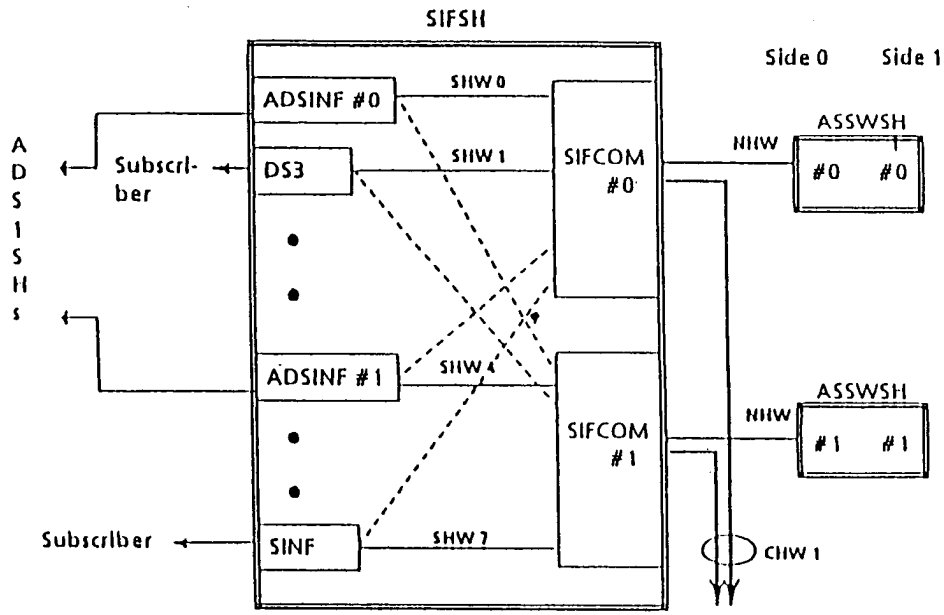


FIG. 5

6653260 "E182260

APPROVED O.G. FIG.
BY
DRAFTSMAN
CLASS
SUBCLASS



ADSINF : ATM DS1 Shelf Interface Card

ASSWSH : ATM Switching Shelf

CHW : Chain Highway

DS3 : Digital Signal Level 3

NHW : Network Highway

SIFCOM : Subscriber Interface Common Card

SINF : Subscriber Interface Card

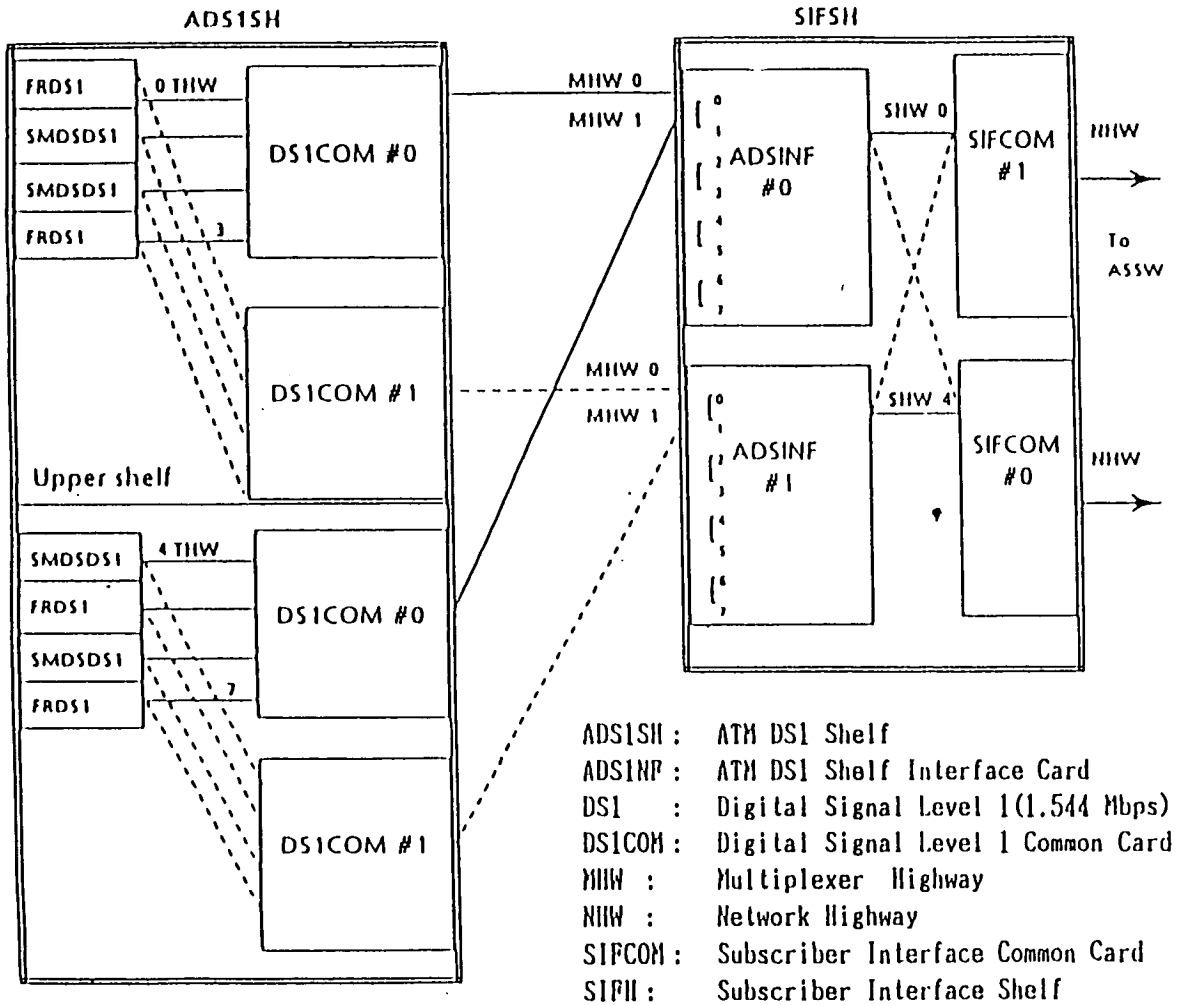
SIFSH : Subscriber Interface Shelf

— — — =Redundant HW

——— =622 Mbps HW

FIG. 6

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



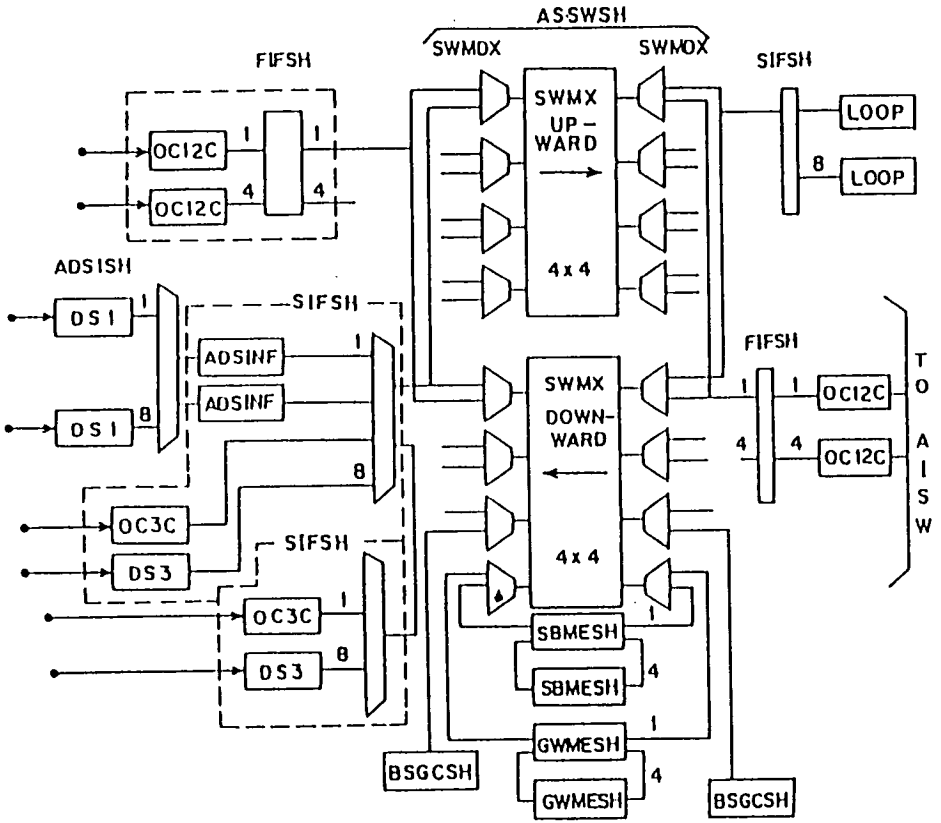
ADS1SH : ATM DS1 Shelf
ADS1NP : ATM DS1 Shelf Interface Card
DS1 : Digital Signal Level 1(1.544 Mbps)
DS1COM : Digital Signal Level 1 Common Card
MIIW : Multiplexer Highway
NIIW : Network Highway
SIFCOM : Subscriber Interface Common Card
SIFH : Subscriber Interface Shelf

——— = 622 Mbps HW

FIG. 7

6692E0 EP1227680

APPROVED BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



FIFSH : Fiber Interface Shelf

ADSISH : ATM DS1 Shelf

SIFSH : Subscriber Interface Shelf

ASSHSH : ATM Switch Shelf

SBMESH : Subscriber Message Handler Shelf

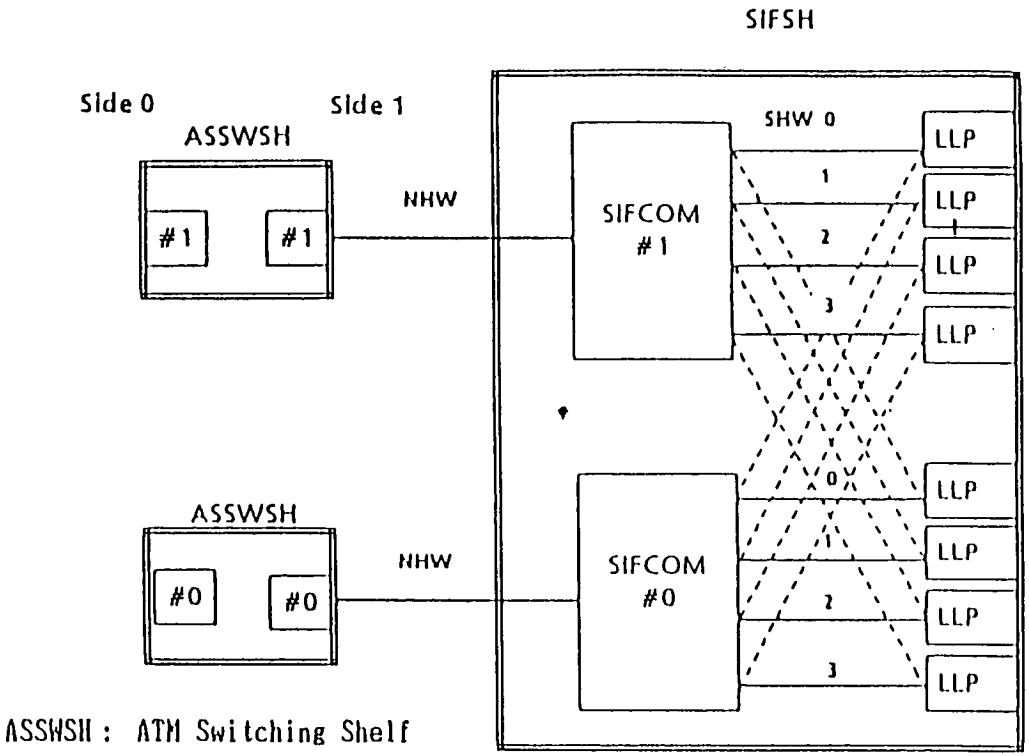
GWMESH : Gateway Message Handler Shelf

BSGCSH : Broadband Signaling Controller Shelf

FIG. 8

669260 EP2260

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



ASSWSH : ATM Switching Shelf

SIFCOM : Subscriber Interface Common Card

LLP : Loopback Card Group

NHW : Network Highway(622 Mbps)

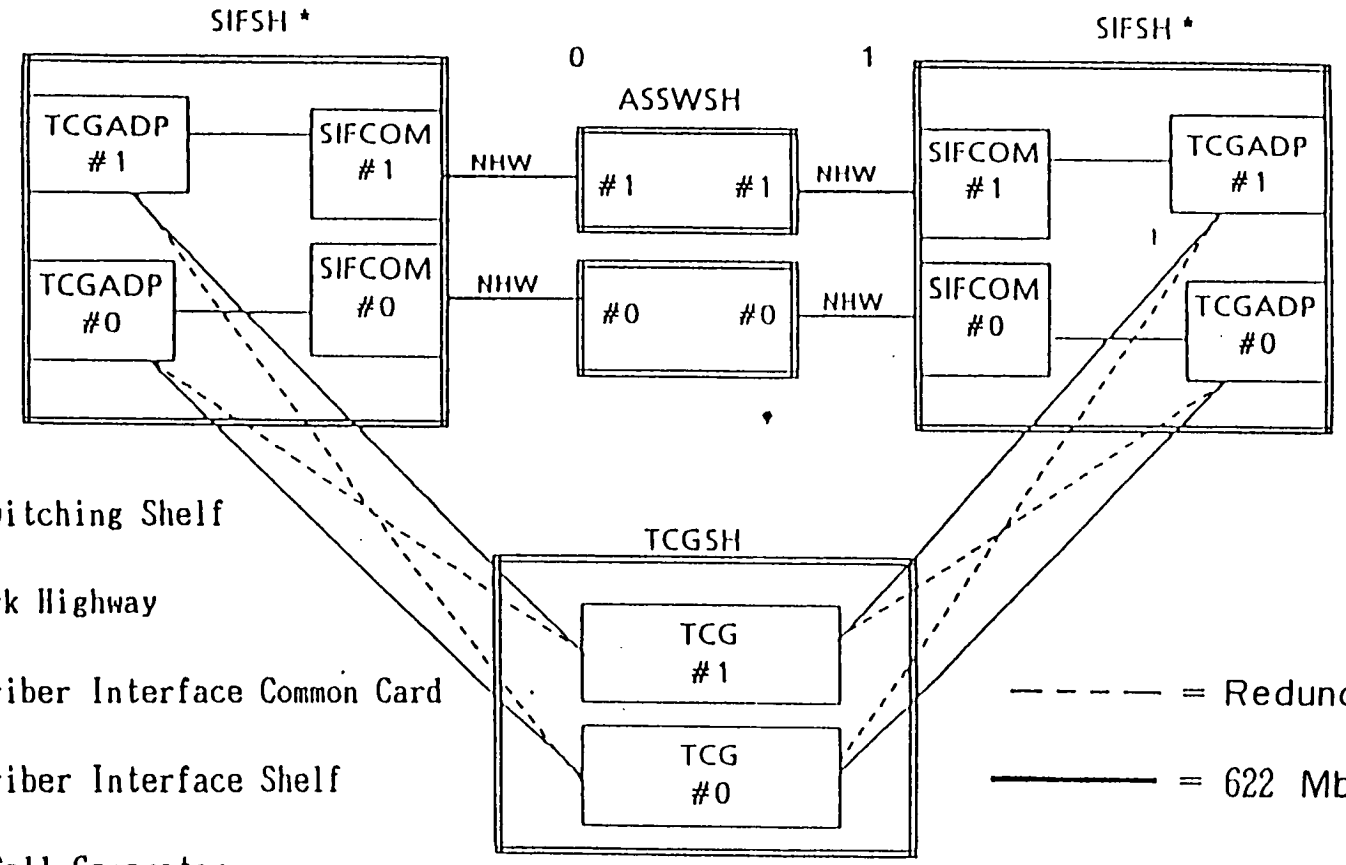
SHW : Subscriber Highway (156 Mbps)

——— = 622 Mbps HW

····· = Redundant HW

FIG. 9

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



ASSWSH : ATM Switching Shelf

NHW : Network Highway

SIFCOM : Subscriber Interface Common Card

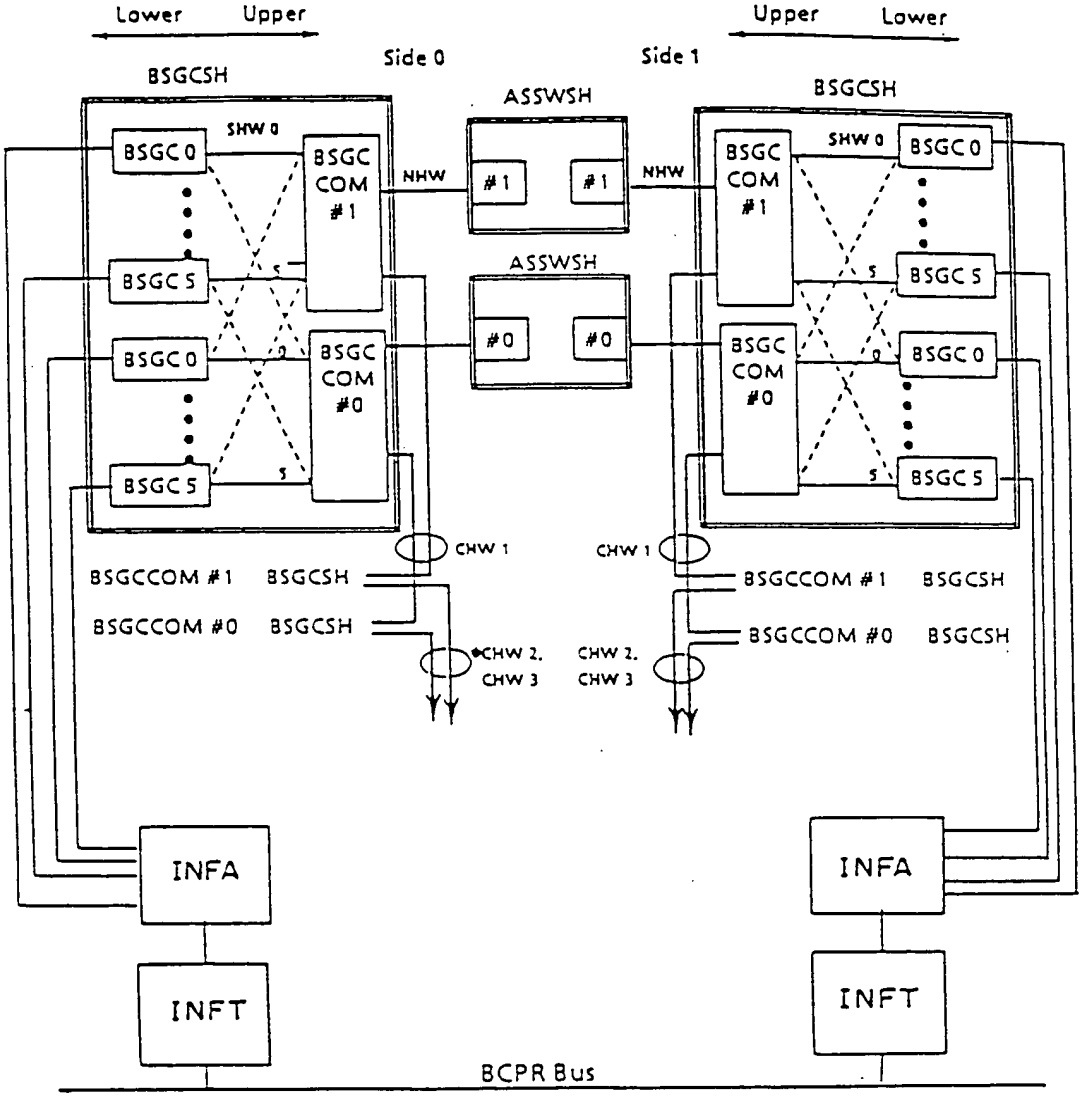
SIFSH : Subscriber Interface Shelf

TCG : Test Cell Generator

TCGADP : Test Cell Generator Adaptor

FIG. 10

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



ASSWSH : ATM
BCPR : Broadband Call Processor
BSGC : Broadband Signaling Controller
BSGCCOM : BSGC Common Card
BSGCSH : BSGC Shelf
CHW : Chain Highway
INFA : Interface Type A
INFT : Interface Type T
SHW : Subscriber Highway

——— = 622

– – – – =

FIG. 11

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

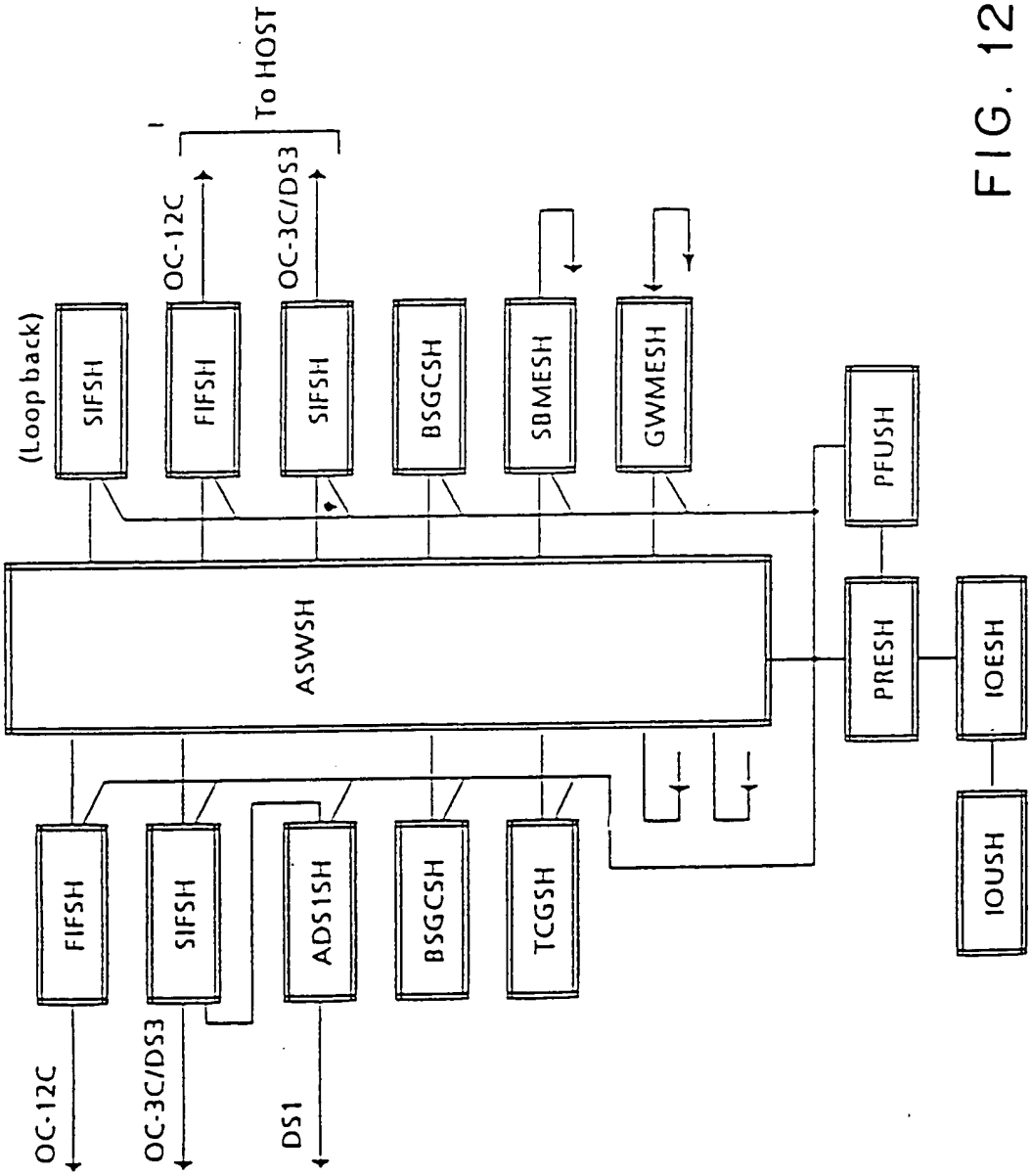


FIG. 12

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

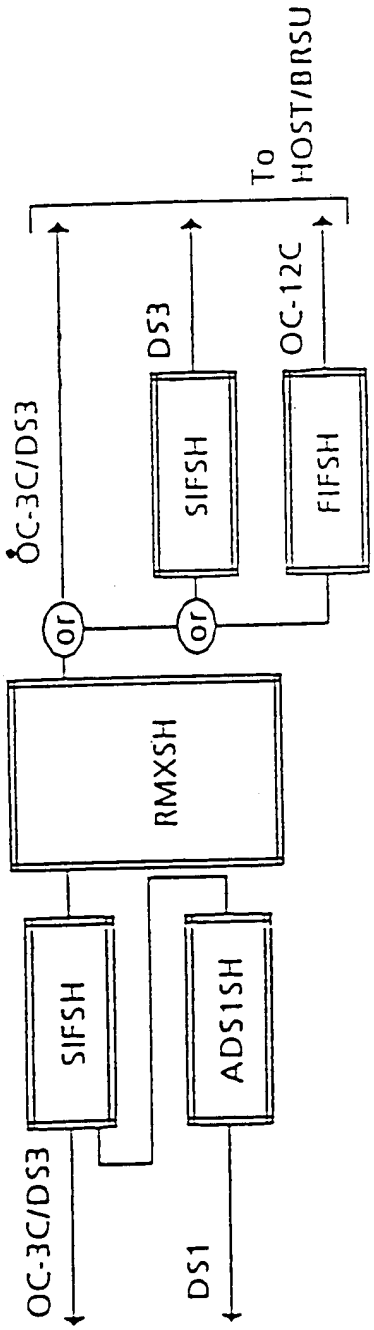
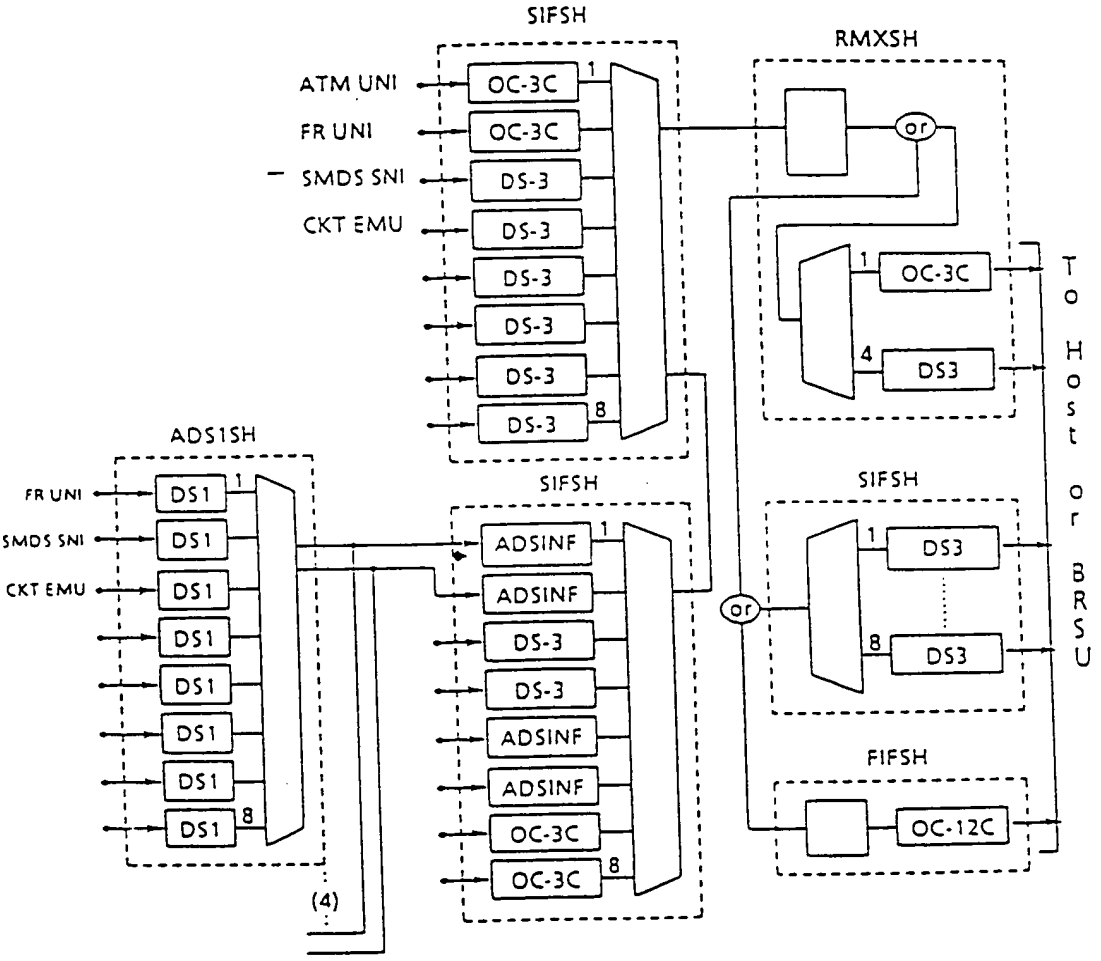


FIG. 13

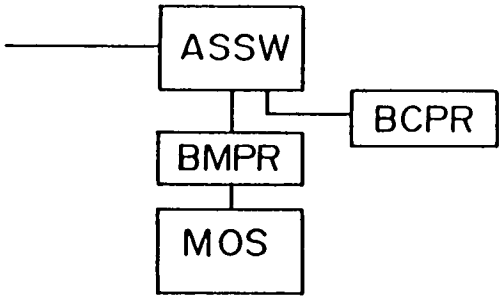
APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



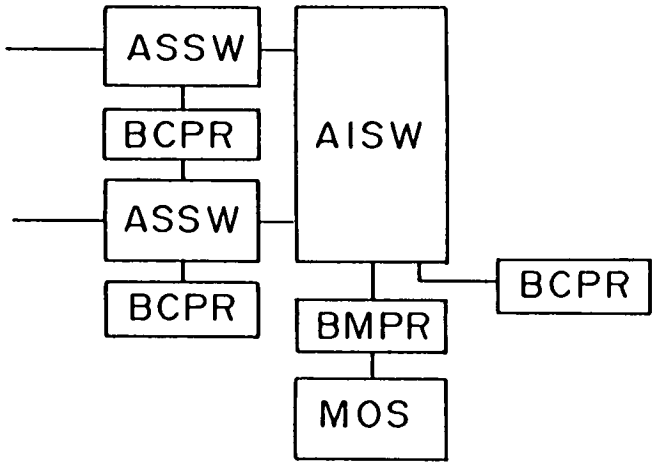
SIFSH Subscriber Interface Shelf
ADS1SH ATM DS1 Shelf
FIFSH Fiber Interface Shelf
RMXSH Remote Multiplex Shelf

FIG. 14

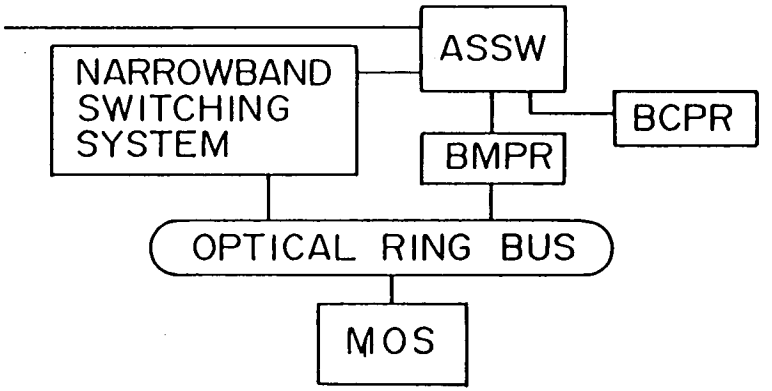
APPROVED BY
DRAFTSMAN
CLASS
O.G.



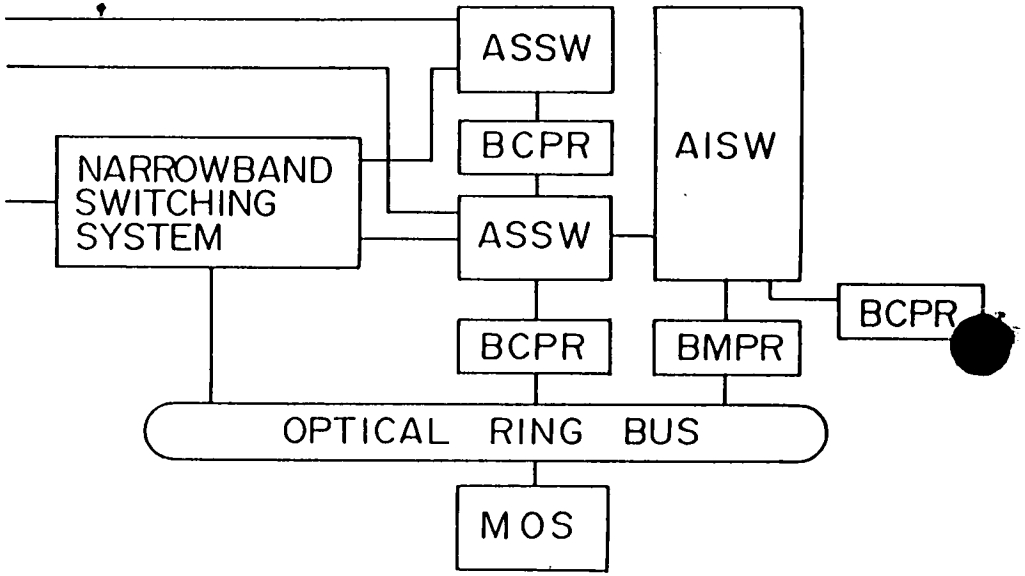
SMALL HOST SWITCH
(BROADBAND ONLY)



LARGE HOST SWITCH
(BROADBAND ONLY)



SMALL HOST SWITCH
(BOTH BROADBAND AND NARROWBAND)

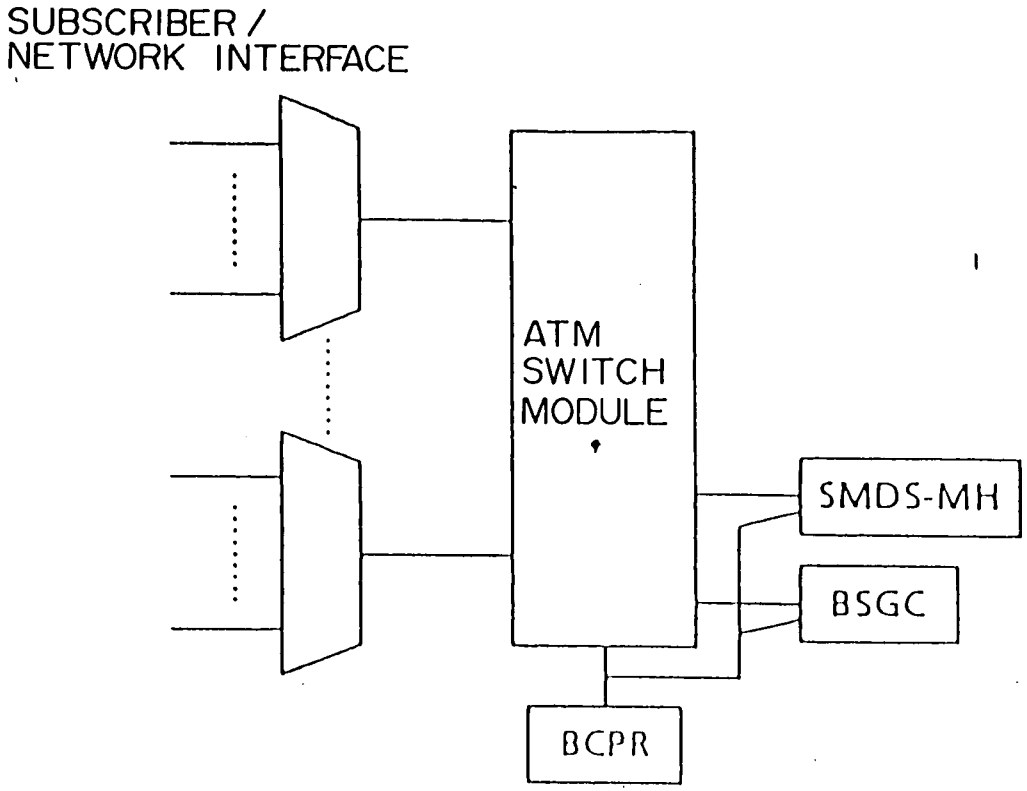


AISW : ATM INTERCONNECTION SWITCH
ASSW : ATM SUBSCRIBER SWITCH
BMPR : BROADBAND MAIN PROCESSOR
MOS : MAINTENANCE AND OPERATION SUBSYSTEM

FIG. 15

6892E0 EP82260

APPROVED BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



ASM : ATM SWITCH MODULE
BCPR : BROADBAND CALL PROCESSOR
BSGC : BROADBAND SIGNALING CONTROLLER
SMDS-MH : SMDS MESSAGE HANDLER

FIG. 16

669260 EP02260

APPROVED
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

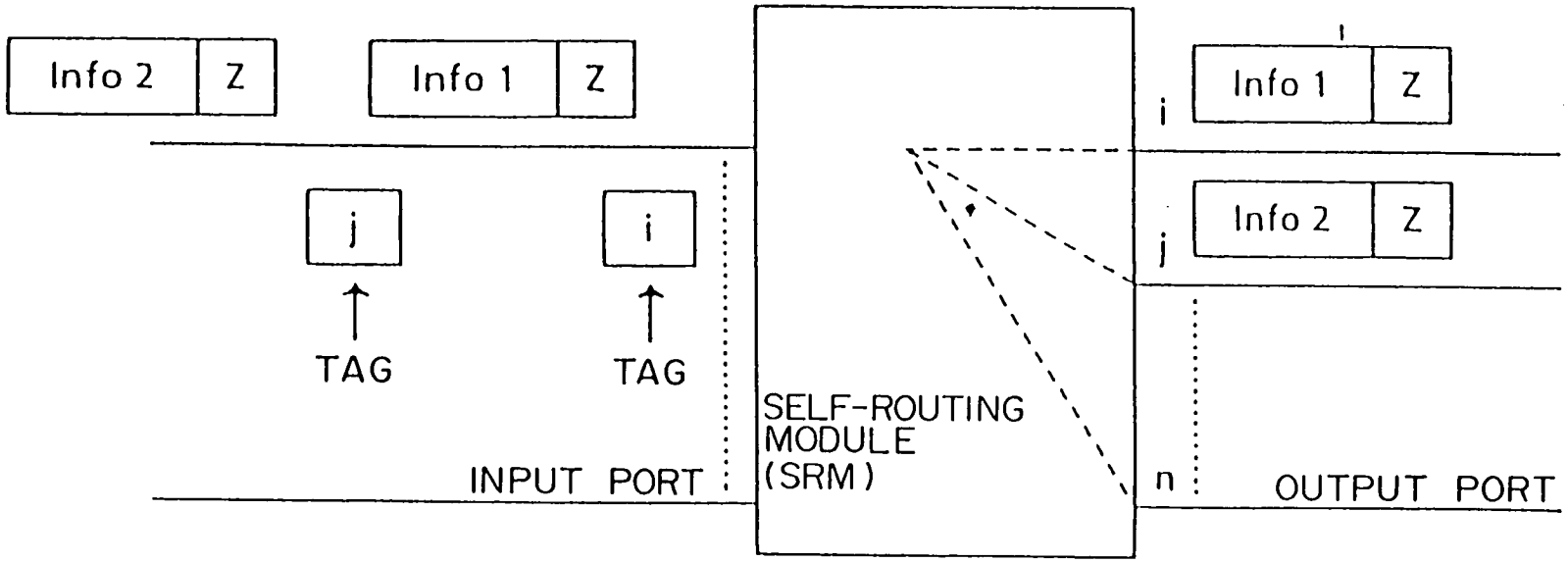


FIG. 17

APPROVED
BY
DRAFTSMAN

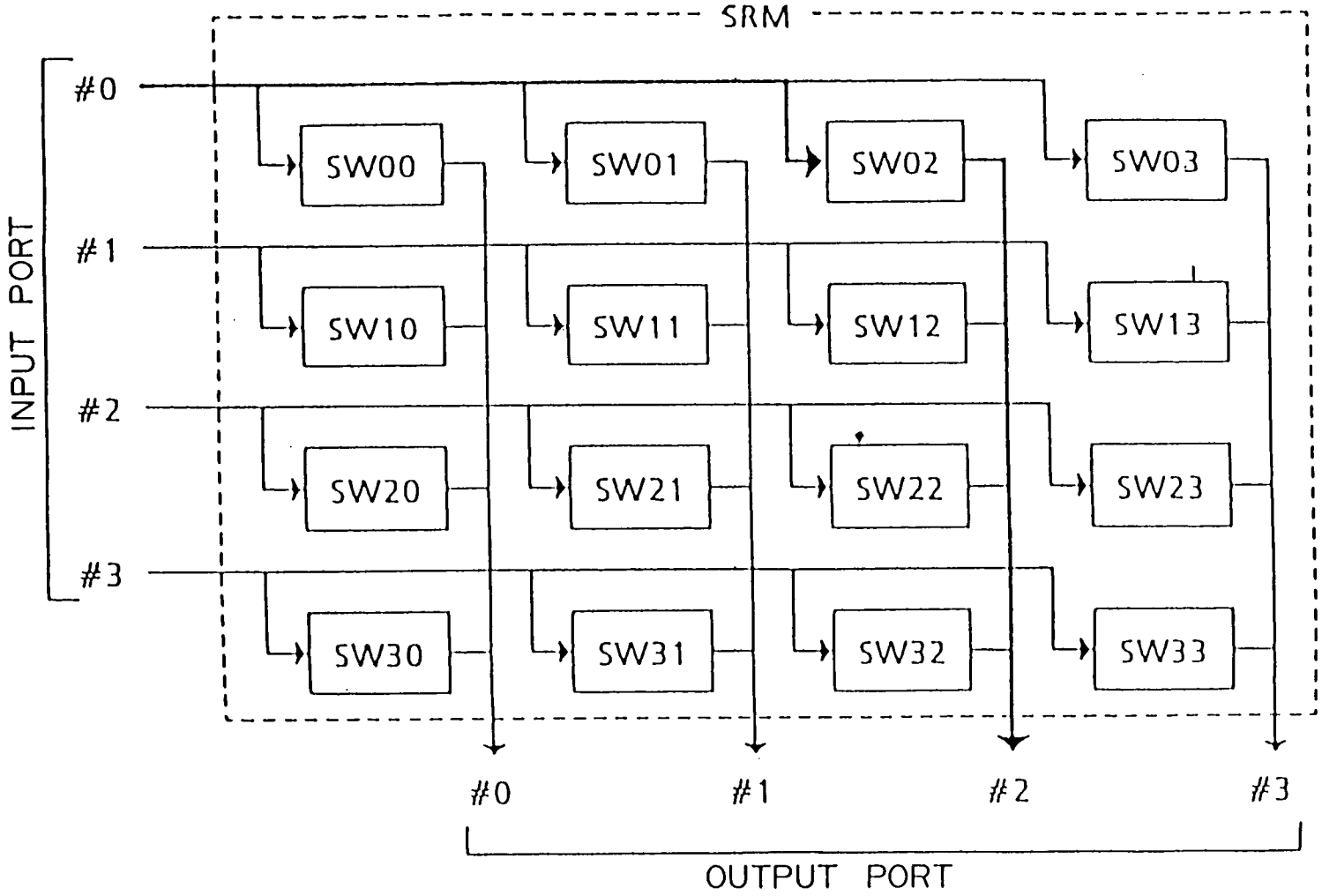
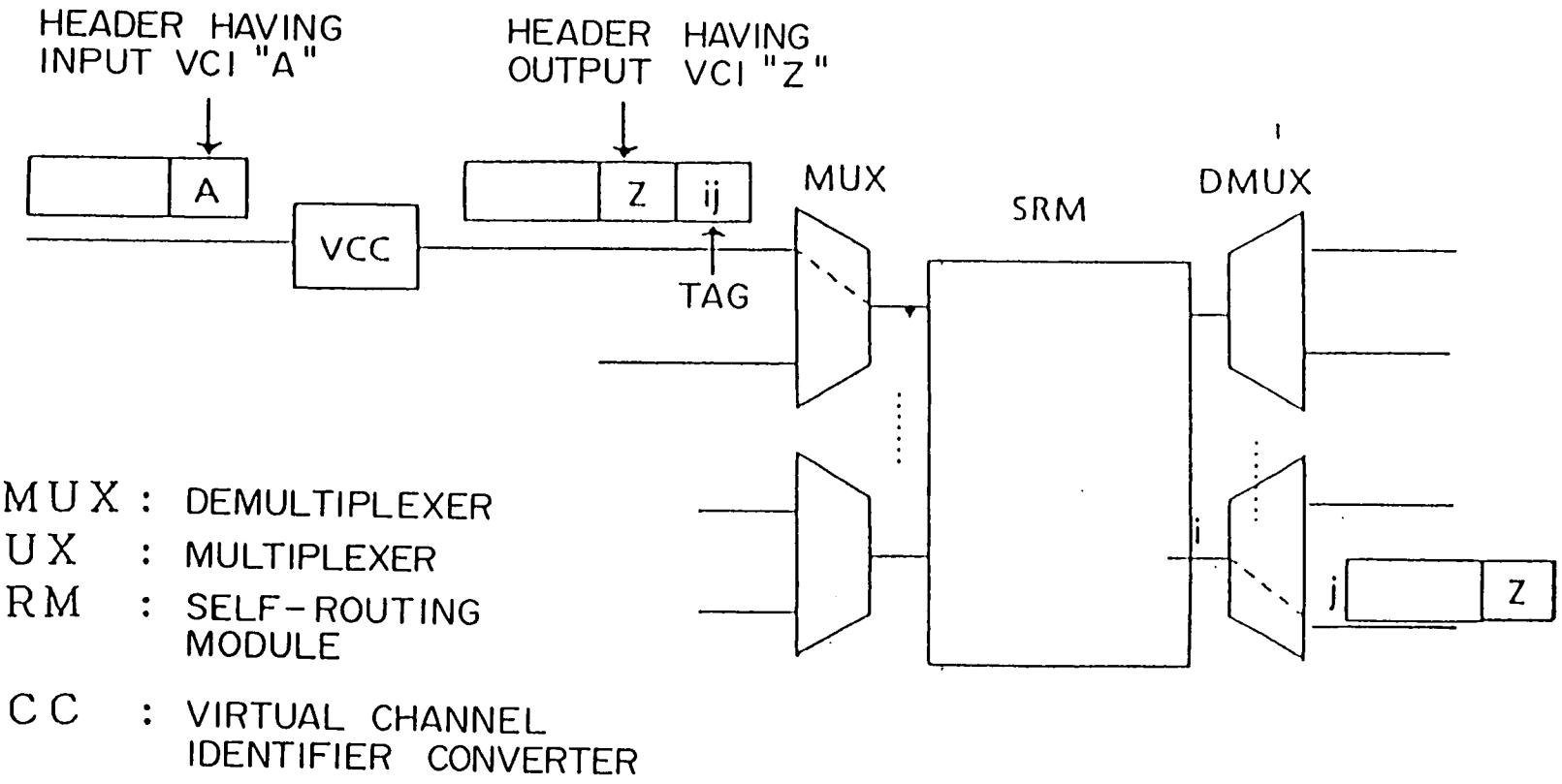


FIG. 18

APPROVED BY
O.G. FIG.
CLASS
SUBCLASS



DMUX : DEMULTIPLEXER
MUX : MULTIPLEXER
SRM : SELF-ROUTING MODULE
VCC : VIRTUAL CHANNEL IDENTIFIER CONVERTER

FIG. 19

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

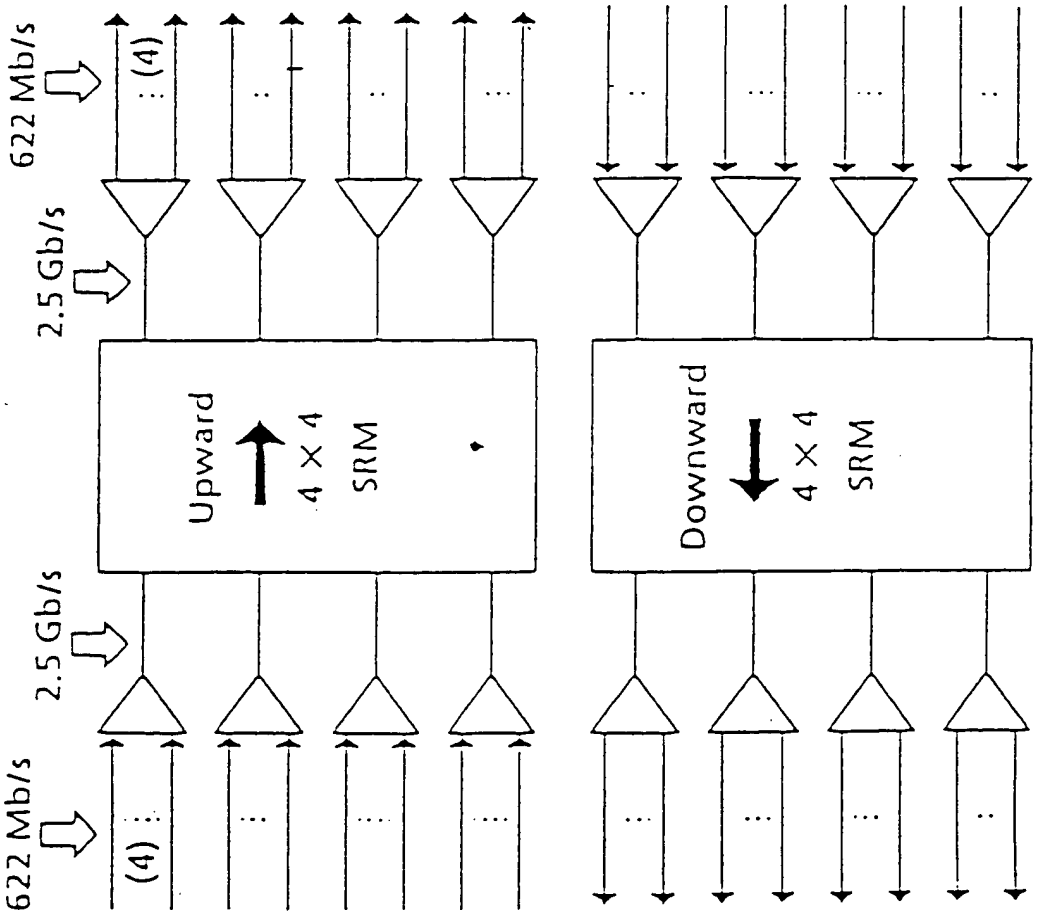


FIG. 20

APPROVED
BY
DRAFTSMAN
O.G. FIG.
CLASS

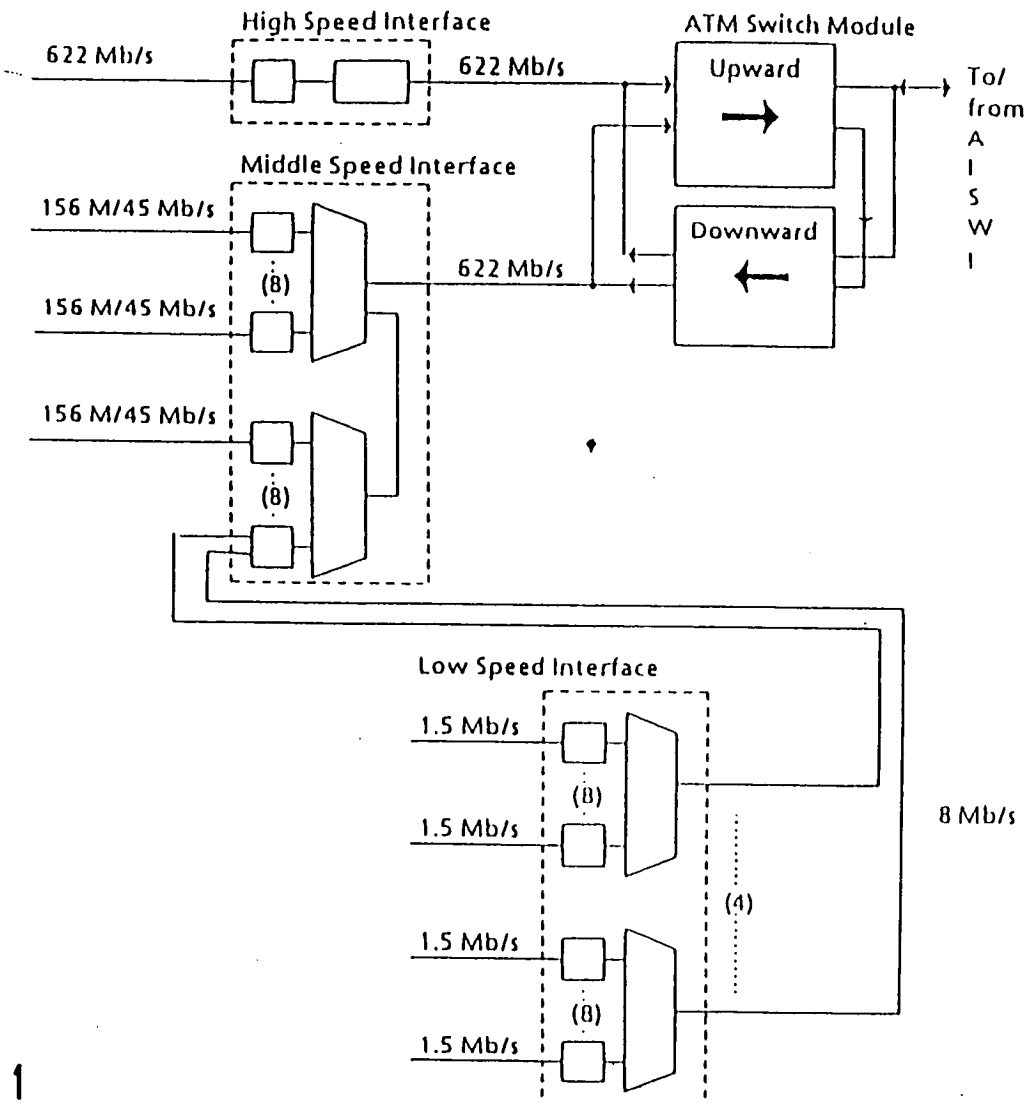
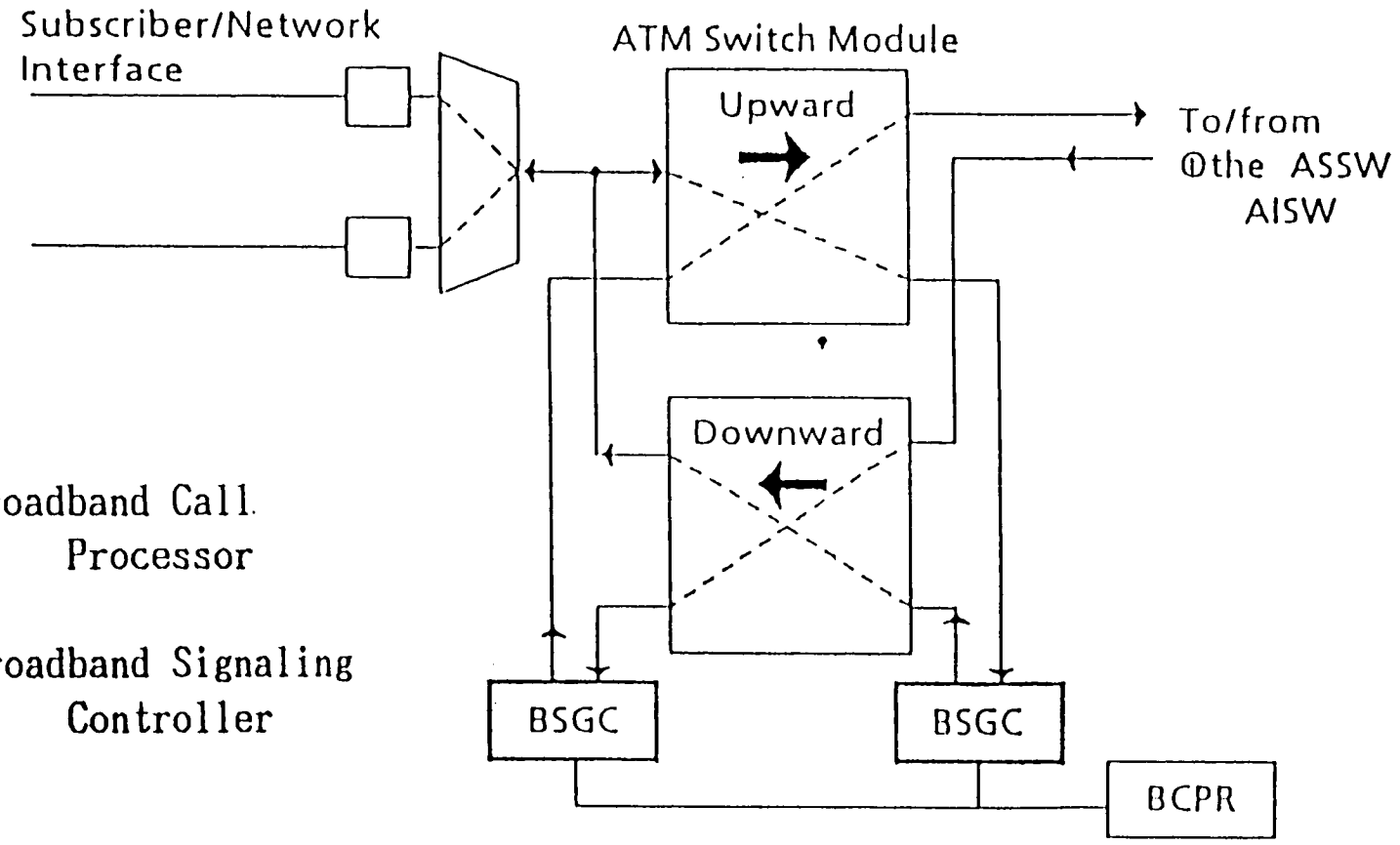


FIG. 21

APPROVED BY DRAFTSMAN
CLASS
SUBCLASS
O.G. FIG.



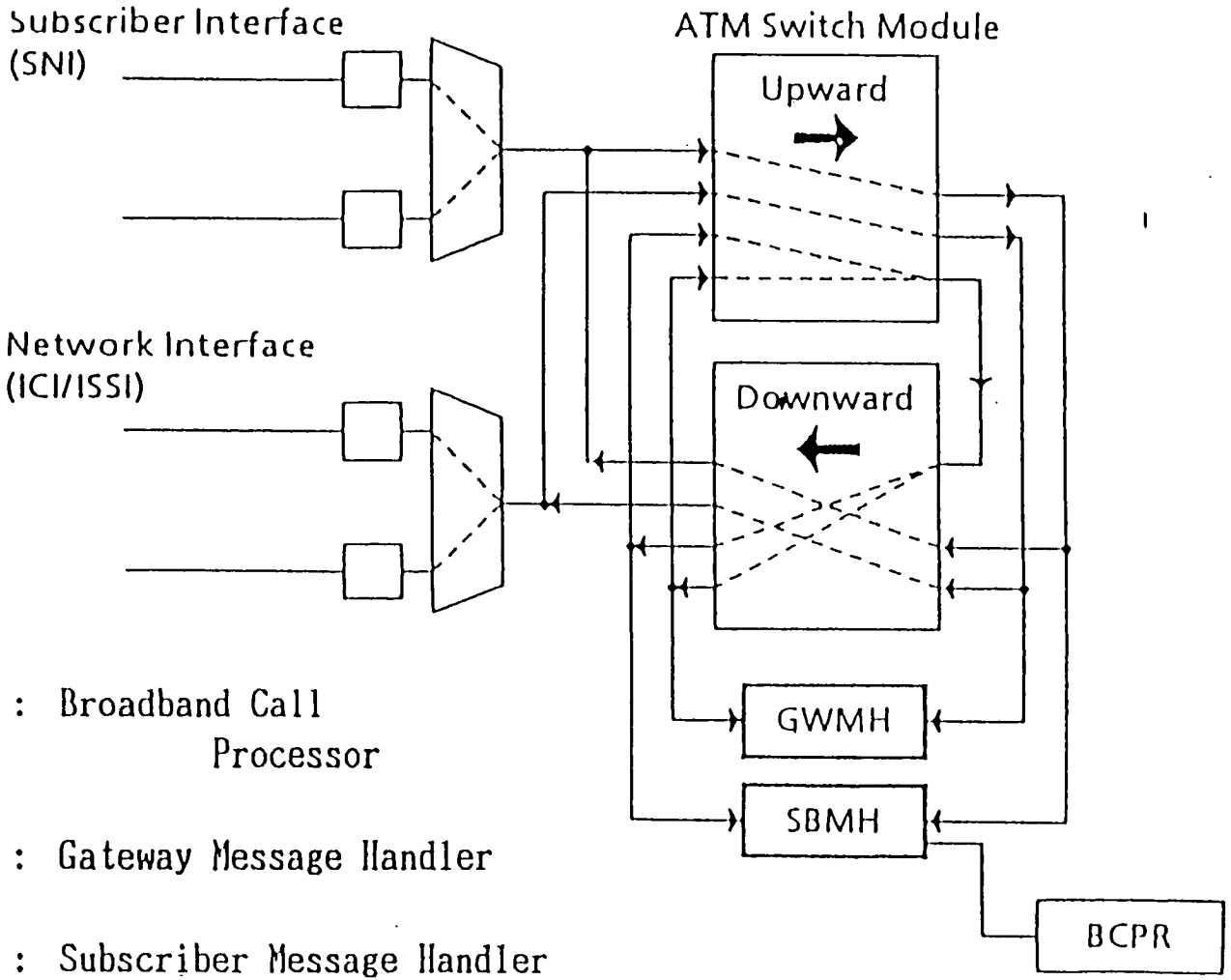
BCPR : Broadband Call Processor

BSGC : Broadband Signaling Controller

FIG. 22

6692E0 EP2728A0

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



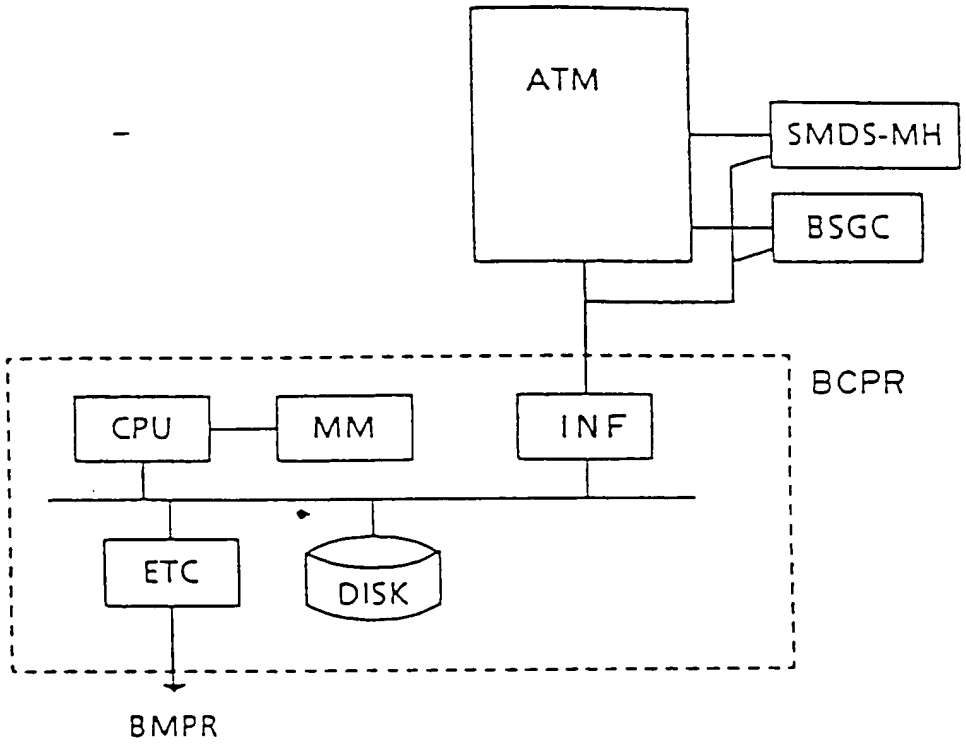
BCPR : Broadband Call Processor

GWMH : Gateway Message Handler

SBMH : Subscriber Message Handler

FIG. 23

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



BCPR : Broadband Call Processor

BMPR : Broadband Main Processor

BSGC : Broadband Signaling Controller

CPU : Central Processing Unit

ETC : Ethernet Controller

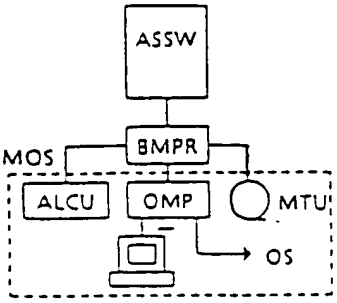
MM : Main Memory

INF : Interface

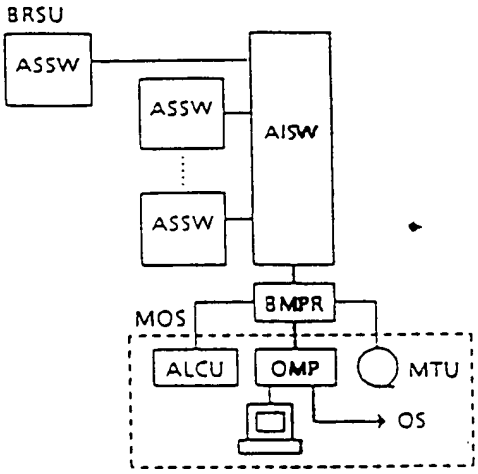
SMDS-MH : SMDS Massage Handler

FIG. 24

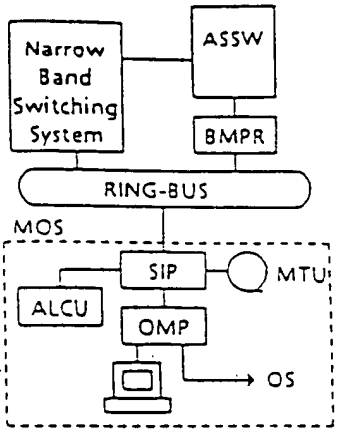
APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



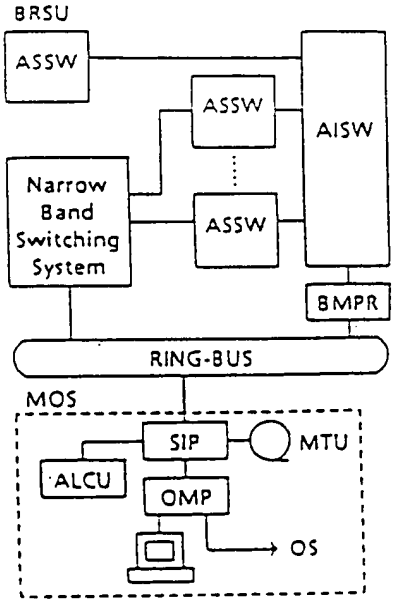
<Small Host: Broadband only>



<Large Host: Broadband only>



<Small Host with Narrow band>



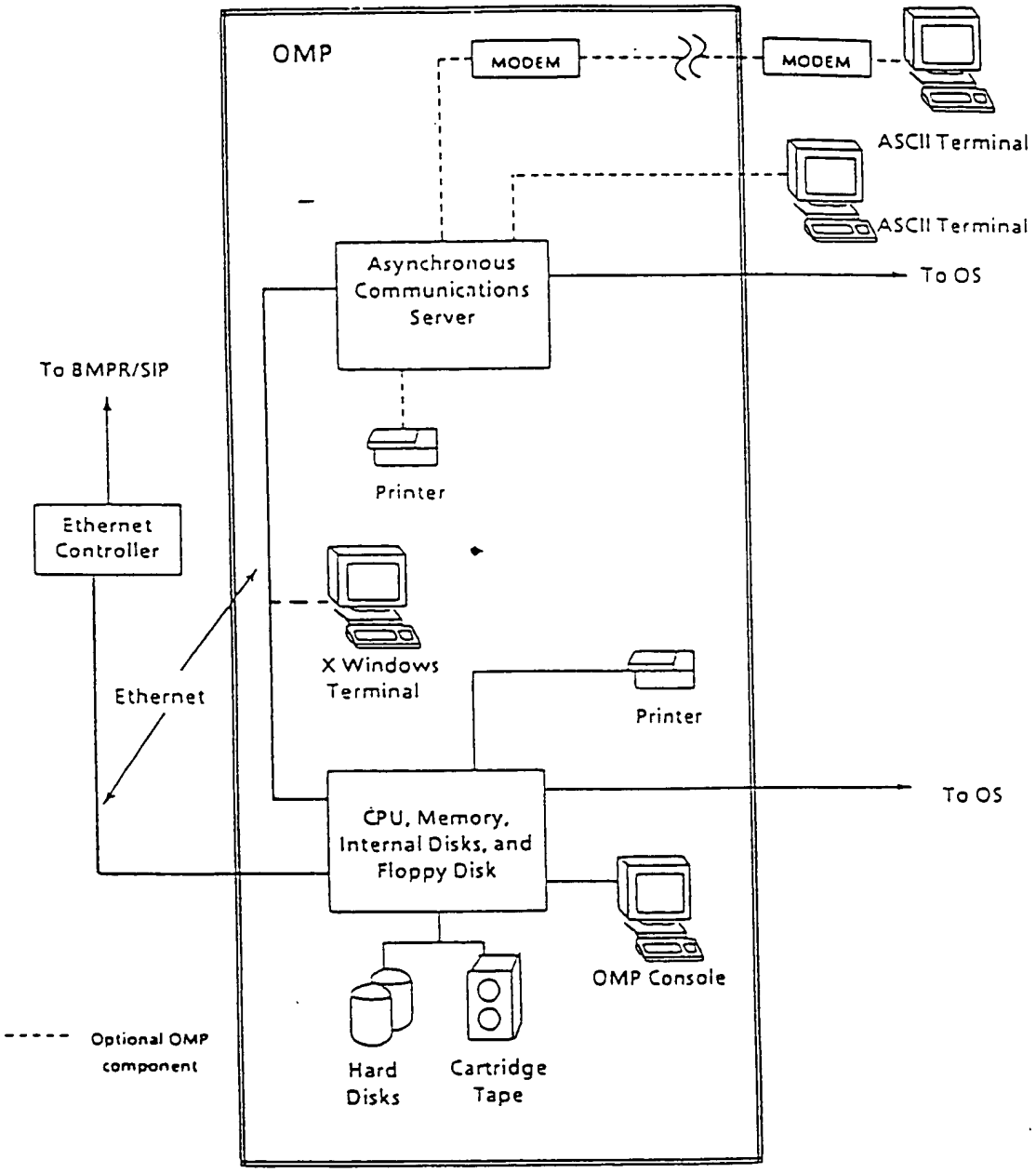
<Large Host with Narrow band>

Legend

ISW : ATM Interconnection Switch
ALCU : Alarm Control Unit
ASSW : ATM Subscriber Switch
BMPR : Broadband Main Processor
BRSU : Broadband Remote Switching Unit
MTU : Magnetic Tape Unit
MOS : Maintenance and Operation Subsystem
SIP : System Integration Processor
OMP : Operation and Maintenance Processor
OS : Operations System

FIG. 25

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



BMPR : Broadband Main Processor

OS : Operations Support System

SIP : Systems Integration Processor

FIG. 26

669220 EP0727860

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

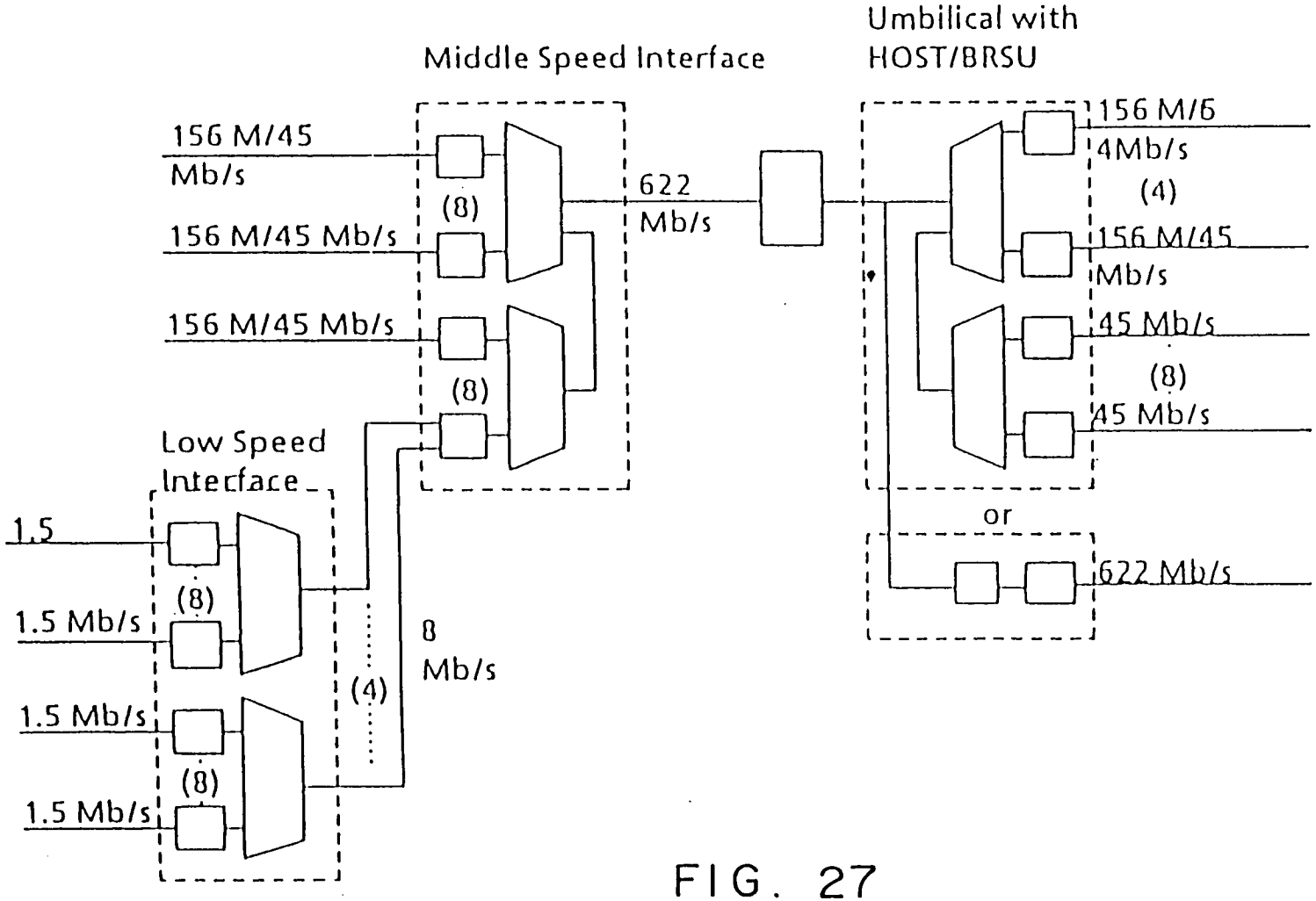
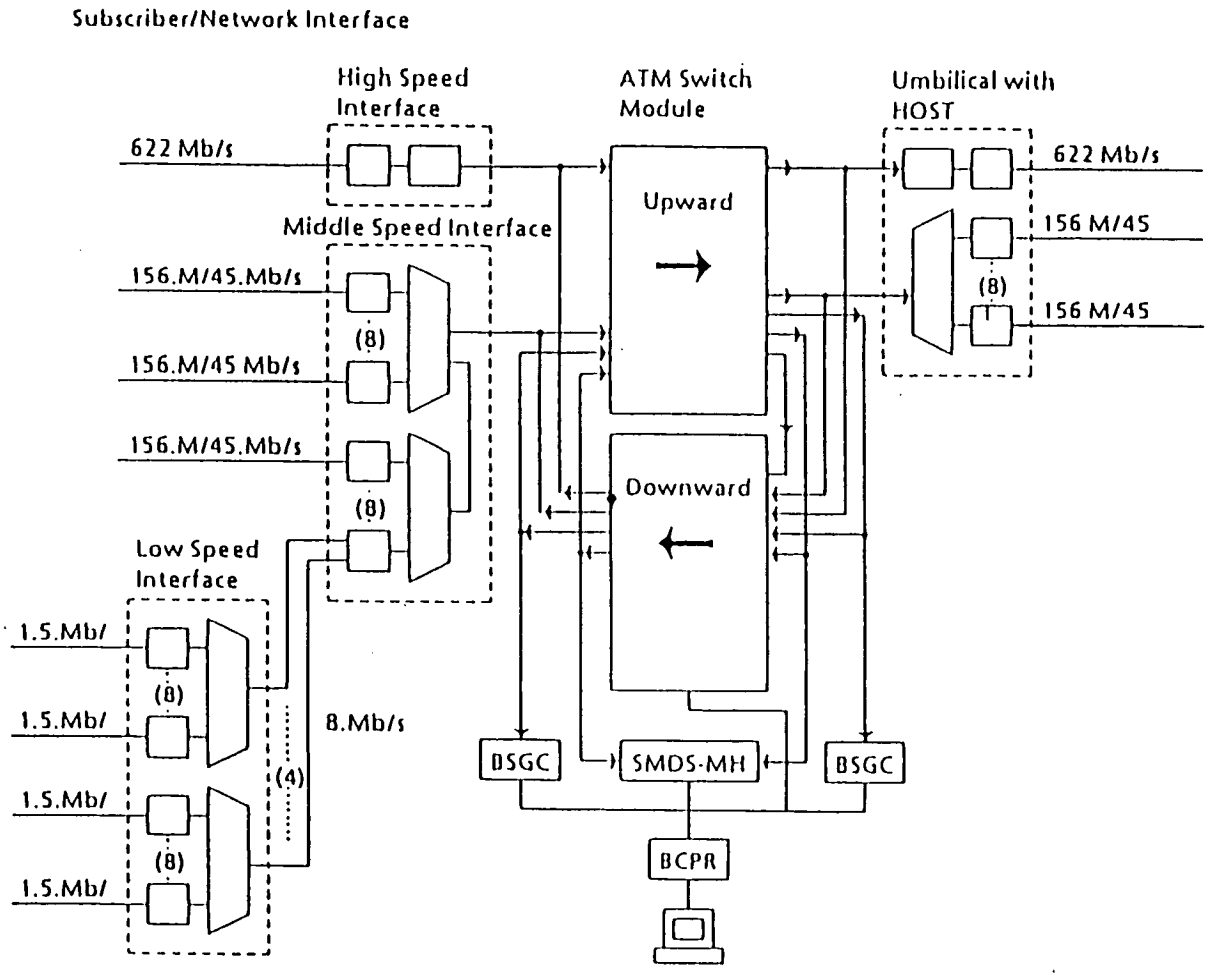


FIG. 27

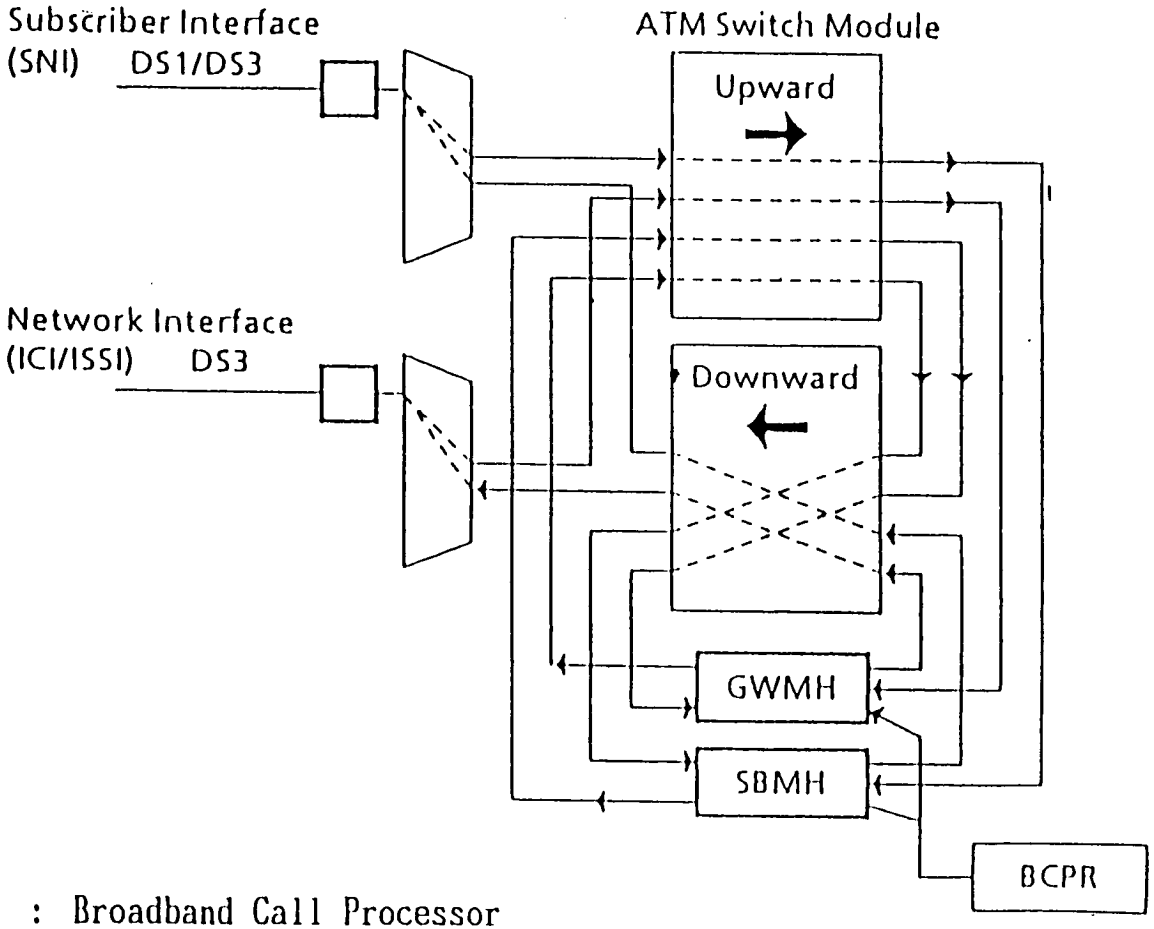
APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



BCPR : Broadband Call Processor
BSGC : Broadband Signaling Controller
SMDS-MH : SMDS Message Handler

FIG. 28

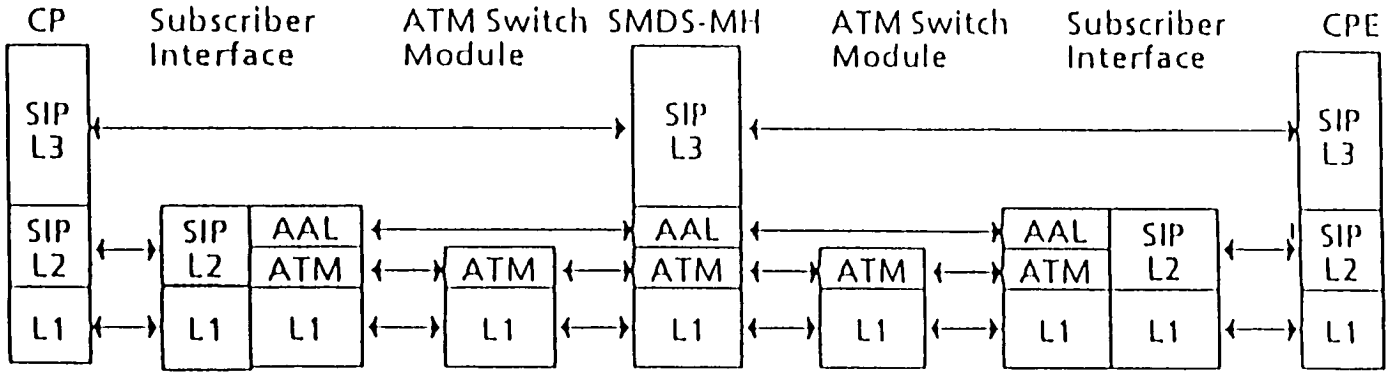
APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



BCPR : Broadband Call Processor
GWMH : Gateway Message Handler
SBMH : Subscriber Message Handler

FIG. 29

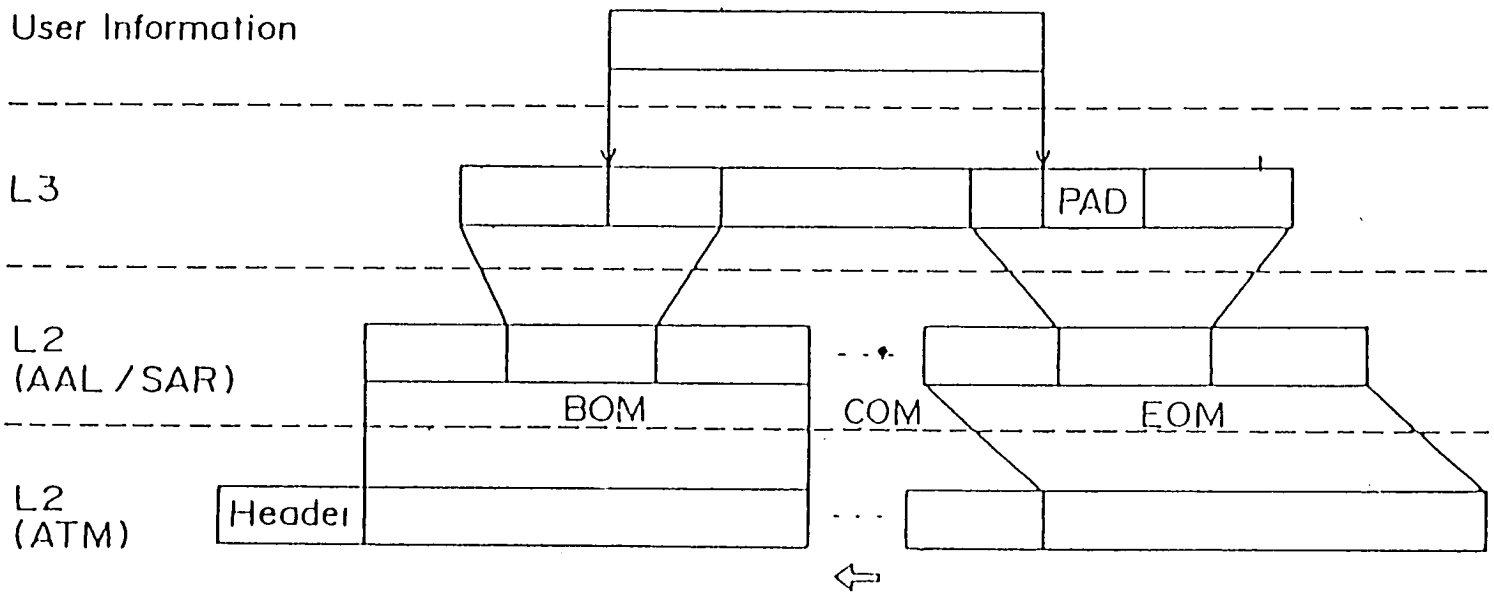
APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



AAL : ATM Adaptation Layer
ATM : ATM Layer
CPE : Customer Premises Equipment
SMDS-MH : SMDS Message Handler
SIP : SMDS Interface Protocol

FIG. 30

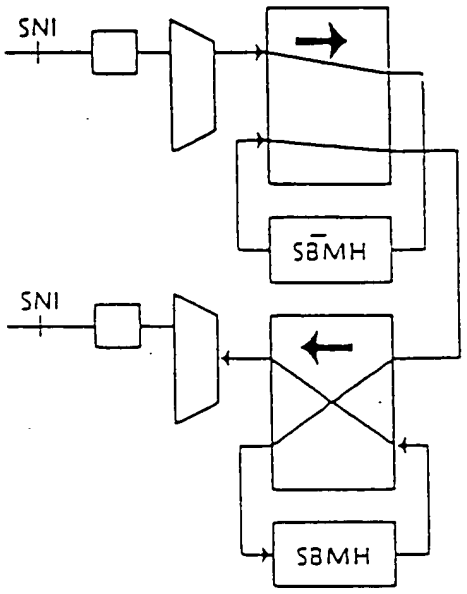
APPROVED
BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



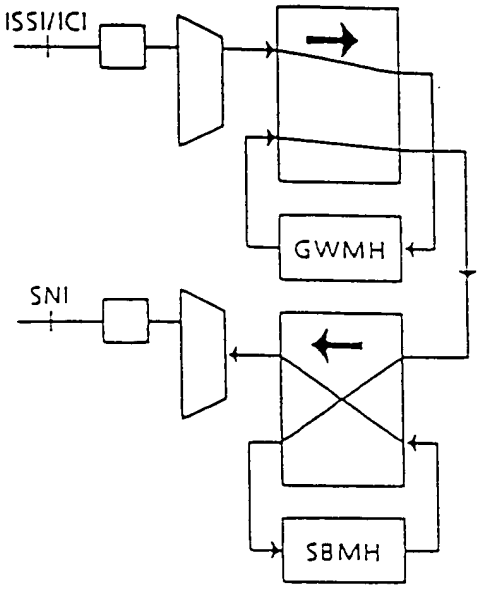
BOM : Beginning of Message
COM : Continuation of Message
EOM : End of Message
SAR : Segmention and Re-assembly

FIG. 31

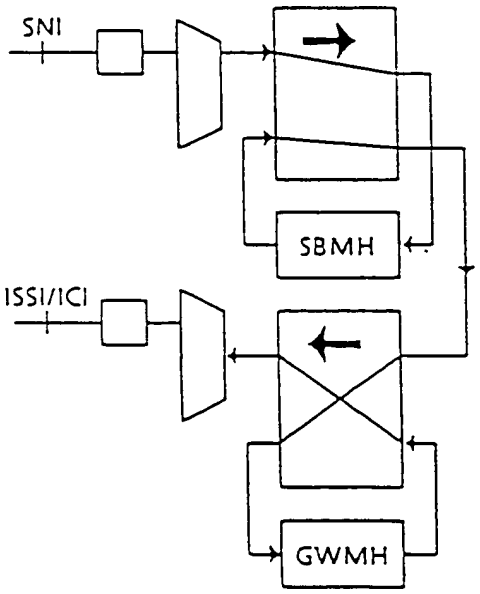
APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



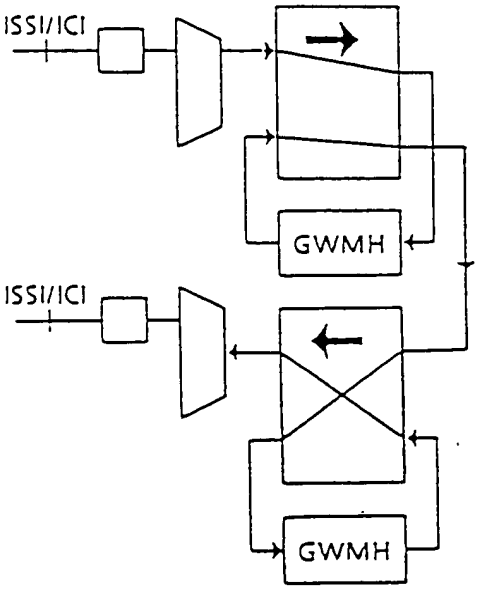
Intra-office connection



Incoming Connection



Outgoing Connection



Transit Connection

FIG. 32

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

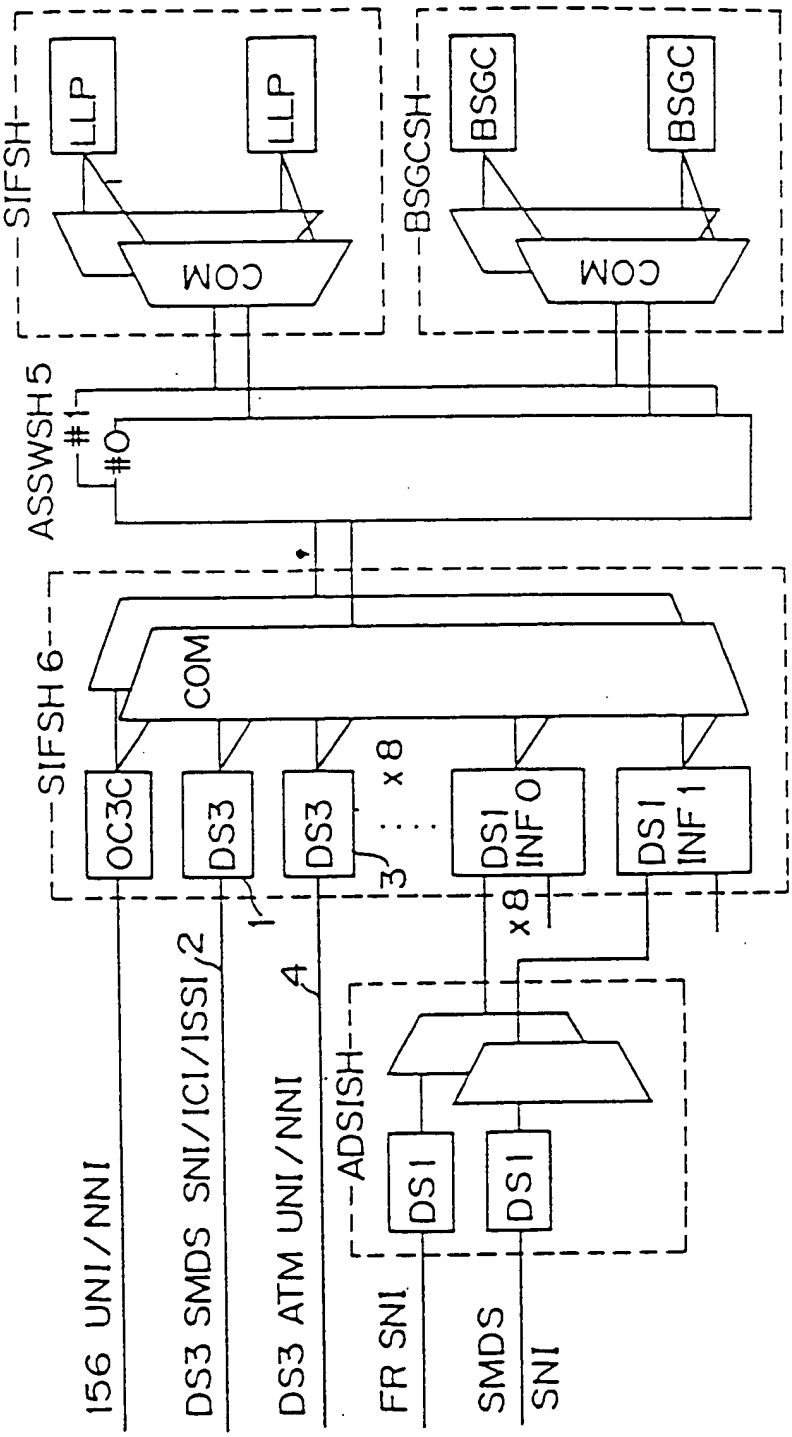


FIG. 33

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

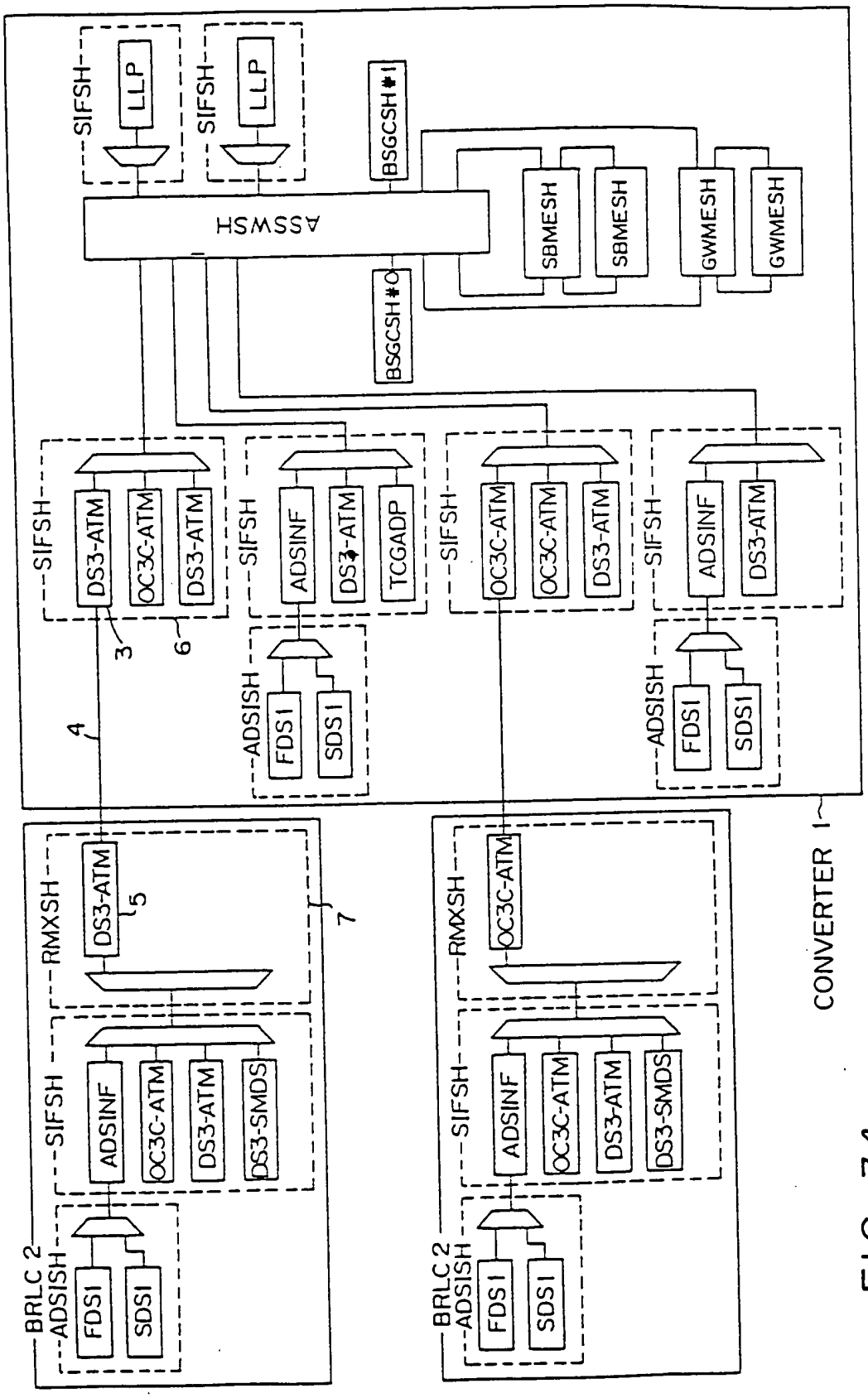


FIG. 34

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

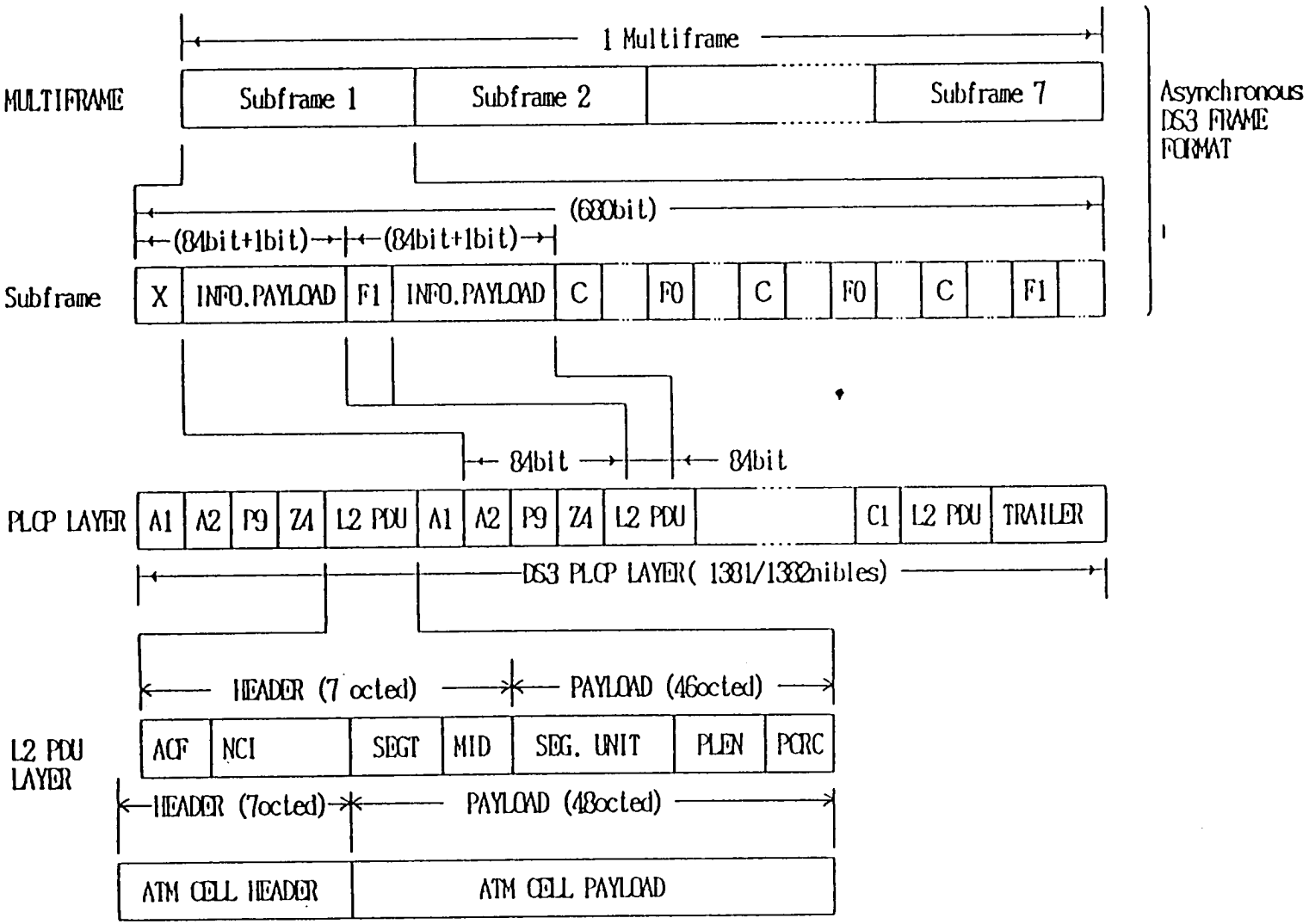
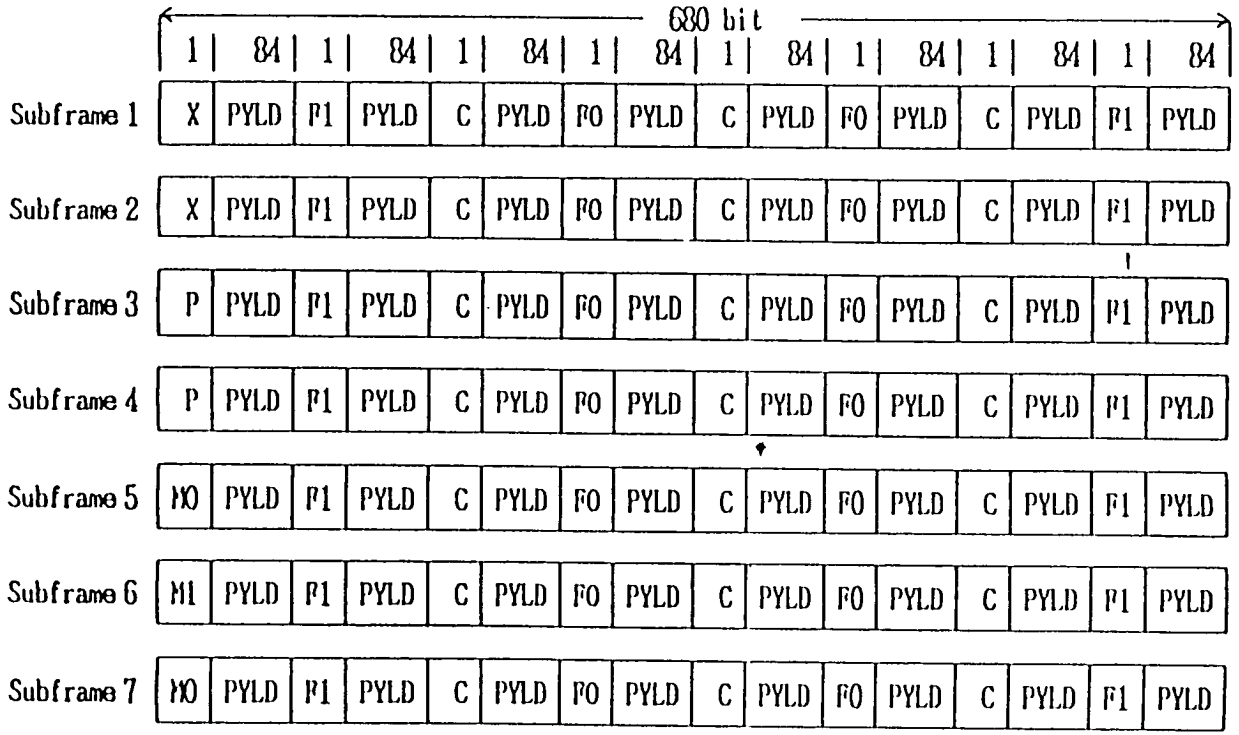


FIG. 35

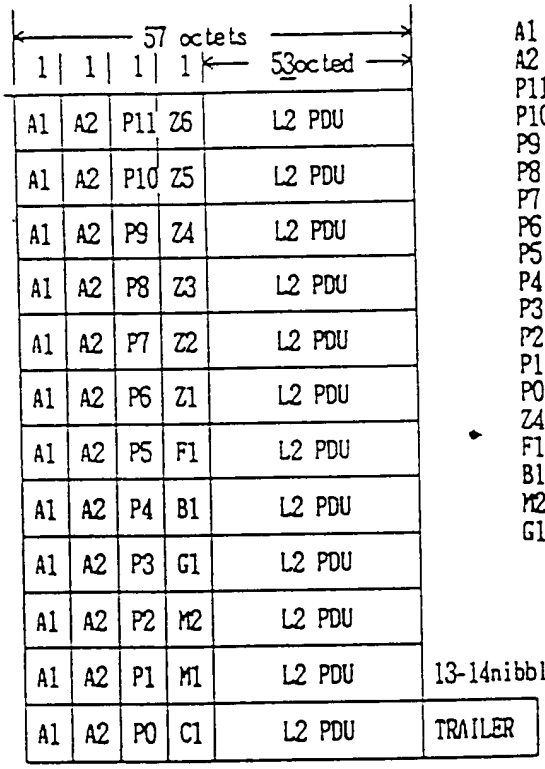
APPROVED
BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



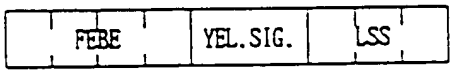
X : YELLOW ALARM (NORMALLY X = 1. TWO X BITS IN SAME MULTIFRAME SHARE SAME VALUE)
M0, M1 : MULTIFRAME ALIGNMENT (M0 = 0, M1 = 1)
F0, F1 : SUBFRAME ALIGNMENT (F0 = 0, F1 = 1)
P : PARITY (OF EVEN NUMBER FOR PRECEDING INFORMATION PAYLOAD)
C : AIS (AIS C = 0, X = 1, PYLD = 1010, · · · · · 10)

FIG. 36

APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS



A1 : Frameing octed (11110110)
A2 : Frameing octed (00101000)
P11 : Path Overhead Identifier octed (00101100)
P10 : Path Overhead Identifier octed (00101001)
P9 : Path Overhead Identifier octed (00100101)
P8 : Path Overhead Identifier octed (00100000)
P7 : Path Overhead Identifier octed (00011100)
P6 : Path Overhead Identifier octed (00011001)
P5 : Path Overhead Identifier octed (00010101)
P4 : Path Overhead Identifier octed (00010000)
P3 : Path Overhead Identifier octed (00001101)
P2 : Path Overhead Identifier octed (00001000)
P1 : Path Overhead Identifier octed (00000100)
P0 : Path Overhead Identifier octed (00000001)
Z4-0 : Growth octed (default 00000000)
F1 : PLCP Path User Channel (default 00000000)
B1 : Bit Interleaved Parity-8 (even parity)
M2-1 : SIP Level 1 Control Information
G1 : PLCP Path Status



FEBE : Far End Block Error
YEL.SIG : Yellow Signal (normal 0)
LSS : Link Status Signal

LSS	Link Status	Incoming SIG/LSS
000	connected	connected
000	connected	rx link up
110	rx link up	rx link dn
110	rx link up	PLCP Out-Of-Frame
011	rx link dn	PLCP Loss-Of-Frame

C1 : Cycle/Stuff Counter
TRAILER : Trailer Nibble (1100)

C1 Code	Frame in Cycle	Trailer Length
11111111	1	13 nibbles
00000000	2	14 nibbles
01100110	3 (no stuff)	13 nibbles
10011001	4 (stuff)	14 nibbles

FIG. 37

669260 ET24260

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

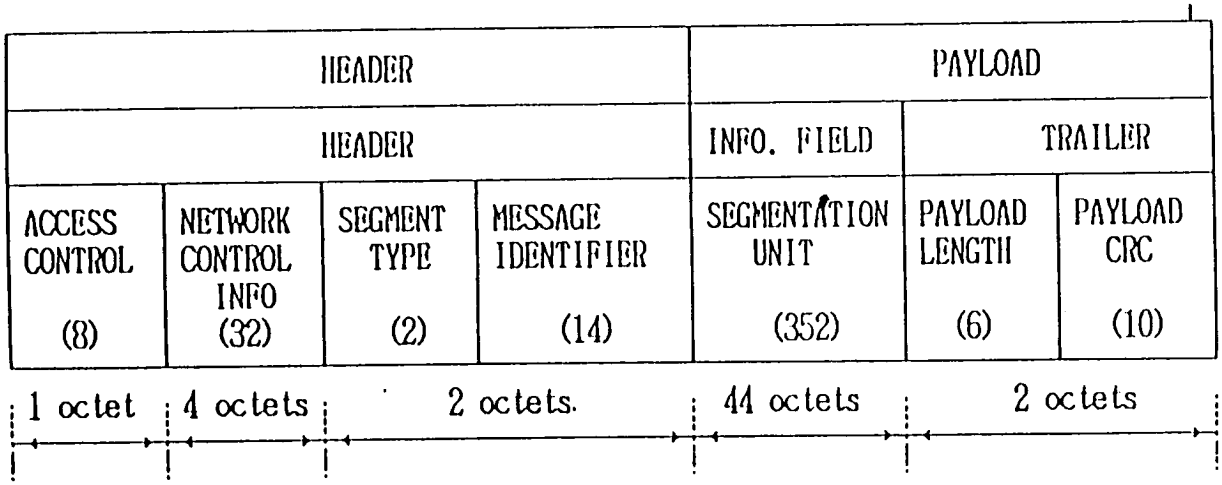


FIG. 38

APPROVED BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

DIR.	SNI	NNI
UP	BUSY | X | X | X | X | REQ2 | REQ1 | REQ0 BUSY : CONTAIN INFORMATION =1, EMPTY =0 REQ2 : PRIORITY LEVEL 2 REQ1 : PRIORITY LEVEL 1 REQ0 : PRIORITY LEVEL 0 REQUEST FOR SEND = 0, NO REQUEST=1 X : NOT PROCESSED BY THE NETWORK	BUSY | DC | DC | DC | DC | DC | DC | DC BUSY : VALID CELL = 1, INVALID CELL =0 DC : DON'T CARE
DOWN	BUSY | 0 | 0 | 0 | 0 | 0 | 0 | 0 BUSY : CONTAIN INFORMATION =1, EMPTY =0	BUSY | 0 | 0 | 0 | 0 | 0 | 0 | 0 BUSY : VALID CELL = 1, INVALID CELL= 0

FIG. 39

669260 EP2272260

APPROVED
DRAFTSMAN
BY
O.G. FIG.
CLASS
SUBCLASS

	VCI	PT	SP	HCS
IF L2 PDU CONTAINS INFORMATION DATA	11111111 11111111 1111	00	00	00100010
IF L2 PDU CONTAINS NO INFORMATION DATA	00000000 00000000 0000	00	00	00000000

FIG. 40

6092E0 EP82260

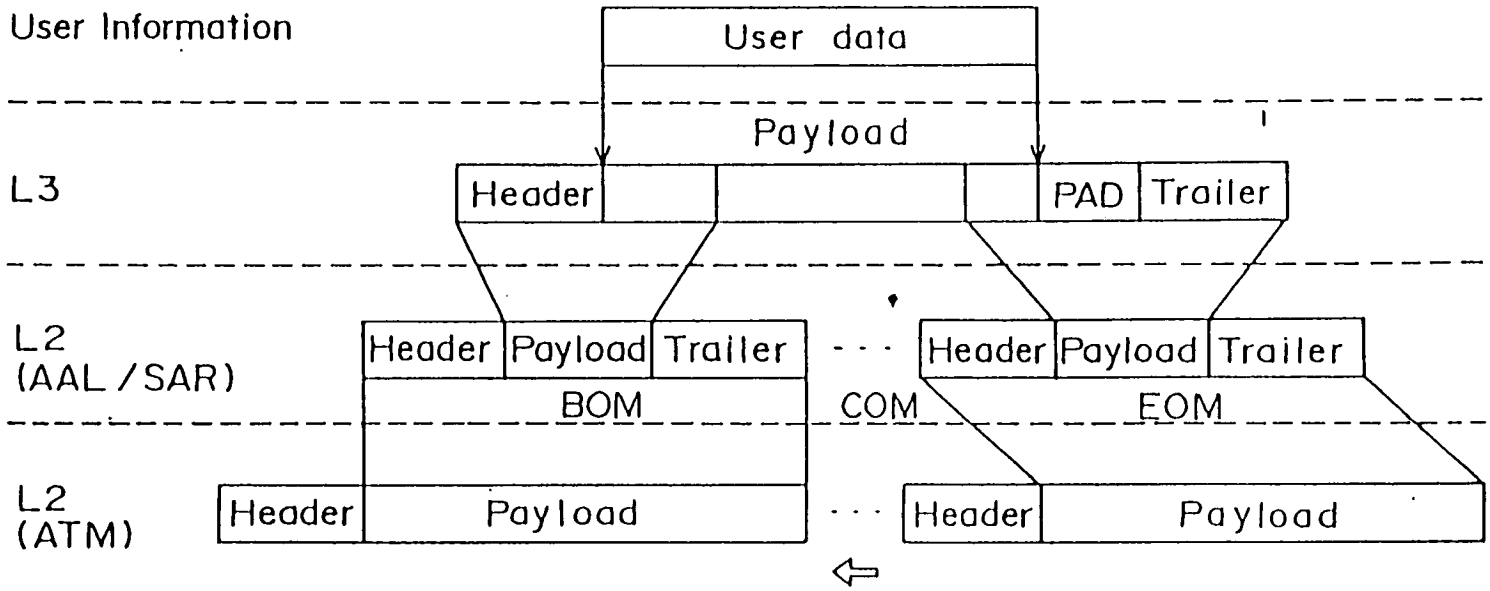
APPROVED BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

VALUE	MEANING
00	CONTINUATION MESSAGE (COM) (EMPTY L2 PDU FROM MSS)
01	END OF MESSAGE (EOM)
10	BEGINNING OF MESSAGE (BOM)
11	SINGLE SEGMENT MESSAGE (SSM)

FIG. 41

0692E0 EP2772260

APPROVED O.G. FIG.
BY
DRAFTSMAN
CLASS
SUBCLASS



BOM : Beginning of Message
COM : Continuation of Message
EOM : End of Message
SAR : Segmention and Re-assembly

FIG. 42

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

5,568,475

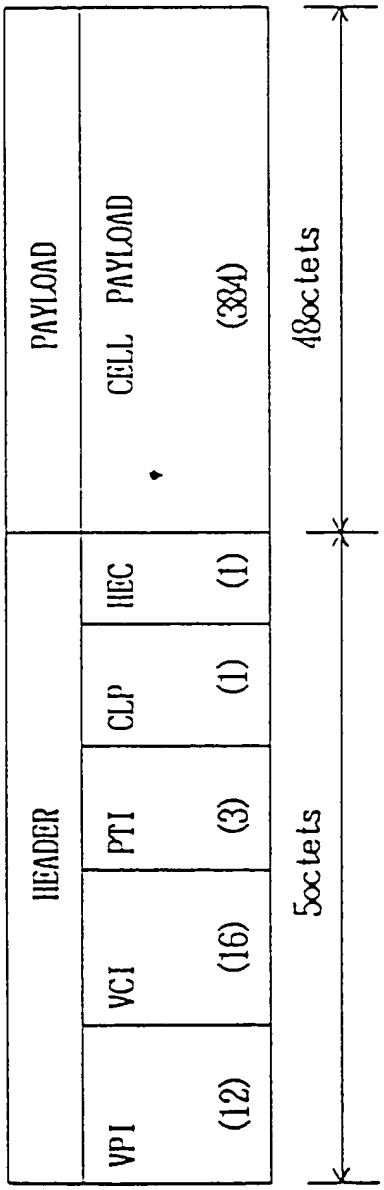


FIG. 43

6692E0 EP2726O

APPROVED
BY
DRAFTSMAN
CLASS
SUBCLASS
O.G. FIG.

FUNCTION	VPI	VCI	PT	CLP
UNASSIGNED CELL	00000000 0000	0000 00000000 0000	XXX	0
ASSIDNED CELL	YYYYYYYY YYYY	YYYY YYYYYYYY YYYY	YYY	Y

X : NOT FIXED
Y : OPTIONAL

FIG. 44

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

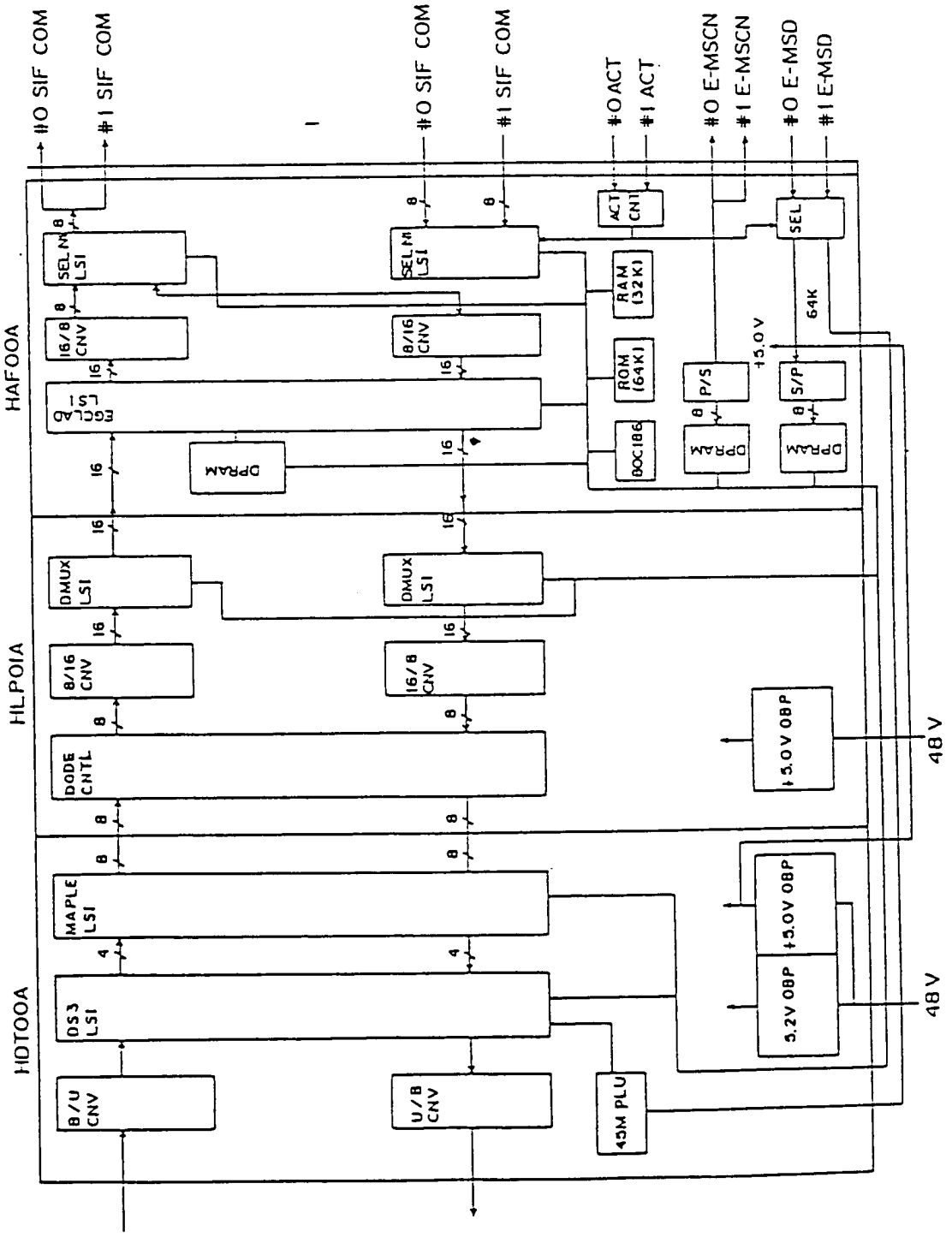


FIG. 45

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

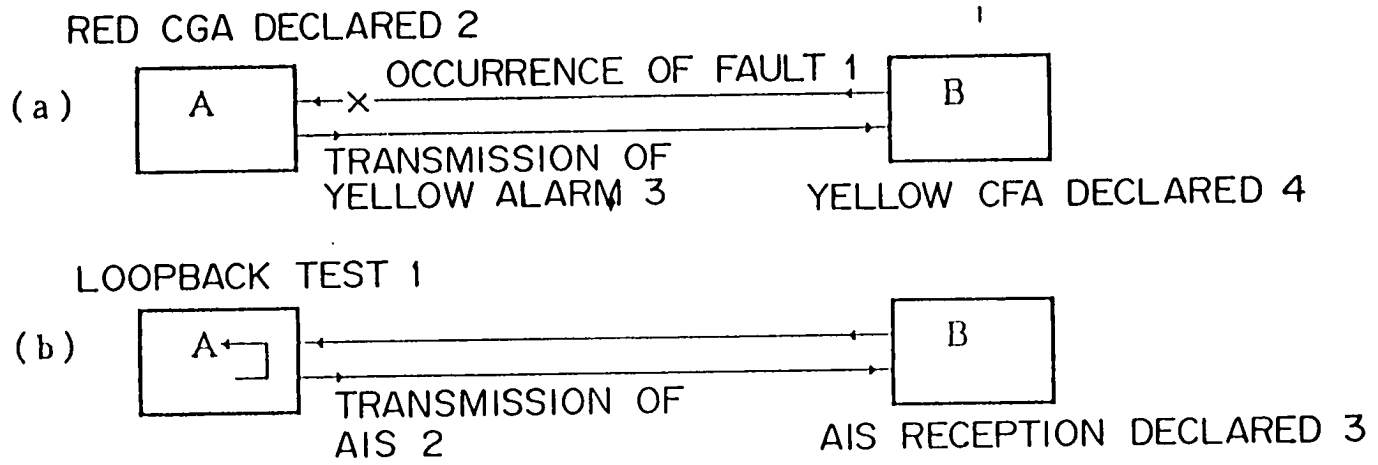


FIG. 46

FAULTY DETECTION	FAULT TO BE MASKED					
	LOS	AIS	OOF	YEL	POOF	PYEL
LOS	–	X	X	X	X	X
AIS		–	X	X	X	X
OOF			–	X	X	X
YEL	–			–		
POOF					–	X
PYEL						–

"X" INDICATES FAULT TO BE MASKED

POOF : PLCP OOF

PYEL : PLCP YELLOW SIGNAL

FIG. 47

APPROVED BY DRAFTSMAN
O.G. FIG. CLASS SUBCLASS

6692E0 EP22260

APPROVED
BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

	DETECTION CONDITION	RECOVERY CONDITION	REACTION
LOS OF SIGNAL	175±75 SEQUENCE OF 0 (NO PULSE)	AVERAGE PULSE DENSITY OF 33%	RED CGA DECLRED TRANSMISSION OF YELLOW ALARM
OUT-OF-FRAME (DS3)	THREE OR MORE ERRORS IN FRAME BITS OF 16 OR LESS IN SERIES	Framing bit pattern AND MATCHING OF CRC	RED CGA DECLRED TRANSMISSION OF YELLOW ALARM
AIS	C=0, X=1, INFO. PYLD=1010,...10	VALUES OTHER THAN LEFT DATA	AIS DECLRED TRANSMISSION OF YELLOW ALARM
YELLOW ALARM (DS3)	X=0	X=1	YELLOW SIGNAL RECEPTION DECLARED

FIG. '48

APPROVED
BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

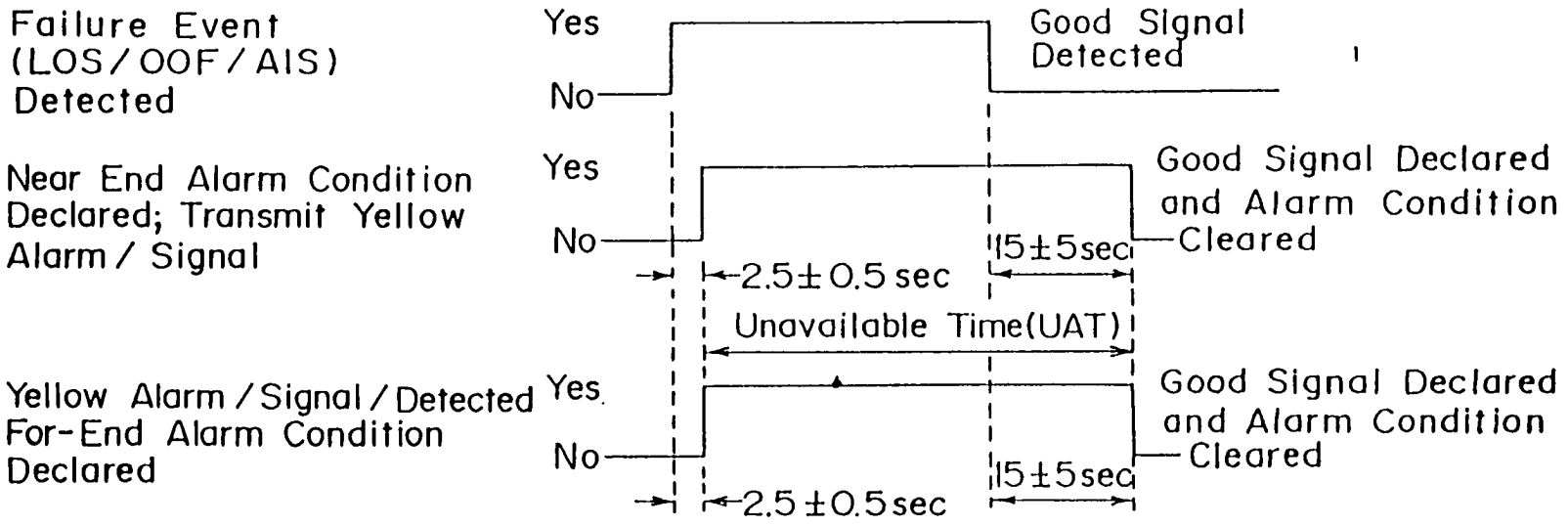


FIG. 49

669260 ET22260

O.G. FIG.
CLASS
SUBCLASS

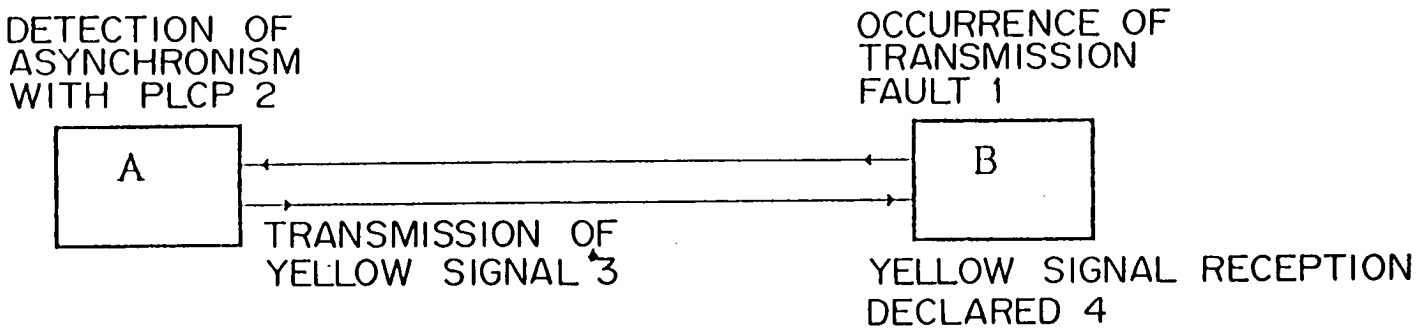


FIG. 50

0692E0 "ET22260

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

	DETECTION CONDITION	RECOVERY CONDITION	REACTION
OUT-OF-FRAME (DS3 PLCP)	A1 AND A2 DETECT REEOR OR PATH OVERHEAD IDENTIFIER DETECTS RERORS TWICE CONTINUOUSLY	MATCHING A1 AND A2, MATCHING PATH OVERHEAD IDENTIFIER	TRANSMISSION OF YELLOW SIGNAL
YELLOW SIGNAL (DS3 PLCP)	DETECTION OF "1" IN FIFTH G1 BIT.	DETECTION OF "0" IN FIFTH G1 BIT.	YELLOW SIGNAL RECEPTION DECLARED

FIG. 51

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

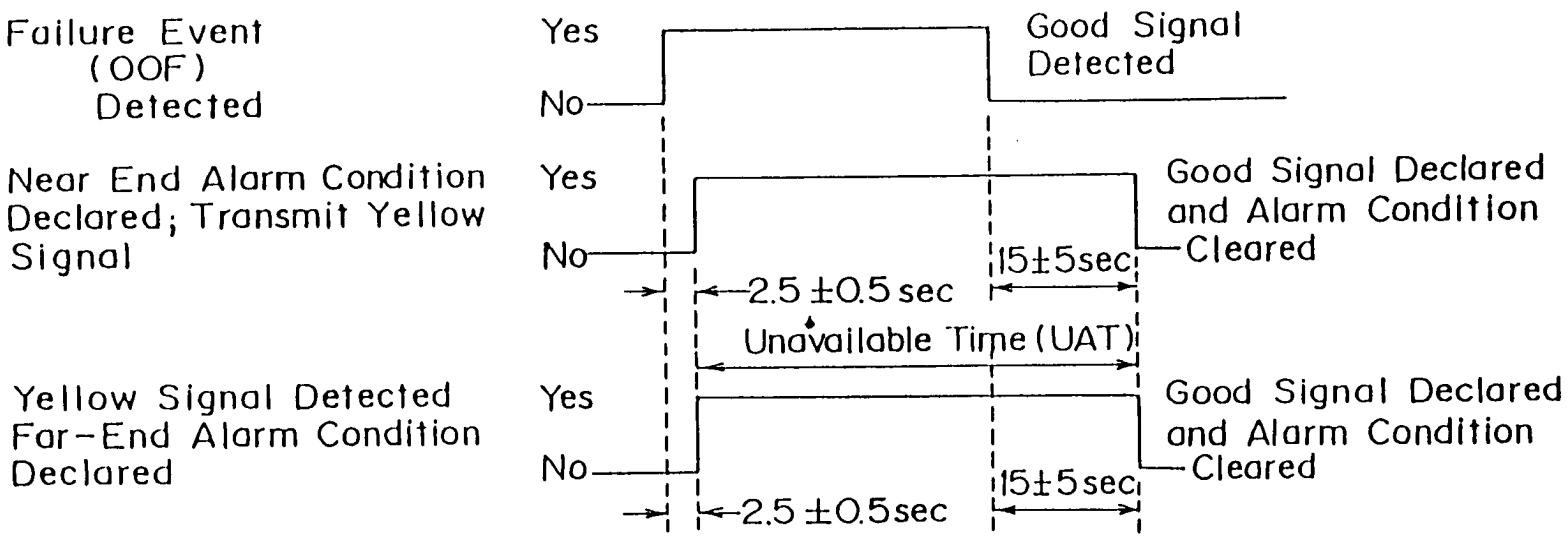


FIG. 52

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

Parameters	Normal counter Advance	Counter Advance During Failure Events and Conditions			
		LOS	OOF	AIS	UAT
LCV	Each BPV	No	Yes	Yes	No
LES	If at least 1 LCV during sec.	Yes	Yes	Yes	No
LSES	If 45 or more LCVs during sec.	Yes	Yes	Yes	No
CV	Each P-bit error	No	No	Yes	No
ES	If at least 1 P-bit error during sec.	No	Yes	Yes	No
SES	If 44 or more P-bit error during sec.	No	Yes	Yes	No
SEFS	If at least one SEF event during sec.	No	Yes	Yes	No
AISS	If at least one incoming AIS during sec.	No	No	No	Yes
UAS	Start at oneset of a failure condition	No	No	No	Yes

FIG. 53

6692E0 ET2726O

APPROVED BY
DRAFTSMAN
C.C. FIG.
CLASS
SUBCLASS

Parameters	Normal counter Advance	Counter Advance During Failure Events and Conditions	
		OOF	UAT
CV(BIP-8)	Each BIP-8	No	No
ES(BIP-8)	If at least 1 BIP-8 during sec,	Yes	No
SES(BIP-8)	If 5 or more BIP-8 error during sec.	Yes	No
SEFS(BIP-8)	If at least one SEFS during sec.	Yes	No
UAS(BIP-8)	Status at oneset of a failure condition	No	Yes

FIG. 54

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

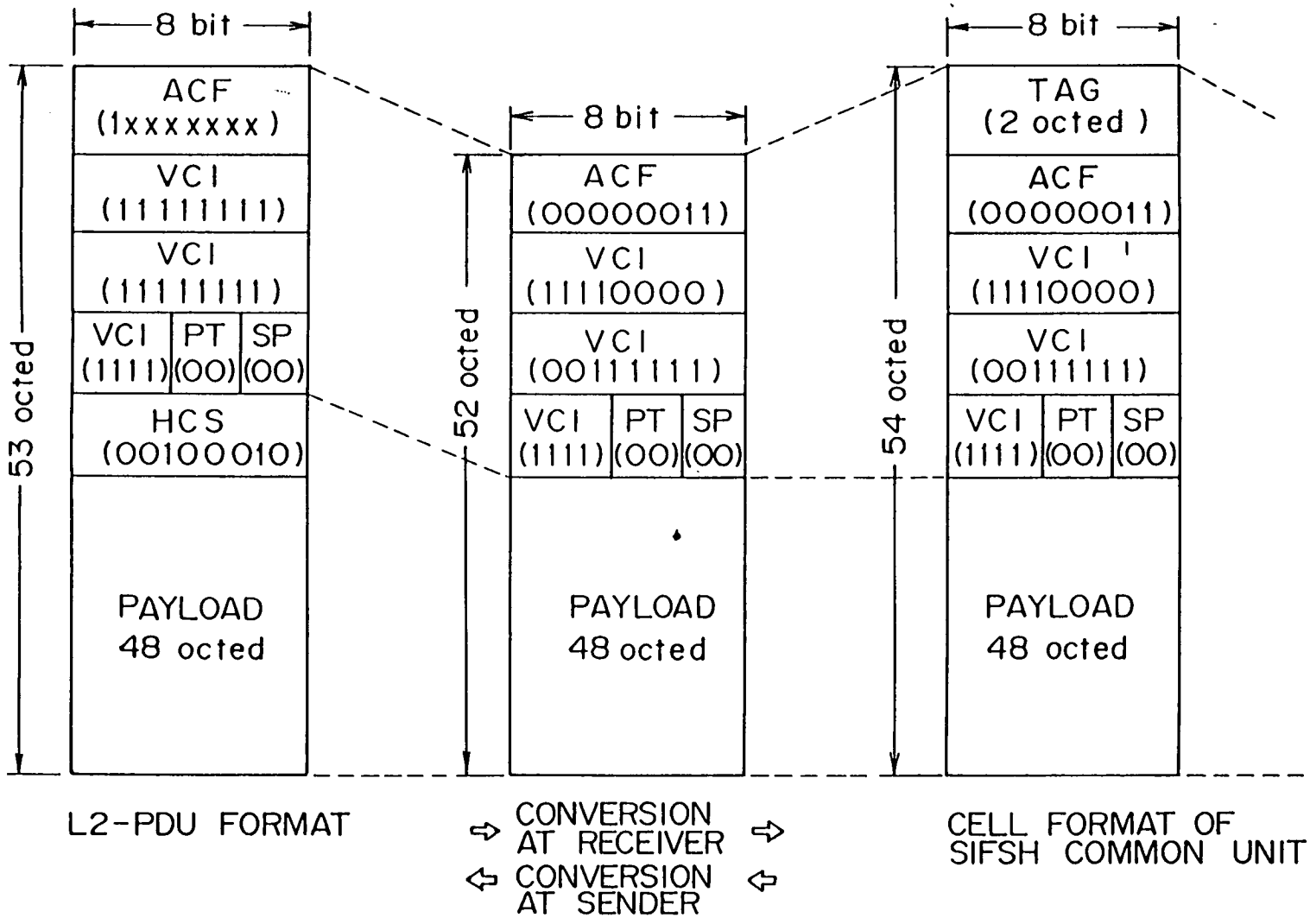
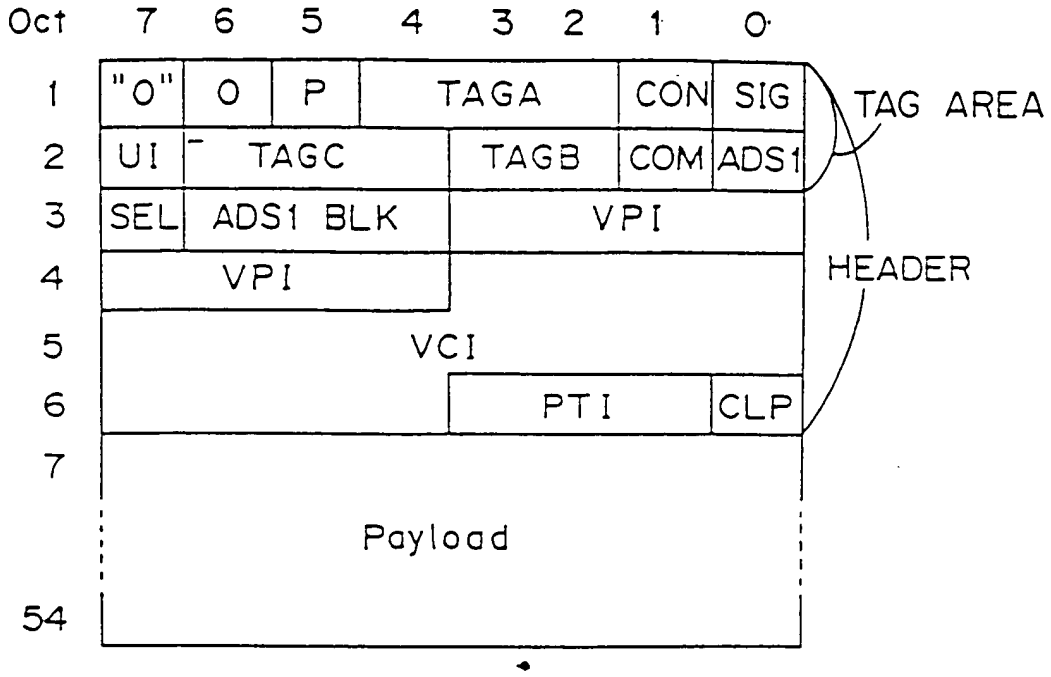


FIG. 55

IN CASE OF CONVERSION AT SENDER EFECTIVE ACF CELL IS "10000000"

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



O : ONE-TO-ONE COMMUNICATIONS MODE (NO COPY MODE)

O : INTERNAL TEST CELL INDICATOR (O: USER CELL, 1: INTERNAL CELL)

P : QUALITY INDICATOR

CON : PRIORITY CLASS INDICATOR AT CONGESTION

TAG A : 2.4 G 4 x 4 SELECTED

TAG B : 2.4 G ⇨ 600 M SELECTED

TAG C : 600 M ⇨ 156 M SELECTED

UL : DAISY-CHAIN HIGH ORDER / LOW ORDER

COM : SELECTING COMMON UNIT ACCOMMODATING 600 MHW

SIG : INTRA-STATION CELL IDENTIFICATION

ADS 1 BLK : MUX ⇨ DTC SELECTED ("000" FOR DS3-SMDS)

ADS 1 SEL : ADS 1 CARD SELECTED ("0" FOR DS3-SMDS)

FIG. 56

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

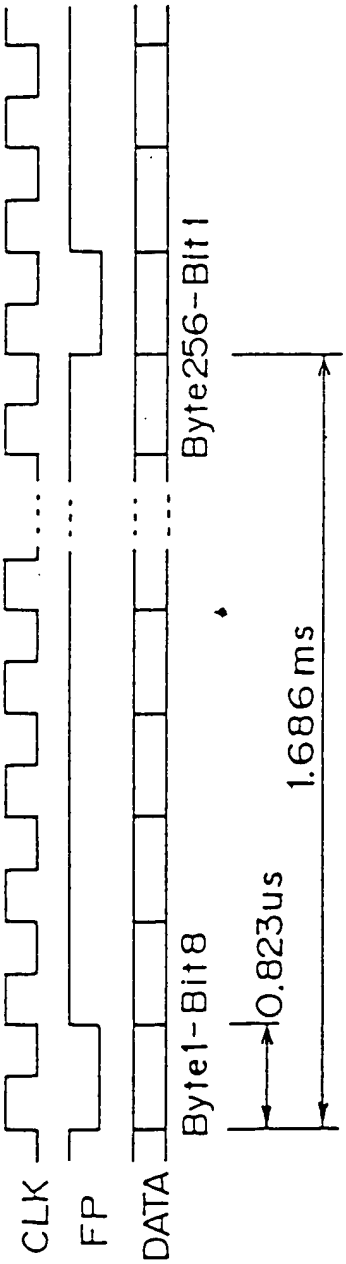


FIG. 57

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

BIT / BYTE	D7	D6	D5	D4	D3	D2	D1	D0
000	PLT1	PLT0						DTEN
001								
002								
003		SDFRST	μPRST					
004								
005		LOOP-2	LOOP-3	AISSND			O-LOOP	V-LOOP
006								
007	PF-CK	PF-CF	PF-PTY		PF-WDT		PTYRST	DS3DEC
008								
009								
010								
011								
012								
013								
014								
015								
016								
017								
018								
019								
020								
021								
. . .								
246								
. . .	UNUSED AREA							
256								

FIG. 58

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

ROW No	DATA	ABBR	MEANING	POLARITY	TYPE
000	0	DTEN	DATA ENABLE (SET IN SIFSH COMMON)	Neg	S/R
000	6	PLT0	STUCK MONITOR PILOT BIT (FIXED EARTH)	Neg	S/R
000	7	PLT1	STUCK MONITOR PILOT BIT (FIXED AT +5)	Neg	S/R
003	5	μPRST	μ-PROCESSOR RESET (FOR MAINTENANCE)	Neg	S/R
003	6	SDFRST	FAULT RESET	Neg	S/R
005	0	V-LOOP	SPECIFYING VPI/VCI CELL LOOPBACK	Pos	S/R
005	1	$\overline{0}$-LOOP	SPECIFYING "0"-BIT CELL LOOPBACK	Pos	S/R
005	4	AISSND	SPECIFYING TRANSMISSION OF AIS PATTERN IN DS3 LINE	Pos	S/R
005	5	LOOP-3	SPECIFYING LINE LOOPBACK	Pos	S/R
005	6	LOOP-2	SPECIFYING INTERNAL LOOPBACK (DS3 SMDS ALL LOOP)	Pos	S/R
007	0	DS3DEC	SPECIFYING DIAGNOSYS OF DS3-HARDWARE	Pos	S/R
007	1	PTYRST	PARITY ERROR RESET	Pos	S/R
007	4	PF-WDT	SPECIFYING PSEUDO-FAULT OF WATCH DOG TIMER	Pos	S/R
007	5	PF-PTY	SPECIFYING PSEUDO-FAULT OF PARITY ERROR	Pos	S/R
007	6	PF-CF	SPECIFYING PSEUDO-FAULT OF CELL FRAME PULSE DISCONNETION CHECKER	Pos Pos	S/R S/R
007	7	PF-CK	SPECIFYING PSEUDO-FAULT OF CELL DISCONNETION CHECKER	Pos	S/R

POLARITY : Neg : 0/1 = SIGNIFICANT/INSIGNIFICANT
; Pos : 0/1 = INSIGNIFICANT/SIGNIFICANT
; DOUBLE VALUES : SIGNIFICANT AT CHANGE POINT

FIG. 59

0 0 3 0 3 0 4 2 0 0 2

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

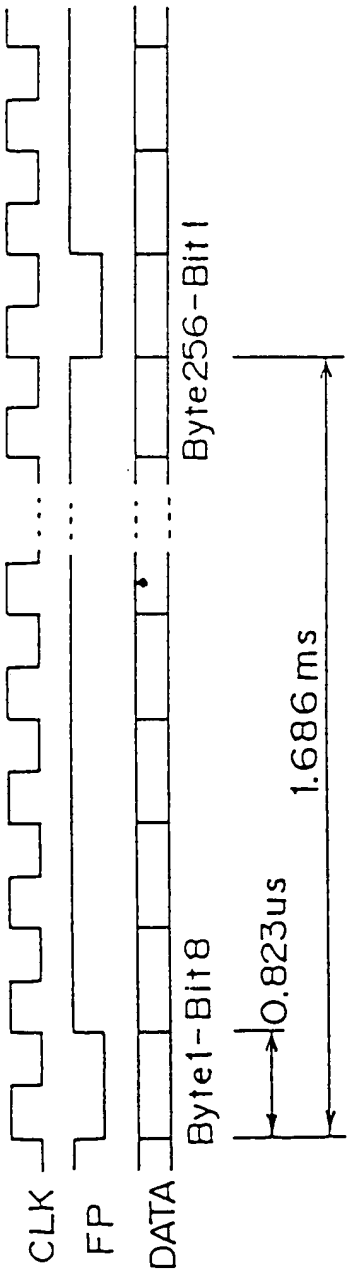


FIG. 60

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

BIT / BYTE	D7	D6	D5	D4	D3	D2	D1	D0
000	PLT1	PLT0	PWCB GROUP ID					
001	0	0	1	0	0	0	0	1
002	SYNCF0	PLTF0	SYNCF1	PLTF1	PE0	PE1		
003	—	SDFRST	μPRST					
004								
005		LOOP-2	LOOP-3	AISSND			O-LOOP	V-LOOP
006								
007	PF-CK	PF-CF	PF-PTY		PF-WDT		PTYRST	DS3DEC
008								
009								
010								
011								
012								
013								
014								
015	EC-AC1	EC-AC0	EC-TID	EC-TQH	EC-TSM			
016	FERR-1	FERR-2	L1ALM	TCAALM	CLOSAL			TIMALM
017			MPE			TSTEND	TSTIND	INS
018	DH19M0	DH19M1	DHCF0	DHCF1	DHDPT0	DHDPT1		
019	UHDPT	UH19M	EGPTY					
020			L1FLG	TCAFLG	CLFLG			
021								
031	DEC NG PHASE No.					DEC NG TST No.		
246								
UNUSED AREA								
255								

FIG. 61

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

ROW No	DATA	ABBREVIATION	MEANINGS	POLARITY	TYPE	RESET
000	6	PLT0	STUCK MONITOR PILOT BIT (EARTH FIXED)	Neg	—	—
000	7	PLT1	STUCK MONITOR PILOT BIT (+5V FIXED)	Neg	—	—
001	0-7	PWCB ID	LOADED PWCB ID	Pos	—	—
002	2	PE1	#1 SYSTEM INTERFACE UNIT REPRESENTATIVE ALARM	Neg	HELD	FRST1
002	3	PE0	#0 SYSTEM INTERFACE UNIT REPRESENTATIVE ALARM	Neg	HELD	FRST0
002	4	PLTF1	#1 PILOT SIGNAL ERROR	Neg	—	—
002	5	SYNCF1	#1 SYSTEM FCK SYNCHRONIZATION ERROR	Neg	—	—
002	6	PLTF0	#0 SYSTEM PILOT SIGNAL REEOR	Neg	—	—
002	7	SYNCF0	#1 SYSTEM FCK SYNCHRONIZATION ERROR	Neg	—	—
003	5	μPRST	μ-PROCESSER RESET	Pos	—	—
003	6	SDFRST	FAULT RESET	Pos	—	—
005	0	V-LOOP	SPECIFIED VPI/VCI CELL LOOPBACK INSTRUCTION	Pos	—	—
005	1	0-LOOP	"0"-BIT CELL LOOPBACK INSTRUCTION	Pos	—	—
005	4	AISSND	AIS PATTERN TRANSMIT INSTRUCTION TO DS3 LINE	Pos	—	—
005	5	LOOP-3	LINE LOOPBACK INSTRUCTION	Pos	—	—
005	6	LOOP-2	INTERNAL LOOPBACK INSTRUCTION	Pos	—	—
007	0	SD3DEC	DS3-SMDS HARDWARE DIAGNOSTIC INSTRUCTION	Pos	—	—
007	1	PTY-RS	PARITY ERROR RESET	Pos	—	—
007	3	PF-WDT	WATCH DOG TIME PSEUDO FAULT INSTRUCTION	Pos	—	—
007	5	PF-PTY	PARITY ERROR PSEUDO FAULT INSTRUCTION	Pos	—	—
007	6	PF-CF	CELL FRAME PULSE DISCONNECTION CHECKER PSEUDO FAULT INSTRUCTION	Pos	—	—
007	7	PF-CK	CLOCK DISCONNECTION CHECKER PSEUDO FAULT INSTRUCTION	Pos	—	—
015	3	EB-T5M	ECHO-BACK OF OTHER LINE MSD(TIMER 5-MINUTE)	ALTERNATION	—	—
015	4	EC-TQH	ECHO-BACK OF OTHER LINE MSD(TIMER QUARTER HOURLY)	ALTERNATION	—	—
015	5	EC-TID	ECHO-BACK OF OTHER LINE MSD(TIMER 1 DAY)	ALTERNATION	—	—

POLARITY:NEG:0/1=SIGNIFICANT/INSIGNIFICANT:POS:0/1
=INSIGNIFICANT/SIGNIFICANT:ALTERNATION:SIGNIFICANT WHEN CHANGE IS MADE

FIG. 62

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

ROW No	DATA	ABBREVIATION	MEANINGS	POLARITY	TYPE	RESET
015	6	EC-AC0	ECHO-BACK OF OTHER LINE MSD(ACT#0)	Neg	—	—
015	7	EC-AC1	ECHO-BACK OF OTHER LINE MSD(ACT#1)	Neg	—	—
016	0	TIMALMD	OTHER LINE TIMER INFORMATION NG OR CONDITION	Pos	NOT HELD	SDFRST
016	3	CLOSAL	156M →45M CONVERSION BUFFER CELL DISCARD START OR CONDITION	Pos	NOT HELD	—
016	4	TCAALM	DS3/PLCP TCA OR CONDITION	Pos	NOT HELD	—
016	5	L1ALM	DS3/PLCP ALARM OR CONDITION	Pos	NOT HELD	—
016	6	FEER-2	SD3-SMDS INF HARDWARE FAULT OR CONDITION	Pos	HELD	SDFRST
016	7	FEER-1	INTRA-STATION COMMUNCATION DISABLE DS3→MSDS INF HARDWARE FAULT	Pos	HELD	SDFRST
017	0	INS	DS3-SMDS INF MICROPROCESSOR INITIALIZATION TERMINATE	Pos	HELD	—
017	1	TSTIND	DS3-SMDS DIAGNOSTICS RESULT INDICATOR	Pos	HELD	SDFRST
017	2	TSTEND	DS3-SMDS DIAGNOSTICS COMPLETION INDICATOR	Pos	HELD	SDFRST
017	5	MPE	DS3-SMDS INF MICROPROCESSOR FAULT	Pos	HELD	μPRST
018	2	DHDPT1	#1 SYSTEM DOWNWARD PRIMARY SIGNAL DATA PARITY ERROR	Pos	HELD	FRST1
018	3	DHDPT0	#0 SYSTEM DOWNWARD PRIMARY SIGNAL DATA PARITY ERROR	Pos	HELD	FRST0
018	4	DHCF1	#1 SYSTEM CELL FRAME FAULT	Pos	HELD	FRST1
018	5	DHCF0	#0 SYSTEM CELL FRAME FAULT	Pos	HELD	FRST0
018	6	DM19M1	#1 SYSTEM DOWN 19M CLOCK FAULT	Pos	HELD	FRST1
018	7	DM19M0	#0 SYSTEM DOWN 19M CLOCK FAULT	Pos	HELD	FRST0
019	5	EGPTY	EGCLAD PARITY ERROR	Pos	HELD	SDFRST
019	6	UH19M	UP 19M CLOCK FAULT	Pos	HELD	SDFRST
019	7	UHDPT	UPWARD PRIMARY SIGNAL DATA PARITY DRROR	Pos	HELD	SDFRST
020	3	CLFLG	156M →45M CONVERSION BUFFER CELL DISCARD START CHANGE FLAG	ALTERNATION	NOT HELD	—
020	4	TCAFLG	DS3/PLCP TCA CHANGE FLAG	ALTERNATION	NOT HELD	—
020	5	LIFLG	DS3/PLCP ALARM CHANGE FLAG	ALTERNATION	NOT HELD	—
031	0-3	DEC NG TST No.	DS3-SMDS INF DIAGNOSTICS NG TST No. INDICATOR	Pos	HELD	—
031	4-7	DEC NG Ph No.	DS3-SMDS INF DIAGNOSTICS NG PH No. INDICATOR	Pos	HELD	—

POLARITY;NEG:0/1=SIGNIFICANT/INSIGNIFICANT;POS:0/1
=INSIGNIFICANT/SIGNIFICANT;ALTERNATION:SIGNIFICANT WHEN CHANGE IS MADE

FIG. 63

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

0636220

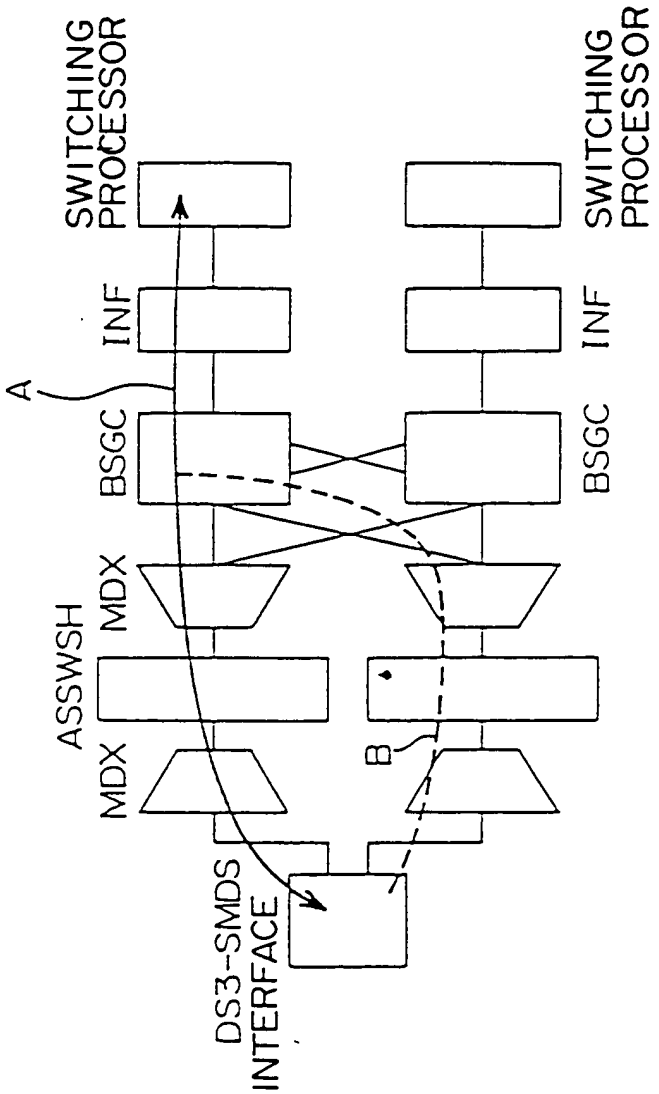


FIG. 64

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

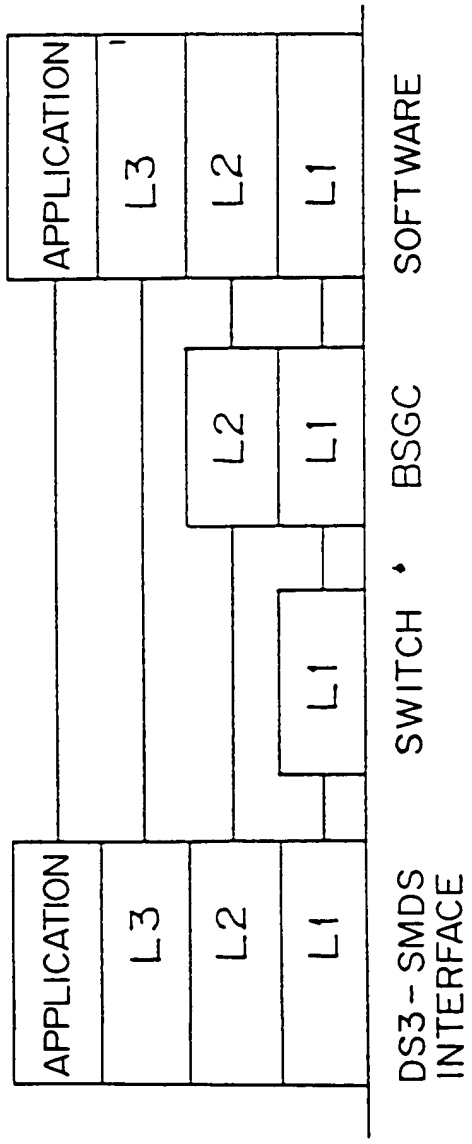
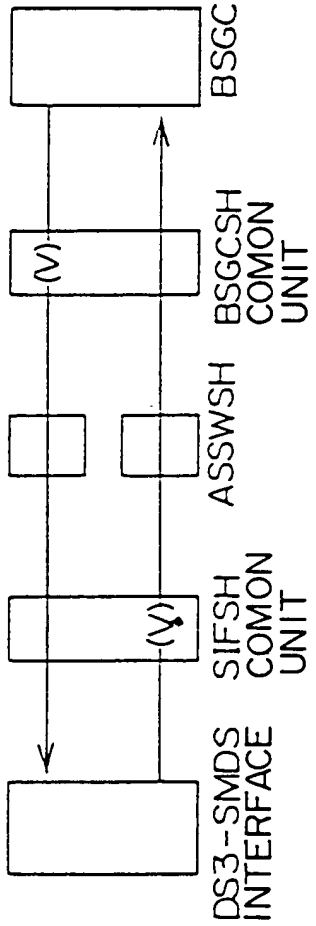


FIG. 65

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

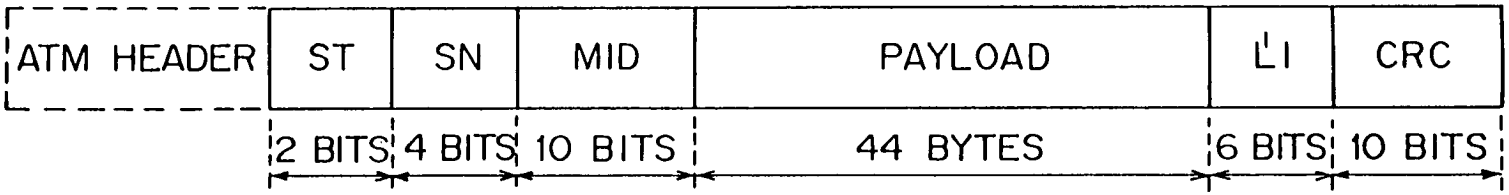


(V) : INDICATES POSITION OF VCC

FIG. 66

6692E0 EP2726O

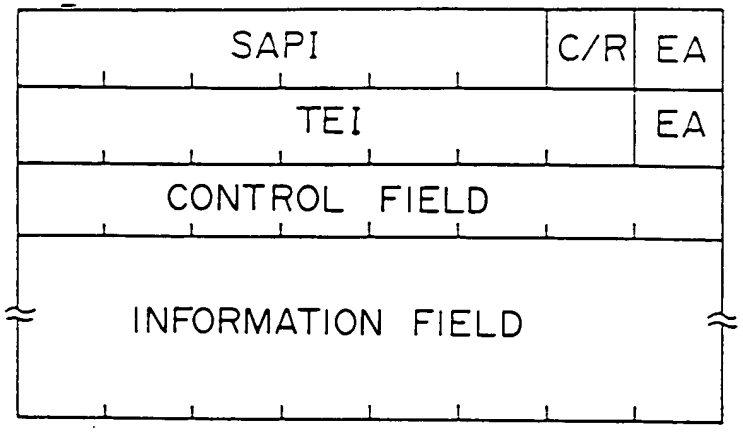
APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS



ST : SEGMENT TYPE (BOM, EOM, SSM, etc)
SN : SEQUENCE NUMBER
LI : PAYLOAD BYTE LENGTH INDICATOR
CRC : CRC (CRC-10 OF ST, SN, MID, AND PAYLOAD)
MID : d.c. FOR INTRA-STATION COMMUNICATIONS CELL

FIG. 67

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

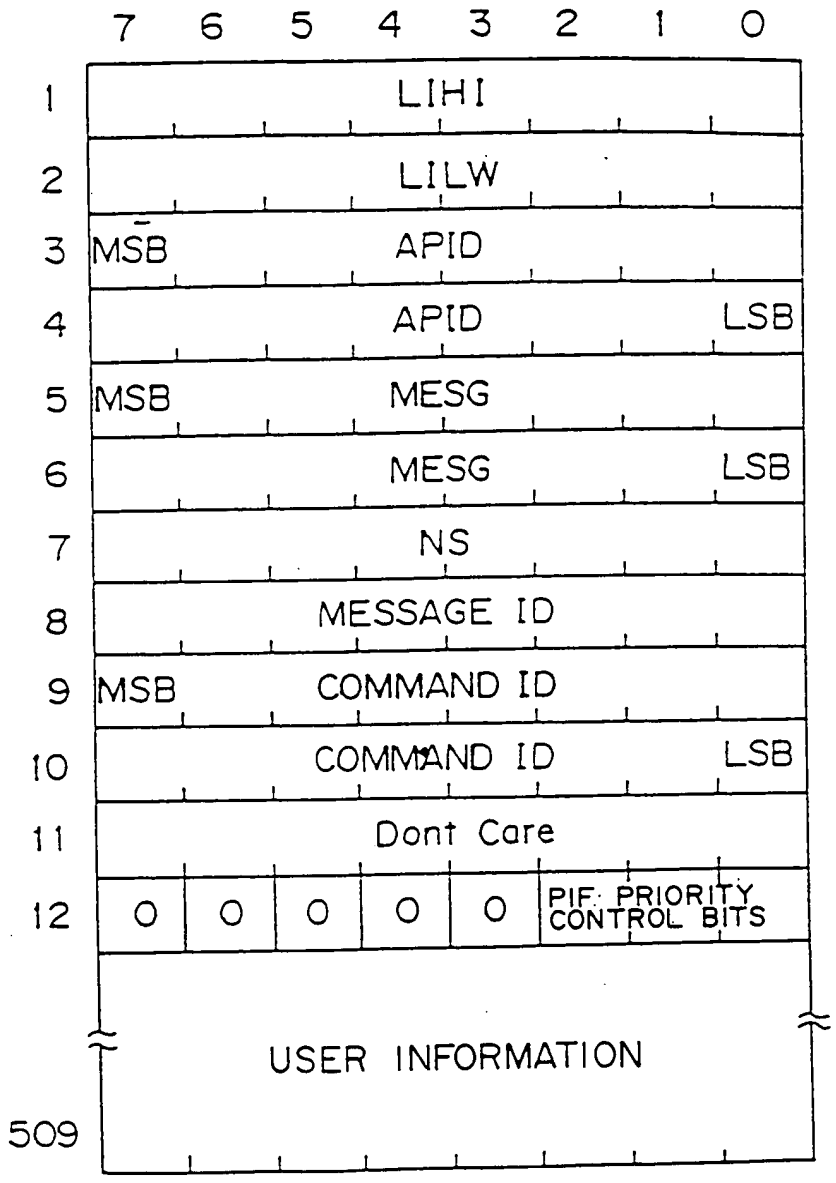


SAPI : ALL '0'
C/R : '1'
EA : EXTENSION ADDRESS (= 0)
TEI : ALL 0 IN SINF → BSGC DIRECTION PRIORITY LEVEL IS DEFINED FOR 3 LOWER BITS.
CONTROL FIELD : ID IS ASSIGNED TO SABM, UA, RR, AND DISC.

FIG. 68

0054248 05/05/2000

APPROVED BY DRAFTSMAN | O.G. FIG. CLASS | SUBCLASS



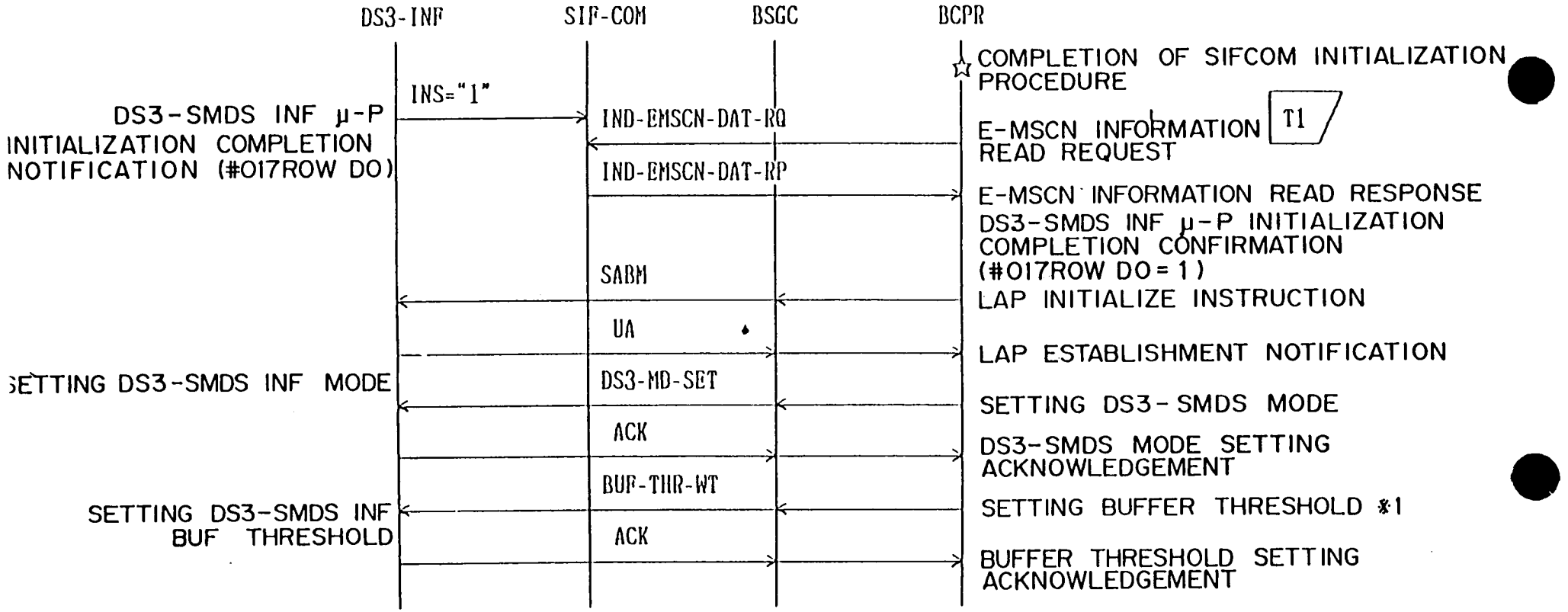
LIHI : INDICATES HIGHER HITS OF OCTETS ≤ LILW
LILW : INDICATES LOWER HITS OF OCTETS ≤ LILW
APID : INDICATES APPLICATION TO BE COMMUNICATED
MESG : IDENTIFIES MESSAGE IN APPLICATION
NS : BCPR → DEVICE SIGNAL
COMMAND ID : SOFTWARE SEQUENCE NUMBER

FIG. 69

6693E0 EP2772B0

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

(1) DS3-SMDS INTERFACE INITIALIZATION

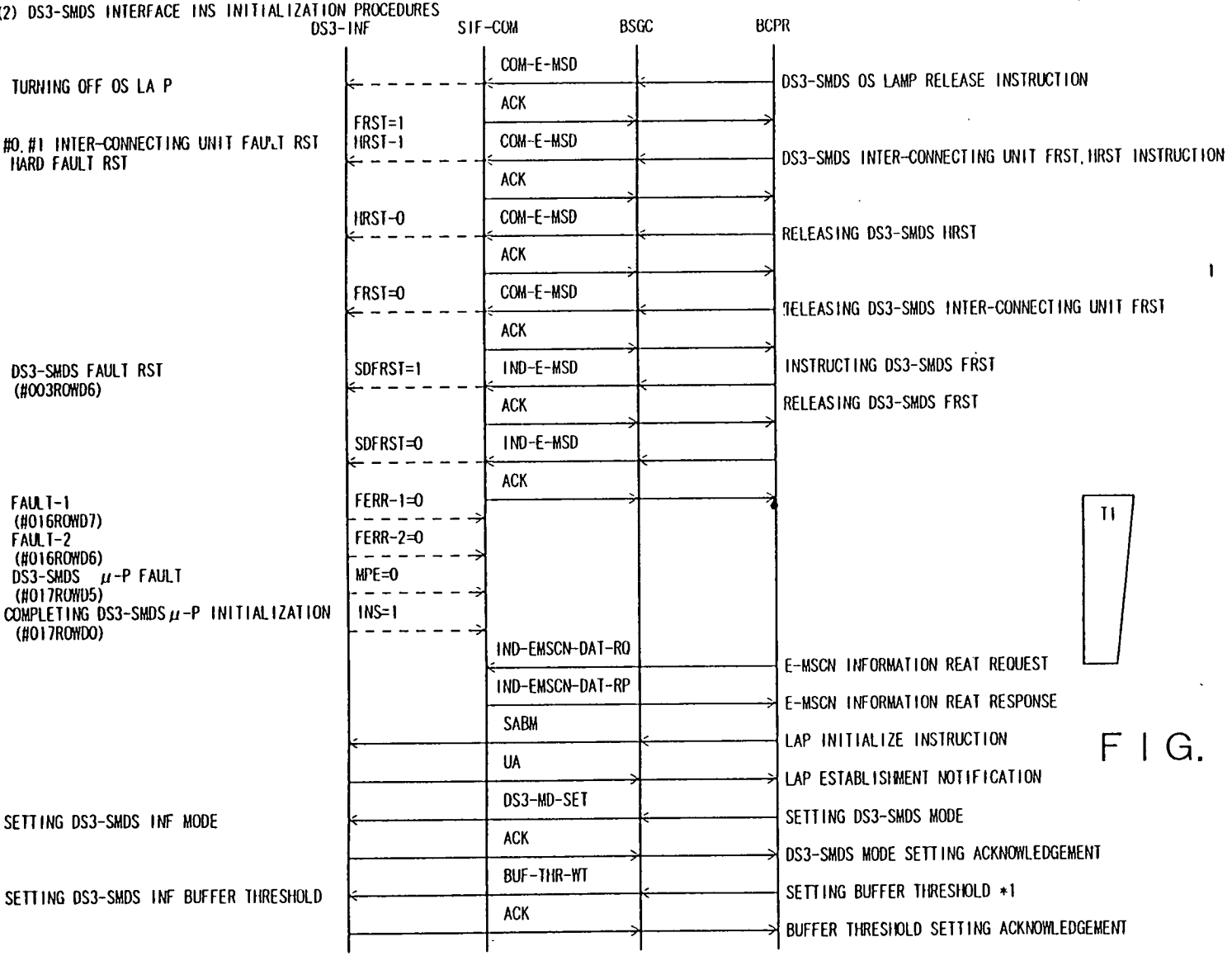


T1 : TIMEOUT AFTER 500 (MSEC) × 30 TIMES
※1 : SET WHEN NECESSARY

FIG. 70

APPROVED
DRAFTSMAN BY
O.G. FIG.
CLASS
SUBCLASS

(2) DS3-SMDS INTERFACE INS INITIALIZATION PROCEDURES



T1: TIMEOUT AFTER 500 (MSEC) X 30 TIMES
*1: SET WHEN NECESSARY

FIG. 71

(3) DS3-SMDS INTERFACE OUS PROCEDURE (MAINTENANCE BLOCK)

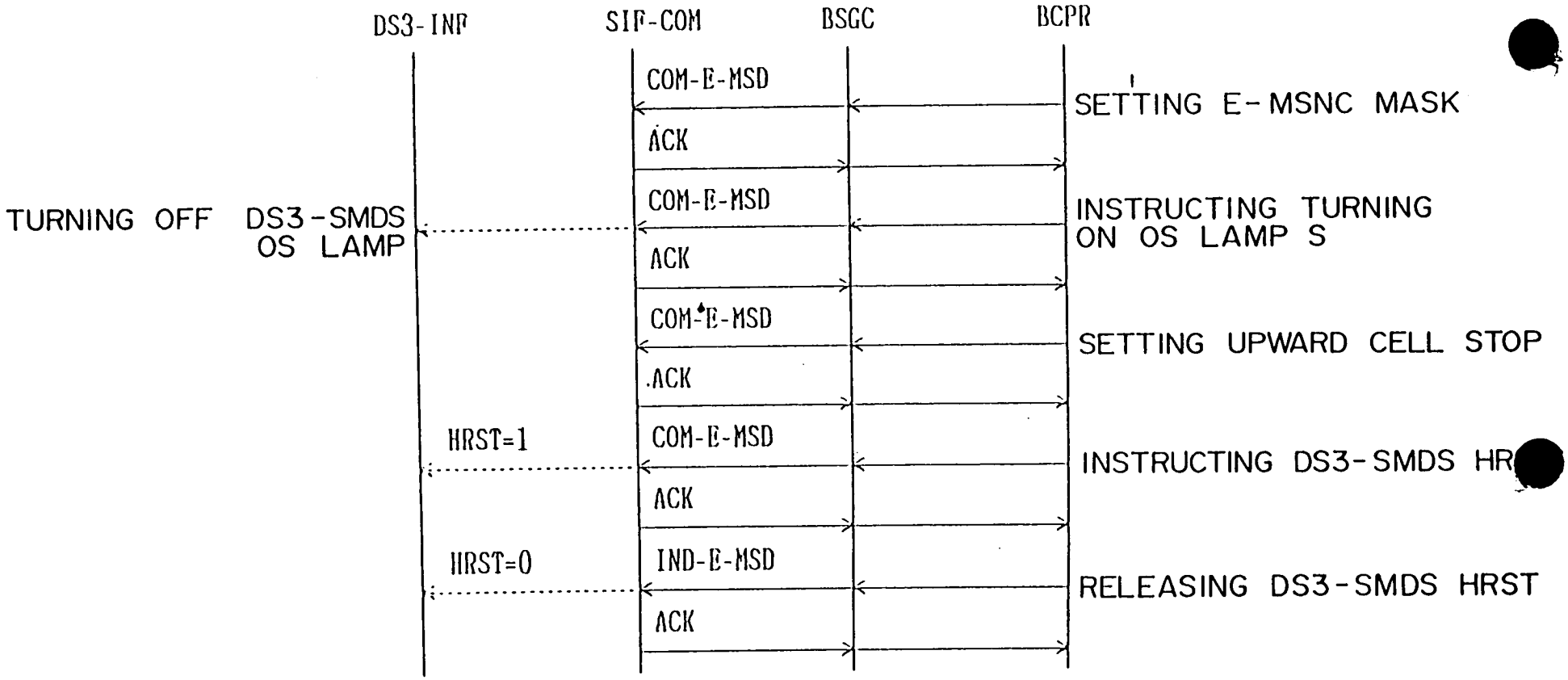


FIG. 72

(4) DS3-SMDS INTERFACE HARDWARE FAULT

① INTRA-STATION CONTROL COMMUNICATIONS ENABLE HARDWARE FAULT

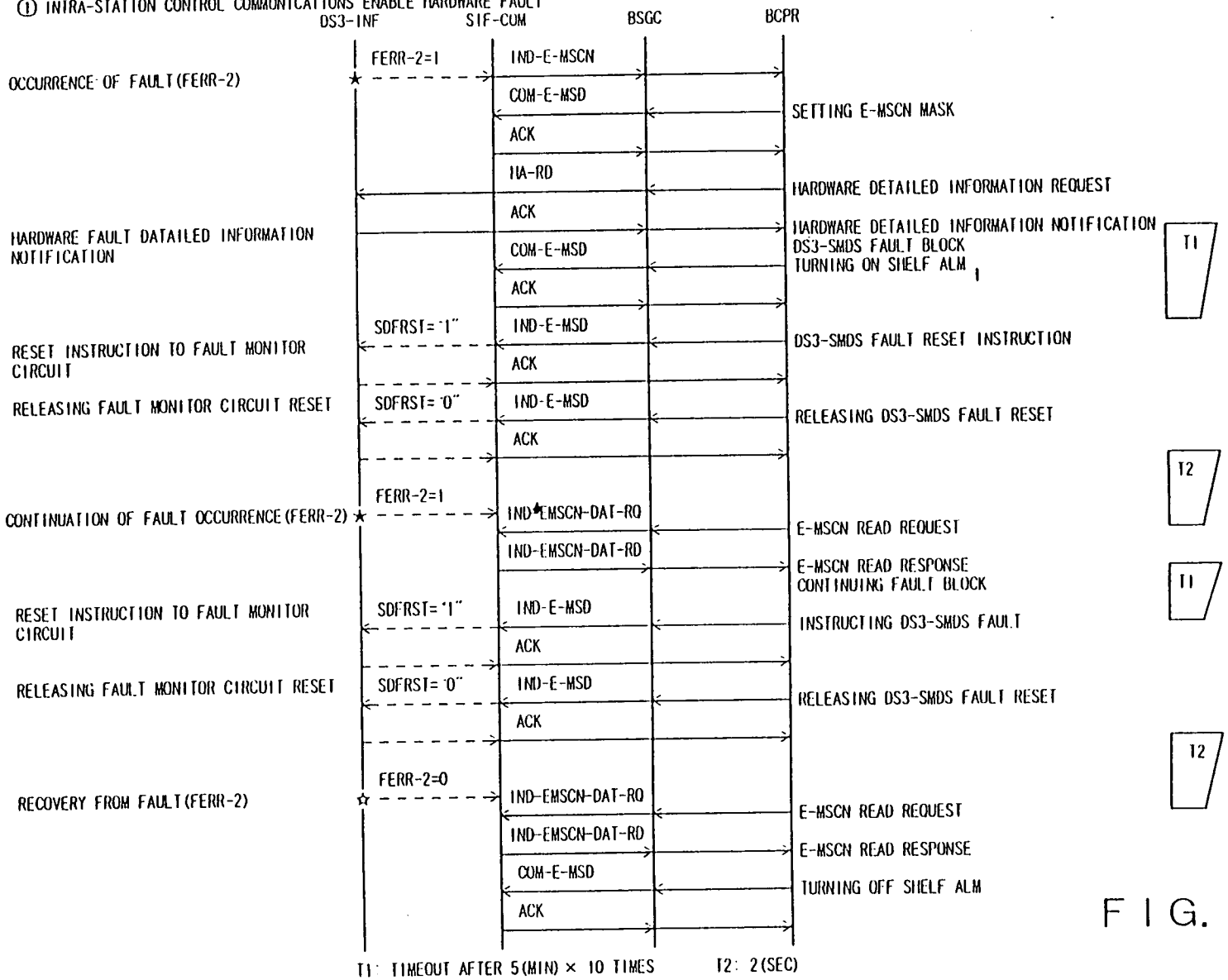


FIG. 73

6692E0 ET82260

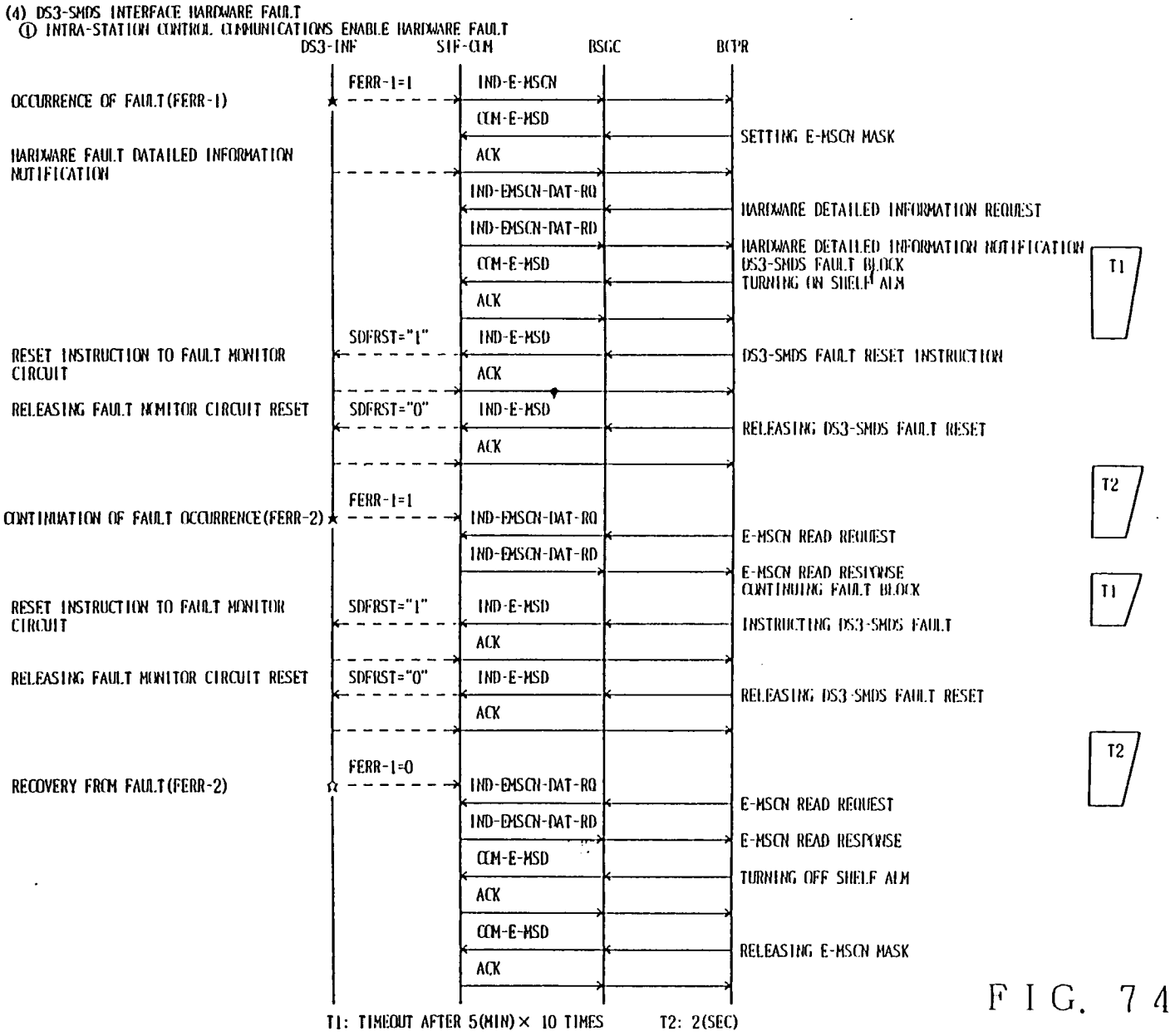


FIG. 74

(4) DS3-SMDS INTERFACE HARDWARE FAULT

③ μ PROCESSOR FAULT

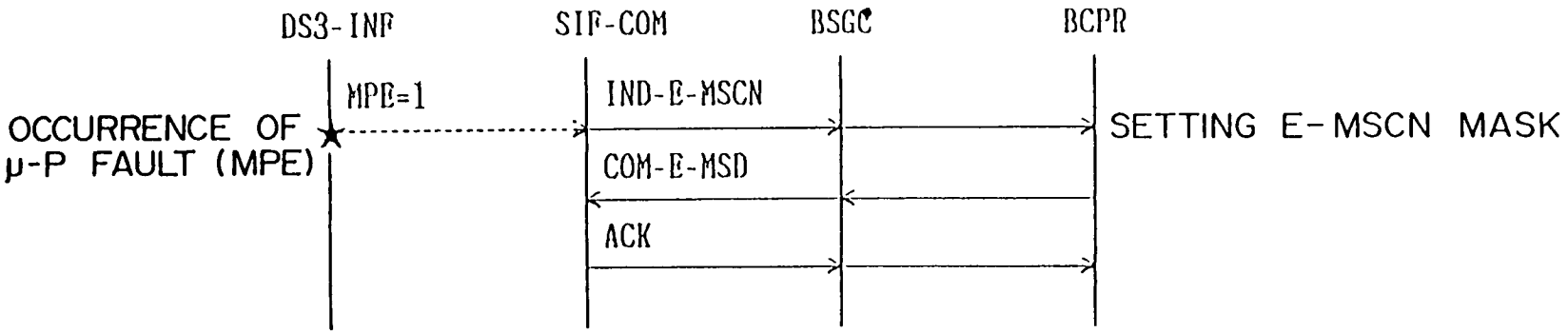


FIG. 75

(4) DS3-SMDS INTERFACE HARDWARE FAULT

④ SIFSH COMMON UNIT - DS3 SMDS IN' INTER-CONNECTING UNIT FAULT (ACT SYSTEM)

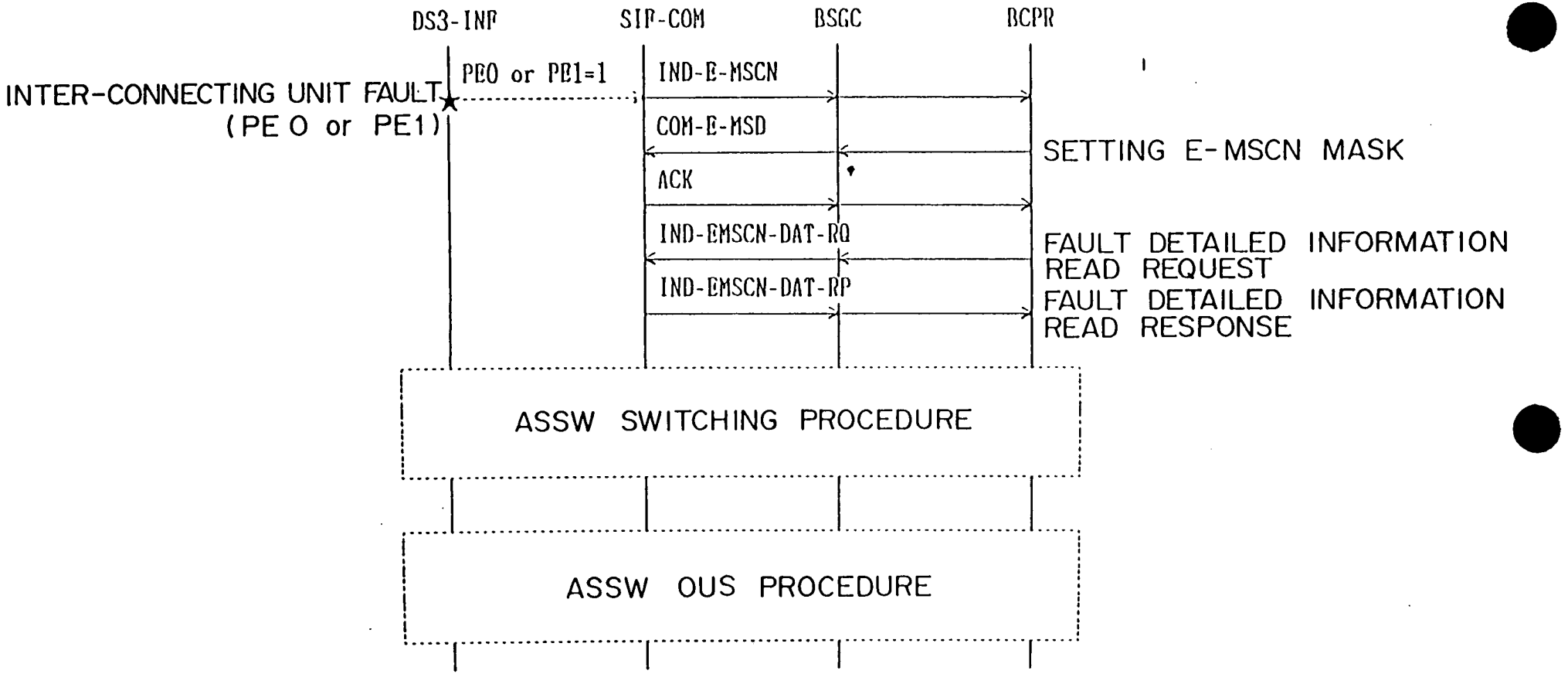


FIG. 76

(4) DS3-SMDS INTERFACE HARDWARE FAULT

⑤ SIFSH COMMON UNIT - DS3 SMDS IN INTER-CONNECTING UNIT FAULT (SBY SYSTEM)

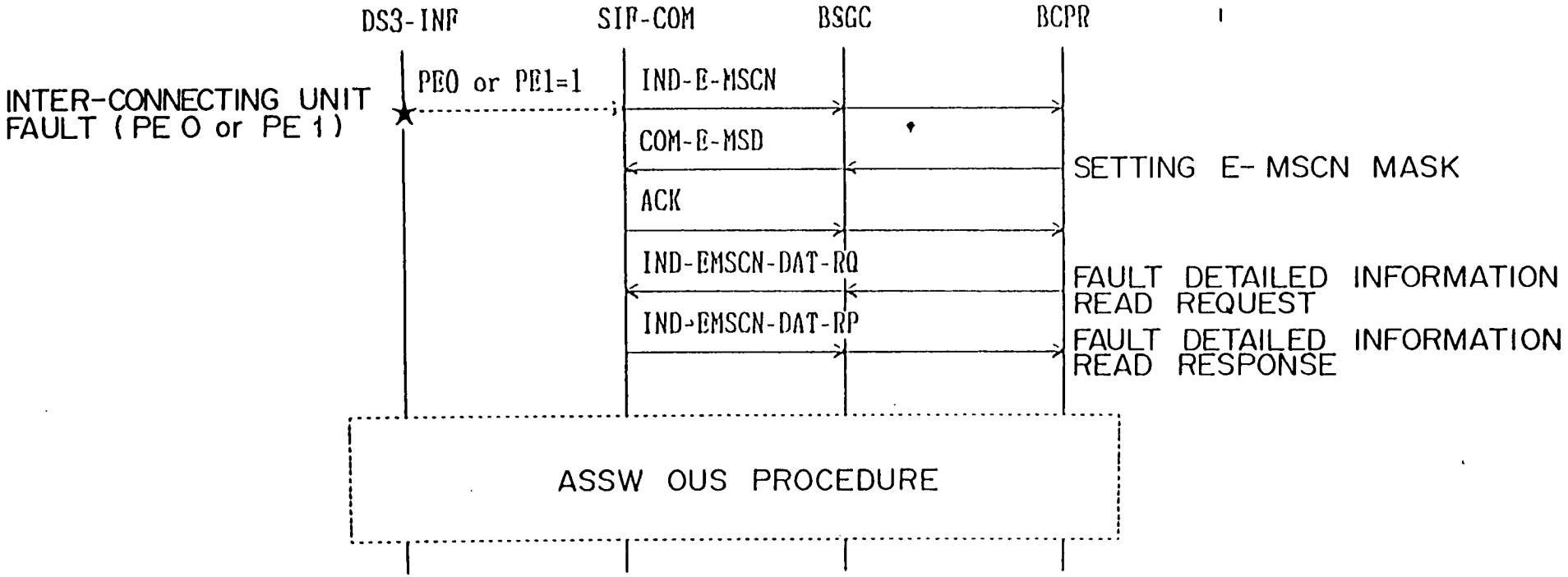


FIG. 77

(5) DS3/PLCP LAYER ALARM PROCESS

#016ROW D6

#020ROW D6

GENERATION OF DS3/PLCP ALARM (DS3RED=1)

SENDING DETAILED INFORMATION

GENERATION OF DS3/PLCP ALARM (DS3RED=0, DS3AIS=1)

SENDING DETAILED INFORMATION

RECOVERY OF DS3/PLCP ALARM (DS3AIS=0)

GENERATION OF DS3/PLCP ALARM (PYOF=1)

RECOVERY OF DS3/PLCP ALARM (PYOF=0)

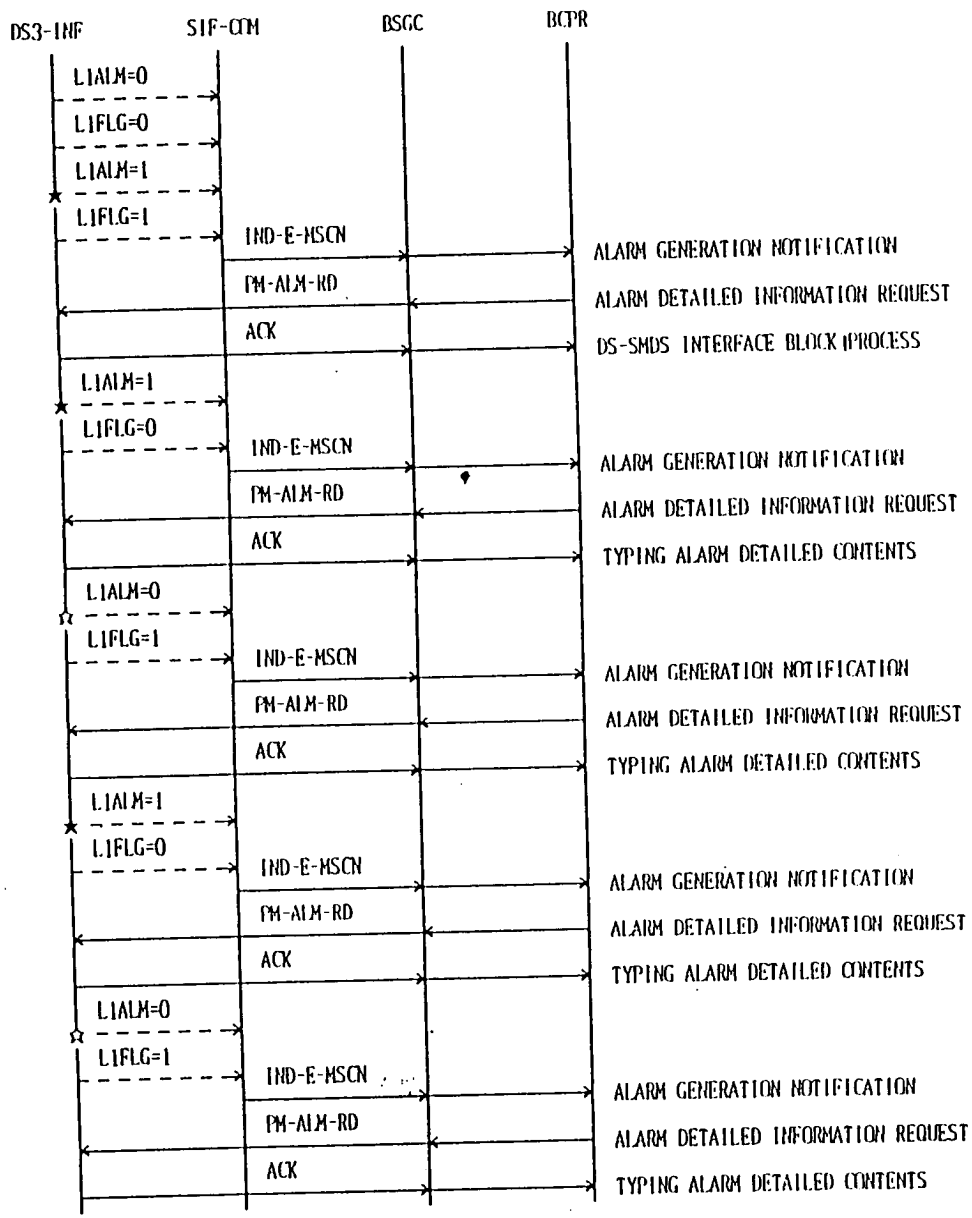


FIG. 78

(6) D/Q-TIMER NOTIFICATION AND PM DATA COLLECTION WHEN DS3/PLCP TCA OCCURS

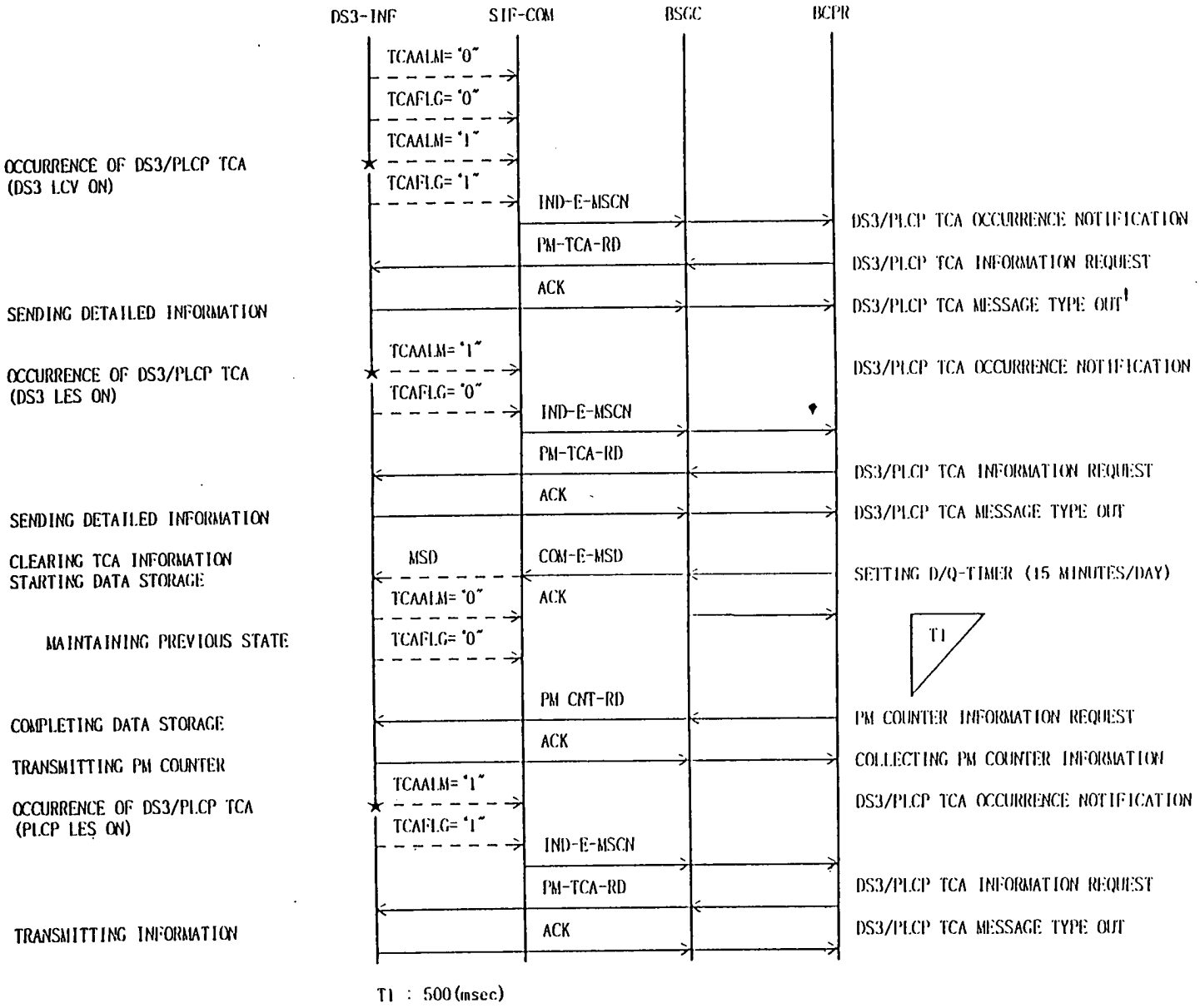
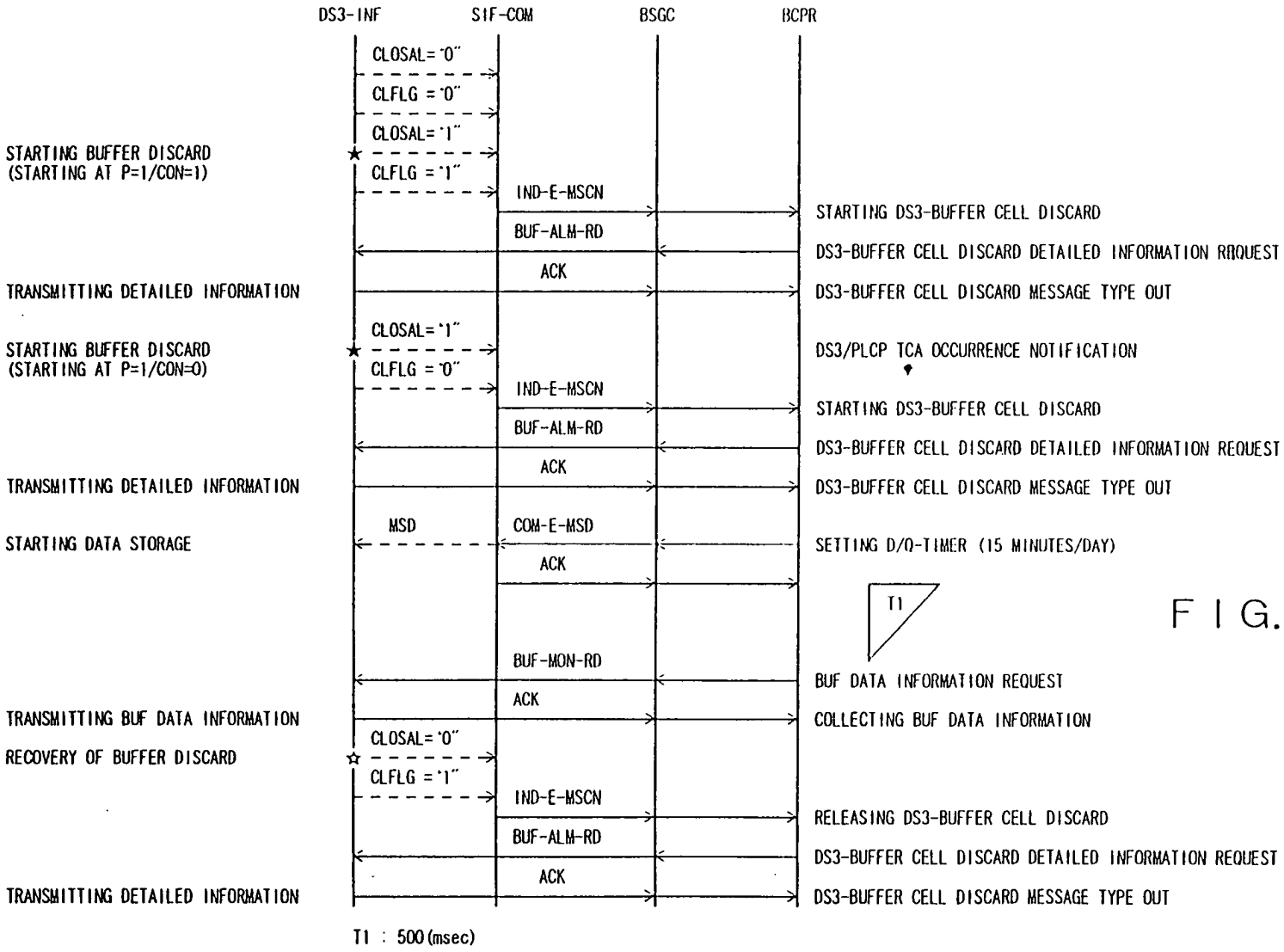


FIG. 79

(6) D/O-TIMER NOTIFICATION AND BUFFER DATA COLLECTION WHEN DS3/PLCP TCA OCCURS



T1 : 500(msec)

FIG. 80

(8) SETTING PVC PATH TEST SPECIAL NUMBER VPI / VCI CELL

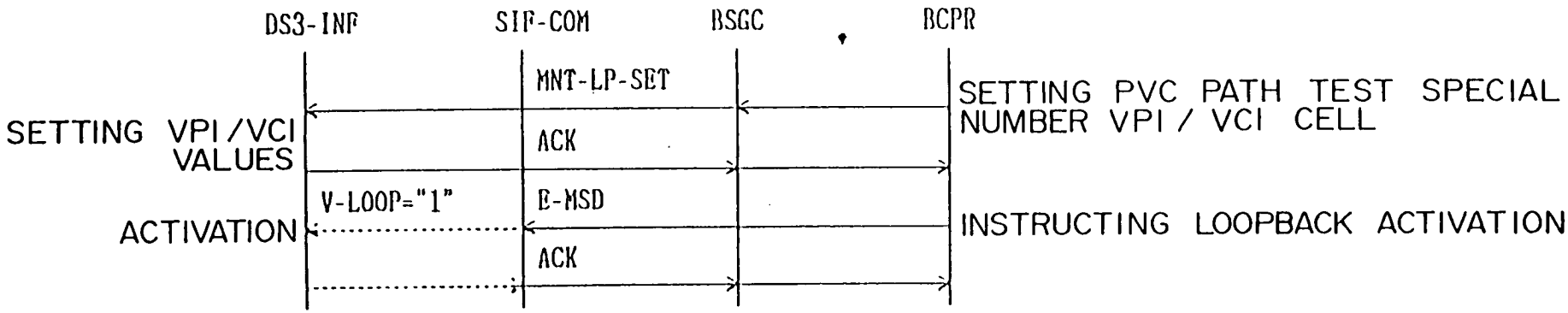


FIG. 81

6692607 EP2726

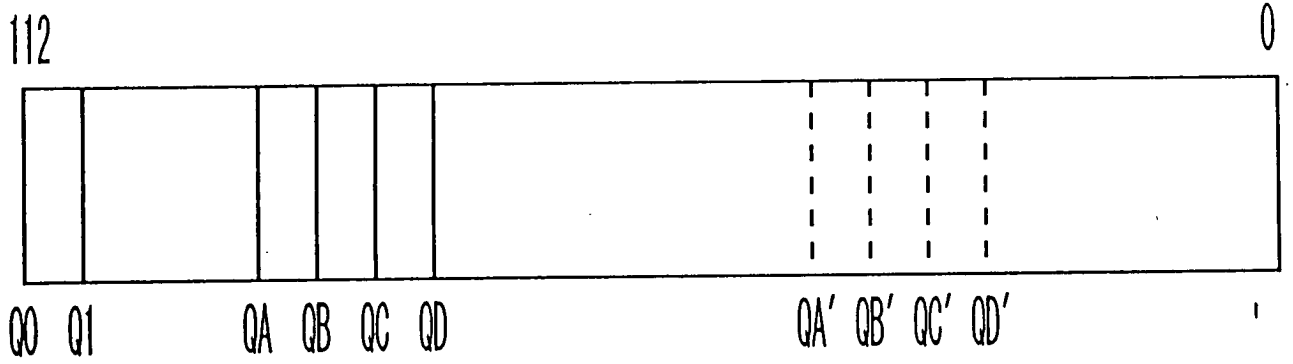


FIG. 82

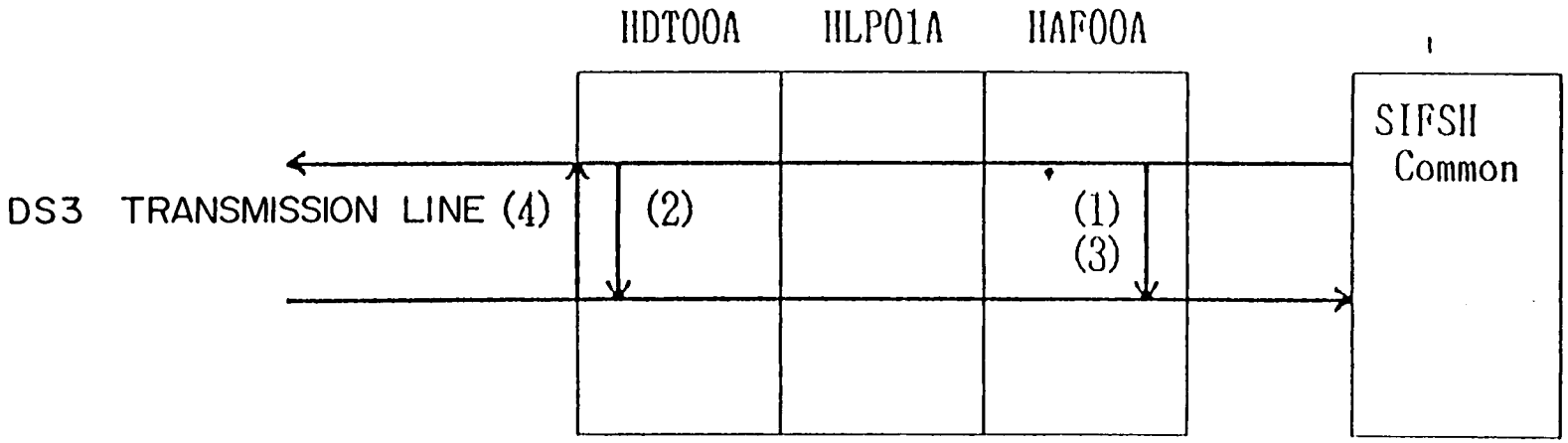

HDT00A
HLP01A
HAF00A
SIFSH
Common
DS3 TRANSMISSION LINE (4)
(2)
(1)
(3)

FIG. 83

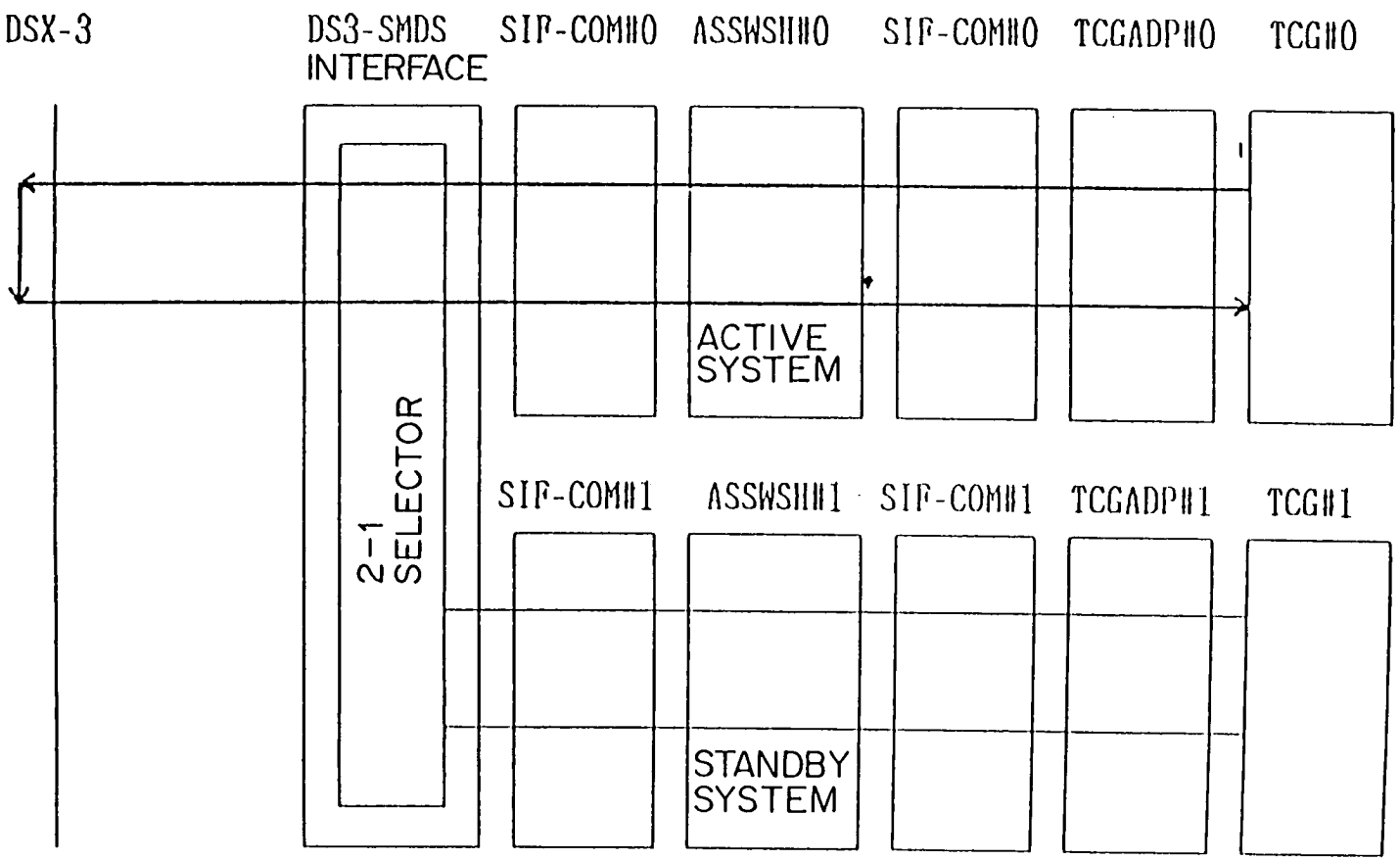

DSX-3
DS3-SMDS INTERFACE
SIF-COM#0
ASSWSI#0
SIF-COM#0
TCGADP#0
TCG#0
2-1 SELECTOR
ACTIVE SYSTEM
SIF-COM#1
ASSWSI#1
SIF-COM#1
TCGADP#1
TCG#1
STANDBY SYSTEM

FIG. 84

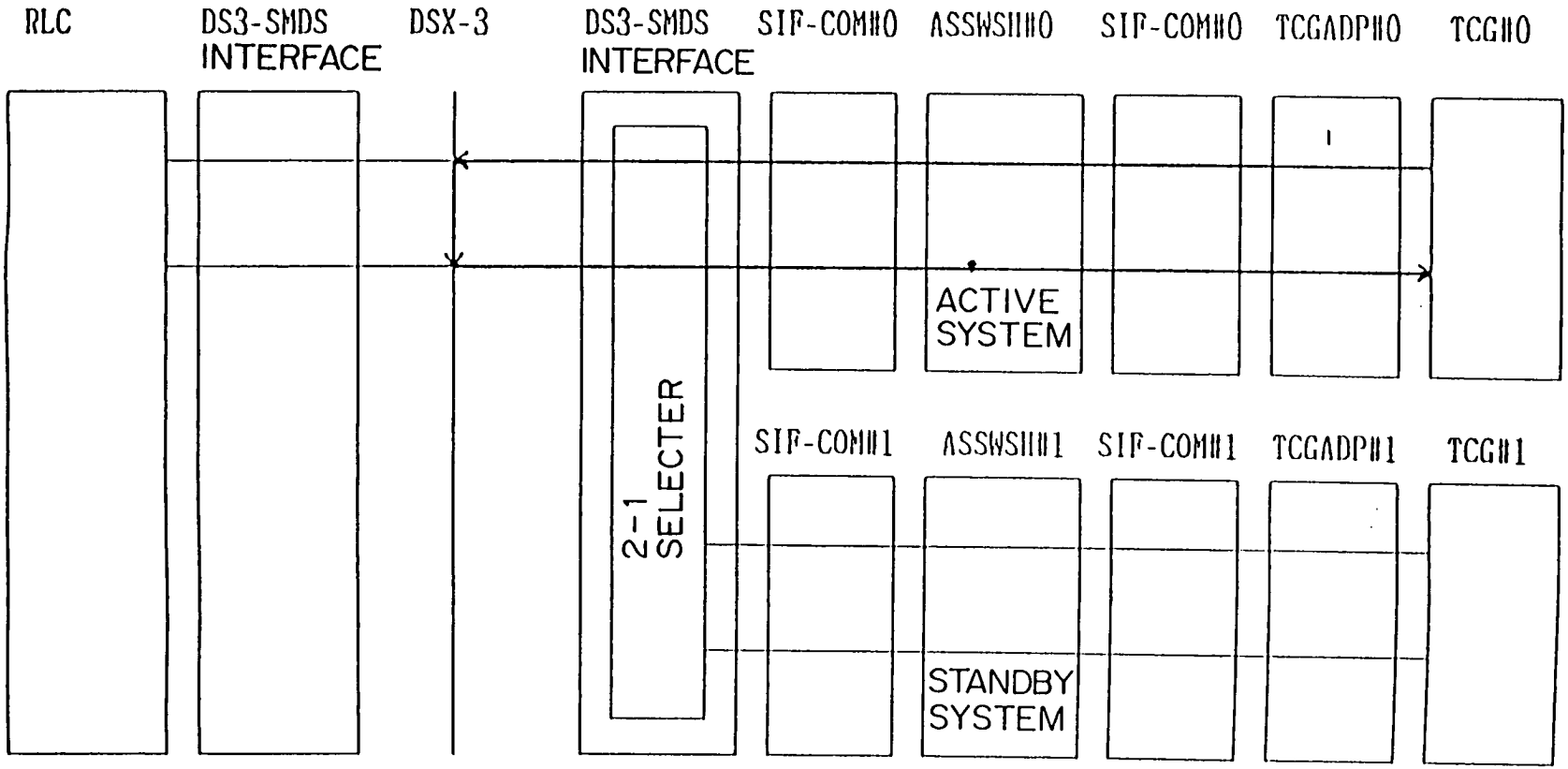

RLC
DS3-SMDS INTERFACE
DSX-3
DS3-SMDS INTERFACE
SIF-COM#0
ASSWSI#0
SIF-COM#0
TCGADP#0
TCG#0
2-1 SELECTER
ACTIVE SYSTEM
SIF-COM#1
ASSWSI#1
SIF-COM#1
TCGADP#1
TCG#1
STANDBY SYSTEM

FIG. 85

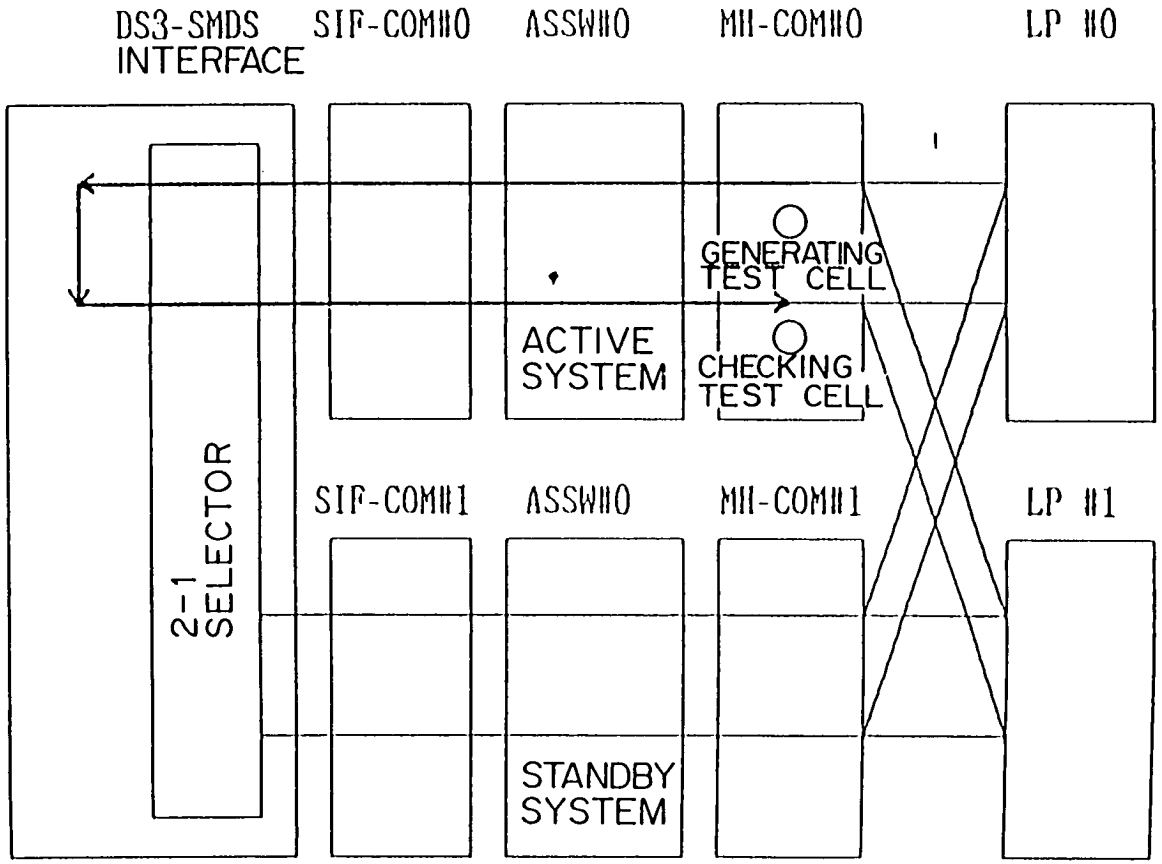
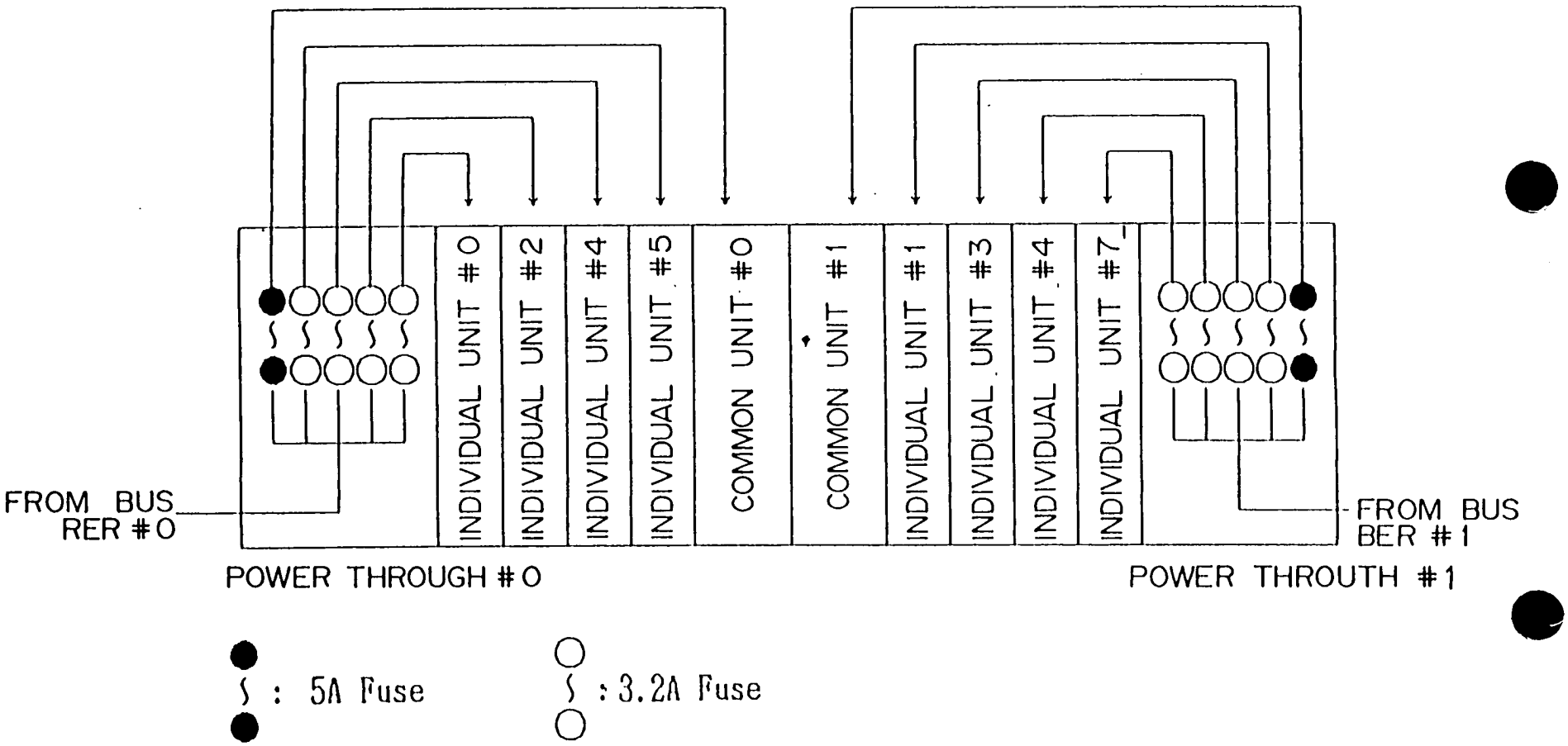

DS3-SMDS INTERFACE
SIF-COM#0
ASSW#0
MH-COM#0
LP #0
GENERATING TEST CELL
ACTIVE SYSTEM
CHECKING TEST CELL
2-1 SELECTOR
SIF-COM#1
ASSW#0
MH-COM#1
LP #1
STANDBY SYSTEM

FIG. 86



NOTE 1 : IN INDIVIDUAL UNIT PACKAGE, EVEN-NUMBER LINES ARE ACCOMMODATED IN LEFT HALF WHILE ODD-NUMBER LINES ARE ACCOMMODATED IN RIGHT HALF.

FIG. 87

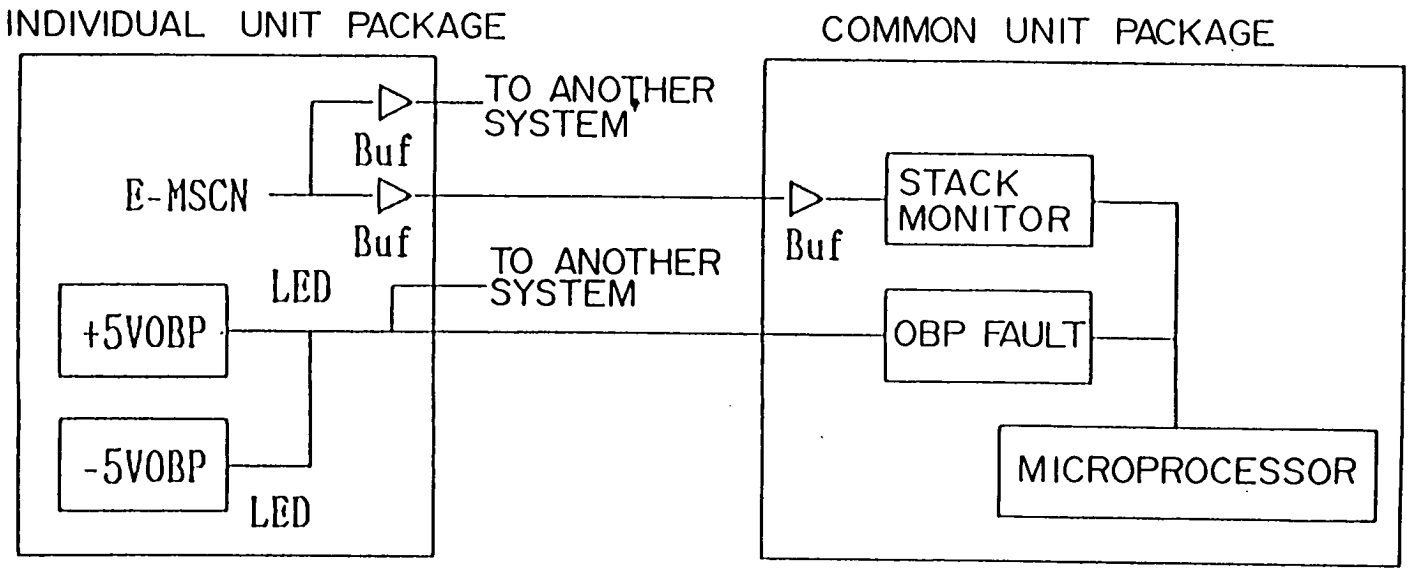

INDIVIDUAL UNIT PACKAGE
COMMON UNIT PACKAGE
TO ANOTHER SYSTEM
Buf
E-MSCN
Buf
Buf
STACK MONITOR
TO ANOTHER SYSTEM
LED
+5VOBP
OBP FAULT
-5VOBP
LED
MICROPROCESSOR

FIG. 88

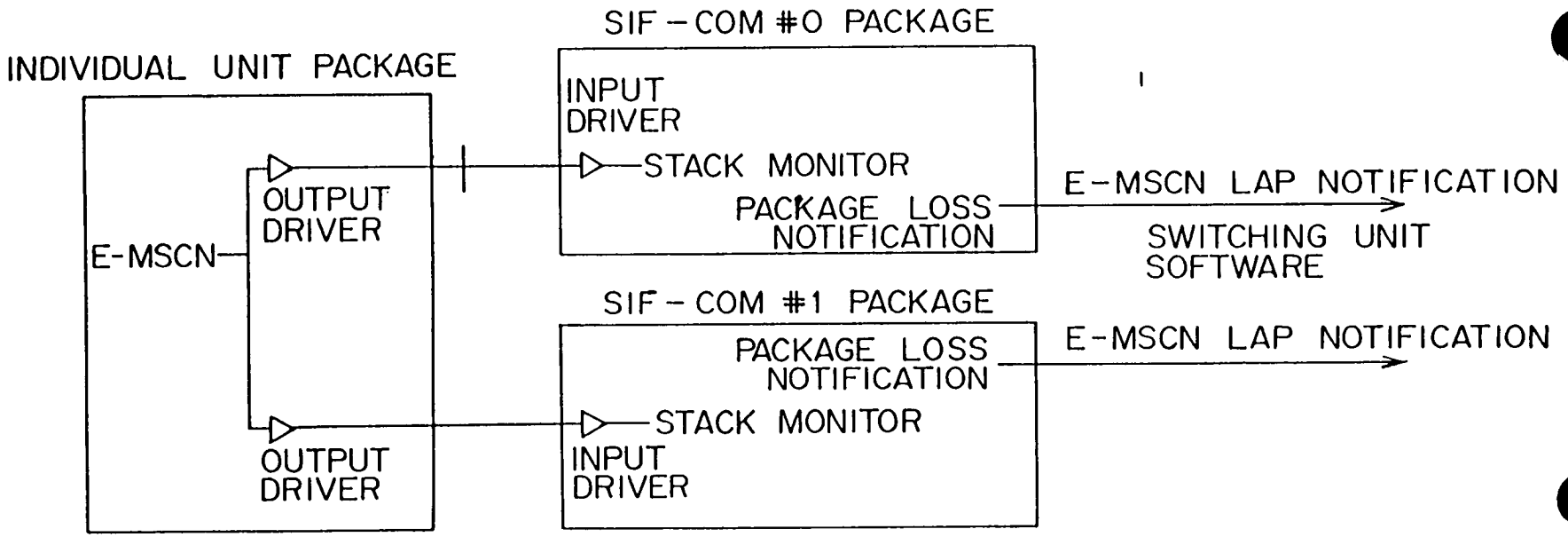

INDIVIDUAL UNIT PACKAGE
E-MSCN
OUTPUT DRIVER
OUTPUT DRIVER
SIF-COM #0 PACKAGE
INPUT DRIVER
STACK MONITOR
PACKAGE LOSS NOTIFICATION
E-MSCN LAP NOTIFICATION
SWITCHING UNIT SOFTWARE
SIF-COM #1 PACKAGE
PACKAGE LOSS NOTIFICATION
E-MSCN LAP NOTIFICATION
STACK MONITOR
INPUT DRIVER

FIG. 89

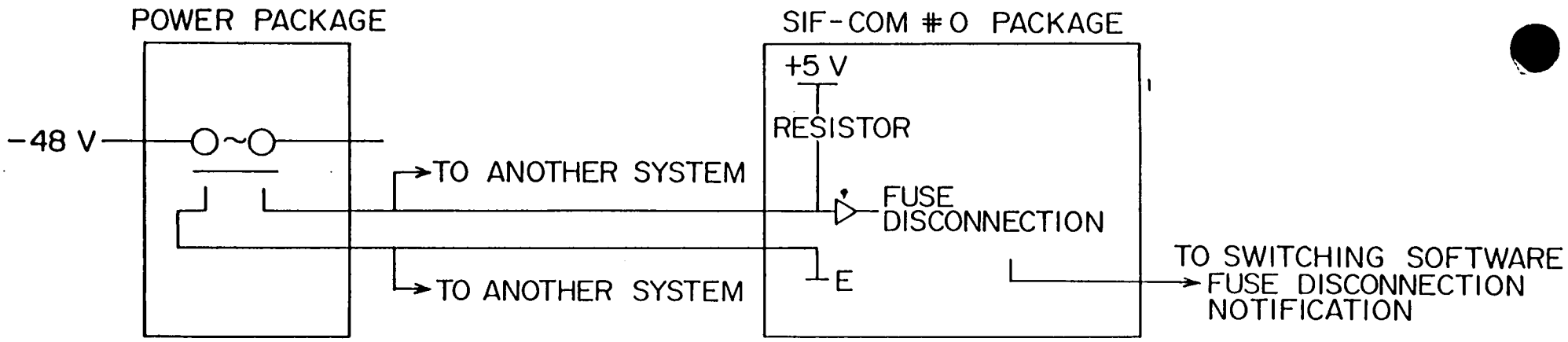

POWER PACKAGE
SIF-COM #0 PACKAGE
+5 V
RESISTOR
-48 V
TO ANOTHER SYSTEM
FUSE
DISCONNECTION
TO ANOTHER SYSTEM
E
TO SWITCHING SOFTWARE
FUSE DISCONNECTION
NOTIFICATION

FIG. 90

#0 SYSTEM ACT	#1 SYSTEM ACT	ACT STATE
0	0	MAINTAINING PREVIOUS STATE
1	0	#1 SYSTEM ACT
0	1	#0 SYSTEM ACT
1	1	MAINTAINING PREVIOUS STATUS

FIG. 91

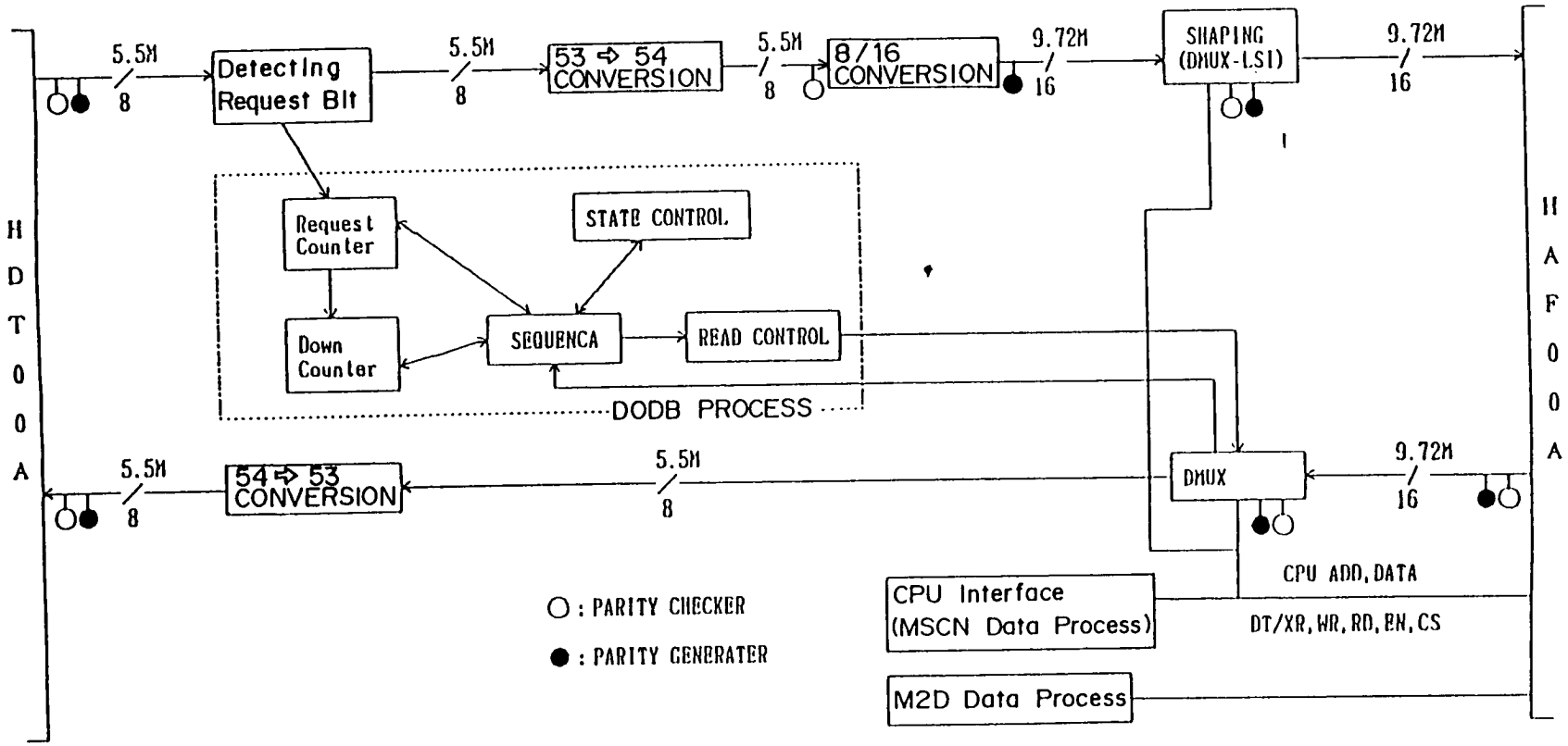

HDT00A
5.5M
8
Detecting Request Bit
5.5M
8
53 ⇨ 54 CONVERSION
5.5M
8
8/16 CONVERSION
9.72M
16
SHAPING (DMUX-LSI)
9.72M
16
HAF00A
Request Counter
STATE CONTROL
Down Counter
SEQUENCA
READ CONTROL
DODB PROCESS
5.5M
8
54 ⇨ 53 CONVERSION
5.5M
8
DMUX
9.72M
16
CPU ADD, DATA
DT/XR, WR, RD, EN, CS
CPU Interface (MSCN Data Process)
M2D Data Process
○ : PARITY CHECKER
● : PARITY GENERATER

FIG. 92

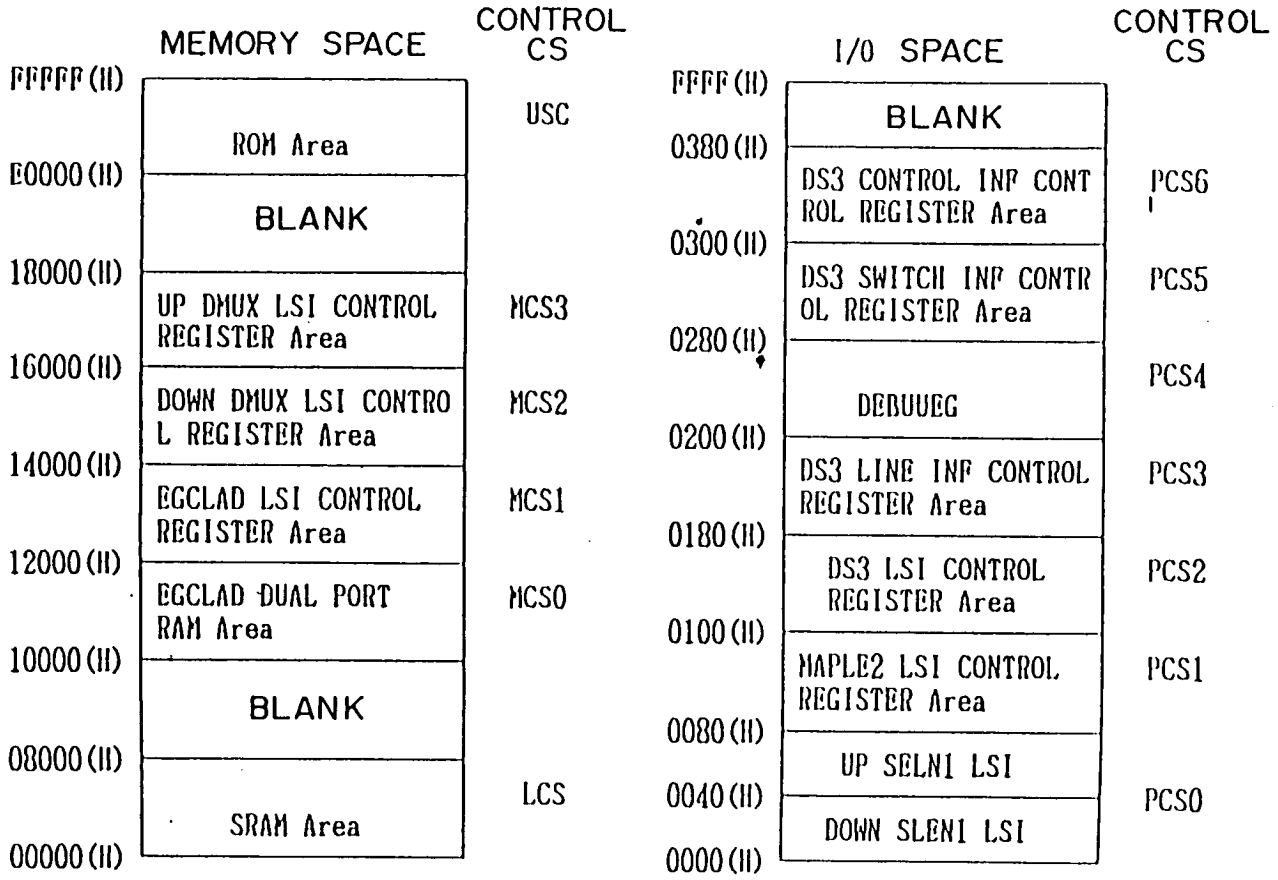

MEMORY SPACE
CONTROL CS
FFFFF(H)
ROM Area
USC
E0000(H)
BLANK
18000(H)
UP DMUX LSI CONTROL REGISTER Area
MCS3
16000(H)
DOWN DMUX LSI CONTROL REGISTER Area
MCS2
14000(H)
EGCLAD LSI CONTROL REGISTER Area
MCS1
12000(H)
EGCLAD DUAL PORT RAM Area
MCS0
10000(H)
BLANK
08000(H)
SRAM Area
LCS
00000(H)
I/O SPACE
CONTROL CS
FFFF(H)
BLANK
0380(H)
DS3 CONTROL INF CONTROL REGISTER Area
PCS6
0300(H)
DS3 SWITCH INF CONTROL REGISTER Area
PCS5
0280(H)
DEBUUEG
PCS4
0200(H)
DS3 LINE INF CONTROL REGISTER Area
PCS3
0180(H)
DS3 LSI CONTROL REGISTER Area
PCS2
0100(H)
MAPLE2 LSI CONTROL REGISTER Area
PCS1
0080(H)
UP SELN1 LSI
0040(H)
DOWN SLEN1 LSI
PCS0
0000(H)

FIG. 93

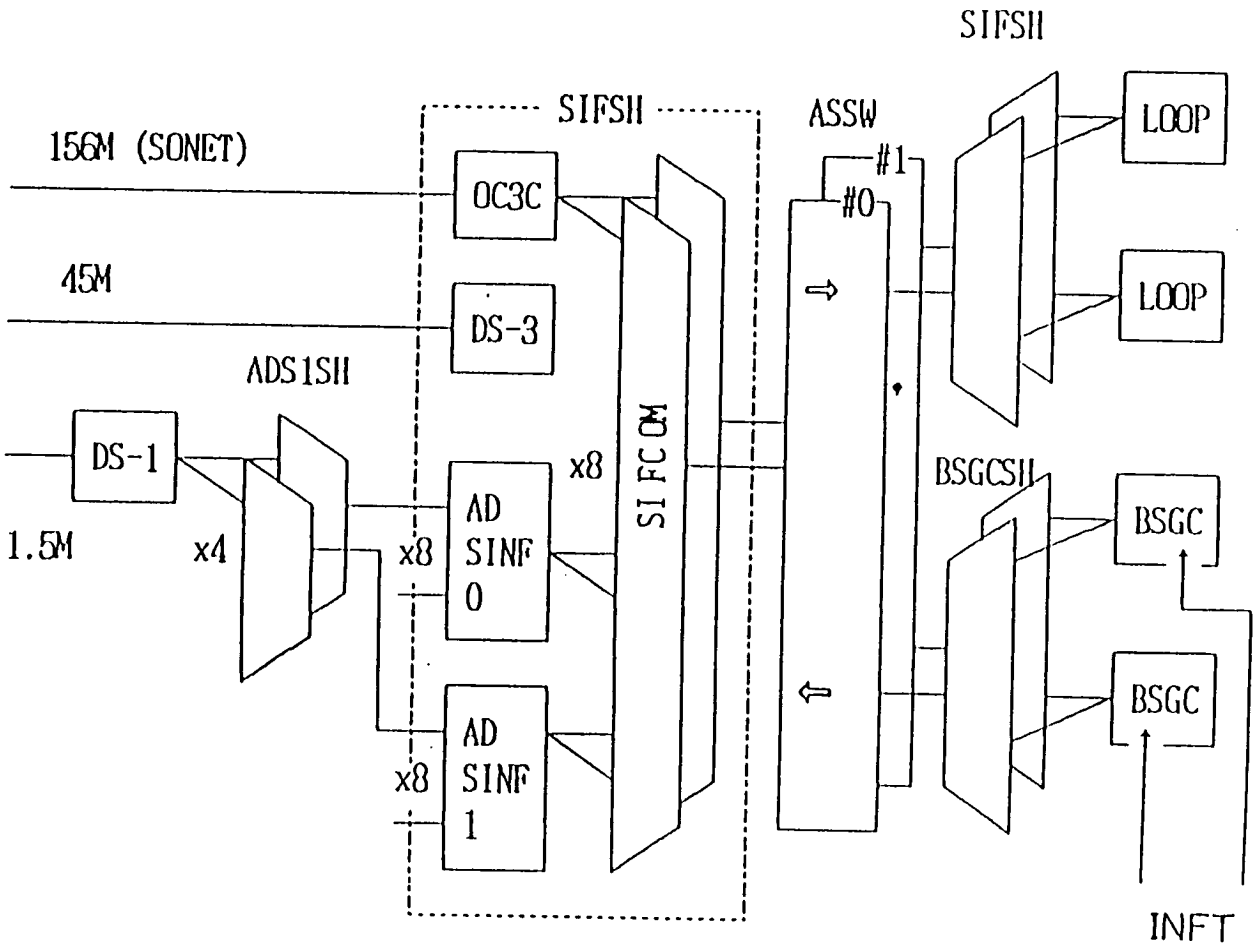

SIFSH
SIFSH
ASSW
#1
#0
156M (SONET)
OC3C
45M
DS-3
ADS1SH
DS-1
1.5M
x4
x8
AD SINF 0
x8
AD SINF 1
x8
SIFCOM
LOOP
LOOP
BSGCSH
BSGC
BSGC
INFT

FIG. 94

PKG NAME	FUNCTION
HSF01A	Shelf common controller
HMX04A	Shelf common up highway multiplexer
HMX05A	Shelf common down higway demultiplexer A
HMX06A	Shelf common down higway demultiplexer B
HPT01A	-48V power supply

FIG. 95

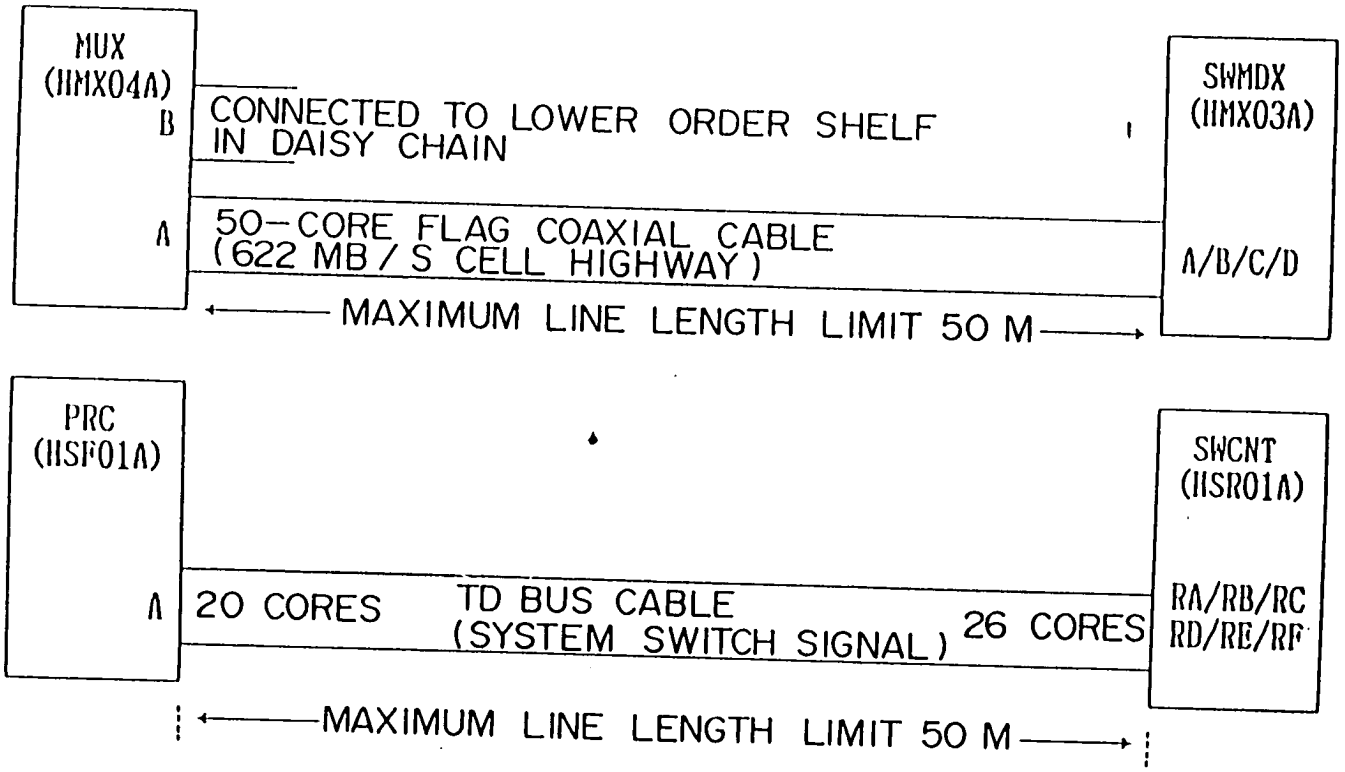

MUX
(HMX04A)
B
CONNECTED TO LOWER ORDER SHELF
IN DAISY CHAIN
A
50-CORE FLAG COAXIAL CABLE
(622 MB/S CELL HIGHWAY)
SWMDX
(HMX03A)
A/B/C/D
MAXIMUM LINE LENGTH LIMIT 50 M
PRC
(HSF01A)
A
20 CORES
TD BUS CABLE
(SYSTEM SWITCH SIGNAL)
26 CORES
SWCNT
(HSR01A)
RA/RB/RC
RD/RE/RF
MAXIMUM LINE LENGTH LIMIT 50 M

FIG. 96

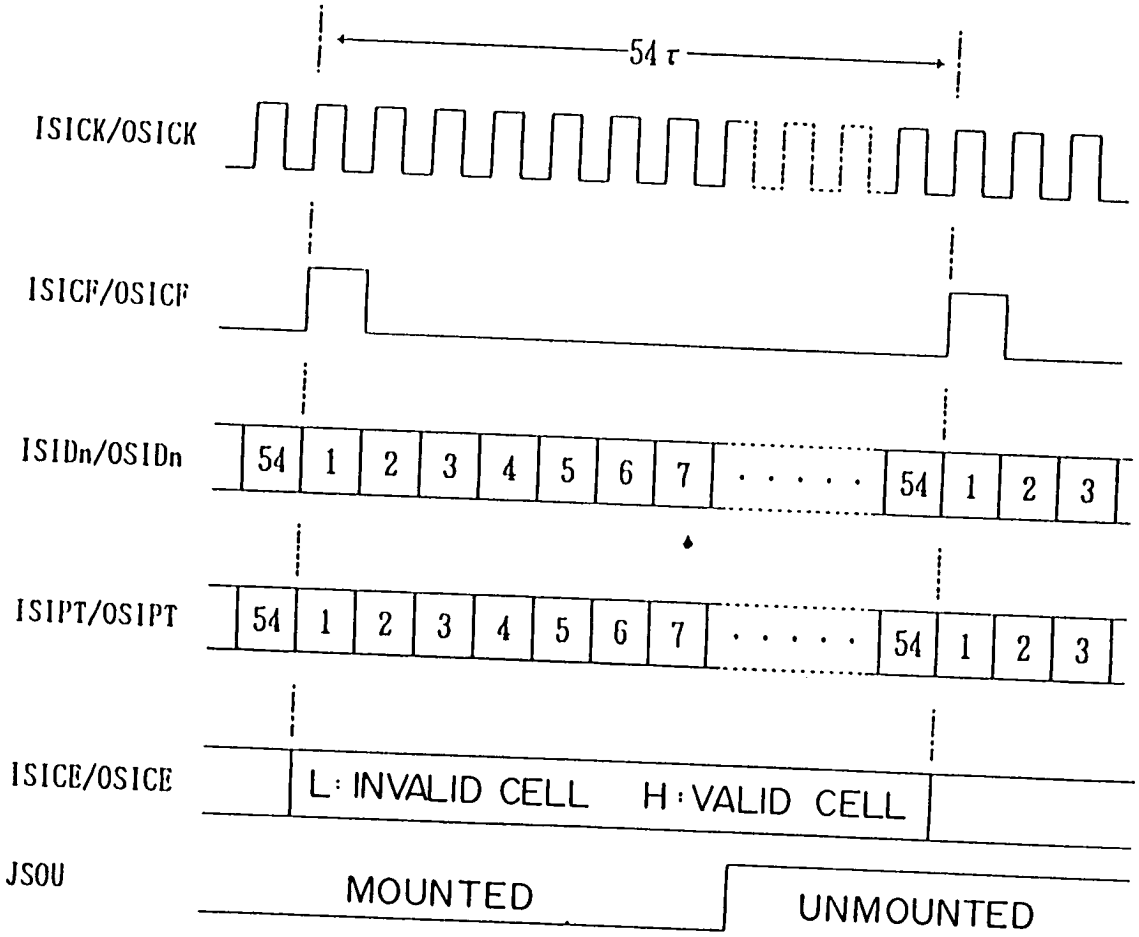
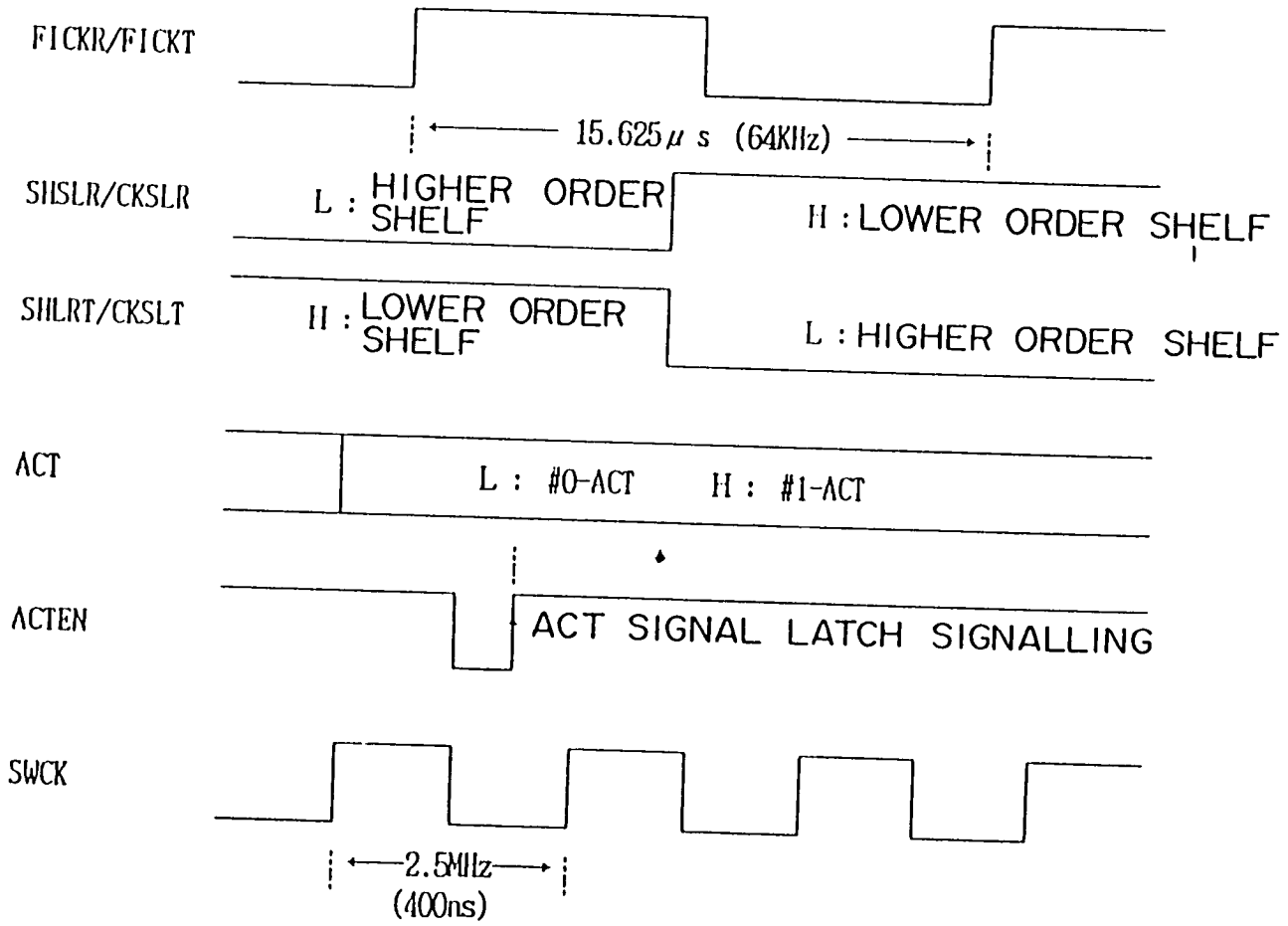

54 τ
ISICK/OSICK
ISICF/OSICF
ISIDn/OSIDn
54 1 2 3 4 5 6 7 · · · · · 54 1 2 3
ISIPT/OSIPT
54 1 2 3 4 5 6 7 · · · · · 54 1 2 3
ISICE/OSICE
L: INVALID CELL H: VALID CELL
JSOU
MOUNTED
UNMOUNTED

FIG. 97



ALM/IPLL/FCD0/FCD1 : CONSTANTLY H

FIG. 98

SYSTEM SELECT SIGNAL		SIFSH-A ACTIVE SYSTEM
SWITCH SELECT INDICATOR IN PRESENT SYSTEM	SWITCH SELECT INDICATOR IN OTHER SYSTEMS	
SELECTING SYSTEM 0	SELECTING SYSTEM 0	SYSTEM 0
SELECTING SYSTEM 1	SELECTING SYSTEM 1	SYSTEM 0
SELECTING SYSTEM 0	SELECTING SYSTEM 1	MAINTAINING OLD SYSTEM
SELECTING SYSTEM 1	SELECTING SYSTEM 0	MAINTAINING OLD SYSTEM

FIG. 99

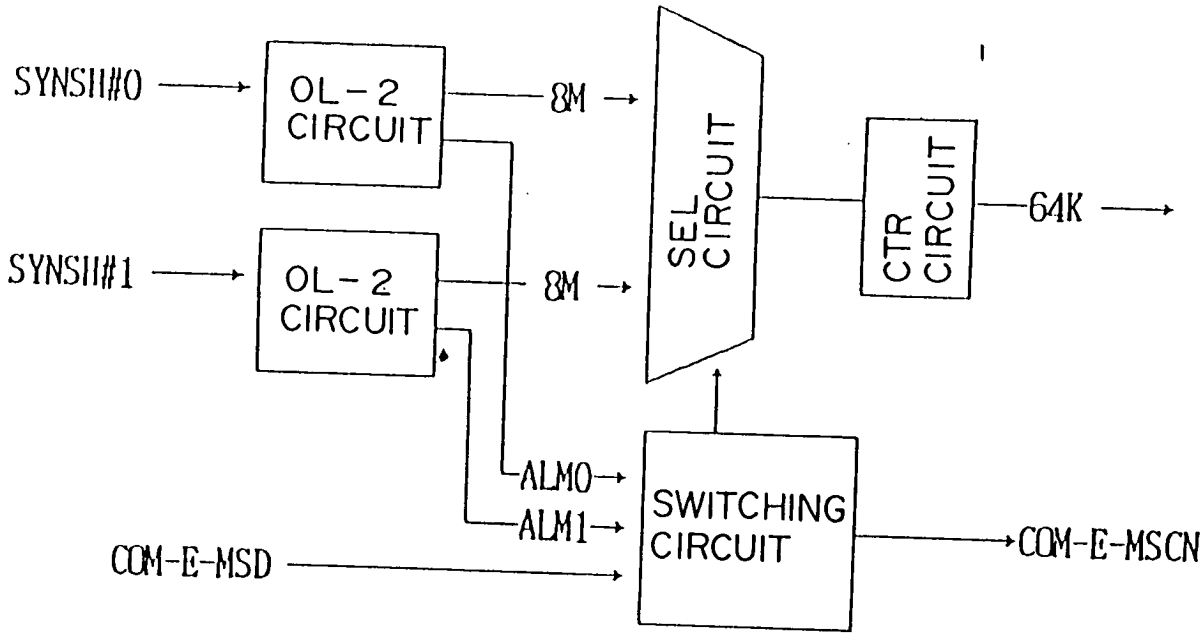

SYNSII#0
OL-2 CIRCUIT
8M
SYNSII#1
OL-2 CIRCUIT
8M
SEL CIRCUIT
CTR CIRCUIT
64K
ALM0
ALM1
SWITCHING CIRCUIT
COM-E-MSD
COM-E-MSCN

FIG. 100

COM-E-MSD INSTRUCTION		OL-2 CIRCUIT ALARM STATE		SELECTED SYSTEM (COM-E-MSCN)
SYSTEM #0	SYSTEM #1	SYSTEM #0	SYSTEM #1	
OFF	OFF	○	○	MAINTAINING OLD SYSTEM
ON	OFF	○	○	SYSTEM #0
OFF	ON	○	○	SYSTEM #1
(NOTE 1) ON	ON	○	○	MAINTAINING OLD SYSTEM
Don't	Care	○	×	SYSTEM #0
Don't	Care	×	○	SYSTEM #1
Don't	Care	×	×	MAINTAINING OLD SYSTEM

NOTE 1 : BOTH SYSTEMS CANNOT BE SELECTED AT COM-E-MSD WHEN SOFTWARE / FIRMWARE OPERATE NORMALLY.

FIG. 101

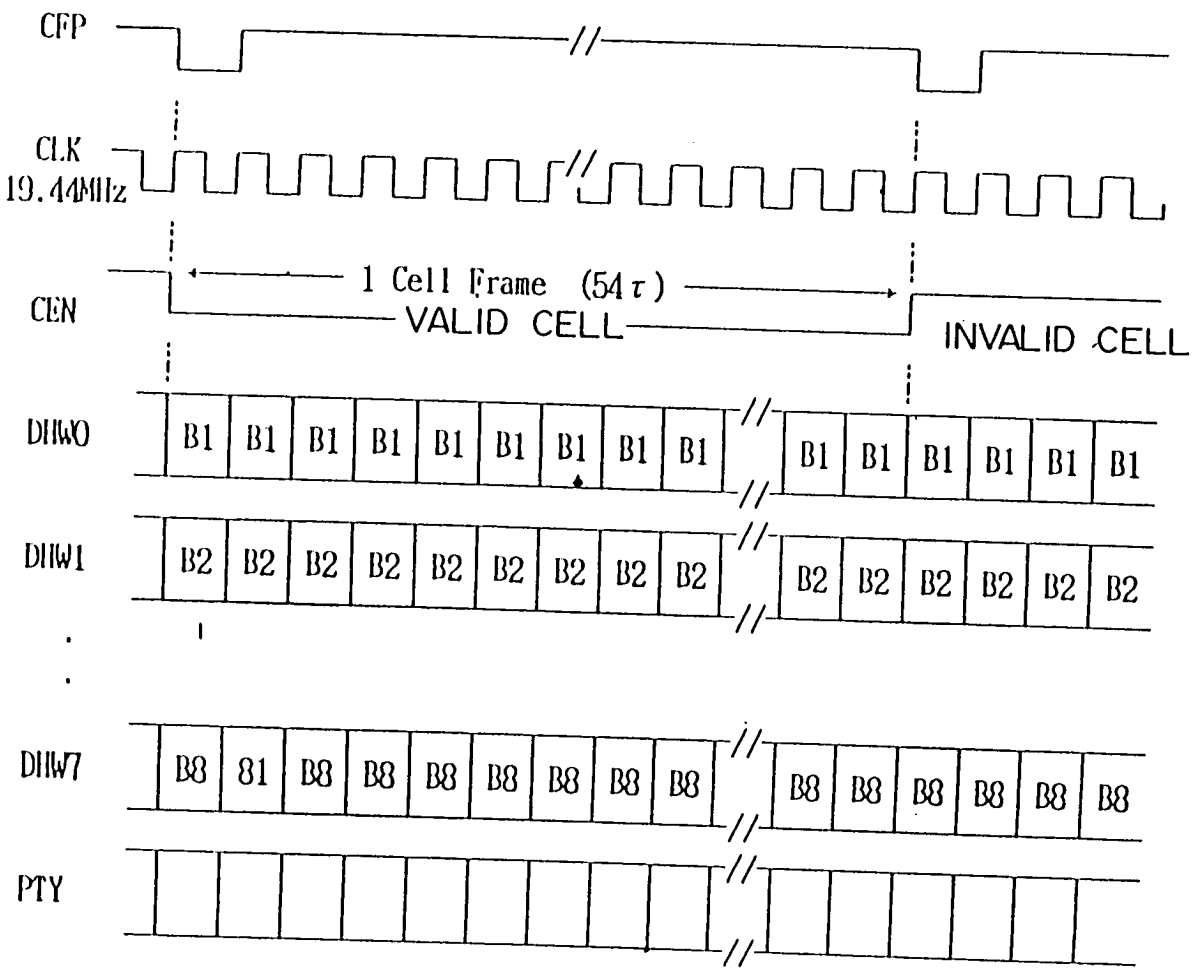

CFP
CLK
19.44MHz
1 Cell Frame (54τ)
CEN
VALID CELL
INVALID CELL
DIW0
DIW1
DIW7
PTY
B1
B2
B8
81

FIG. 102

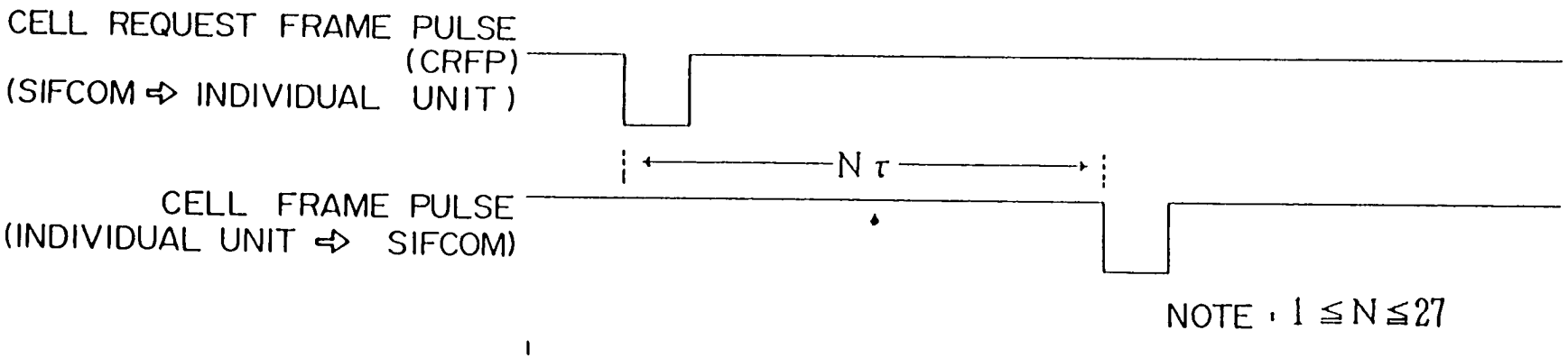

CELL REQUEST FRAME PULSE
(CRFP)
(SIFCOM ⇨ INDIVIDUAL UNIT)
Nτ
CELL FRAME PULSE
(INDIVIDUAL UNIT ⇨ SIFCOM)
NOTE : 1 ≦ N ≦ 27

FIG. 103

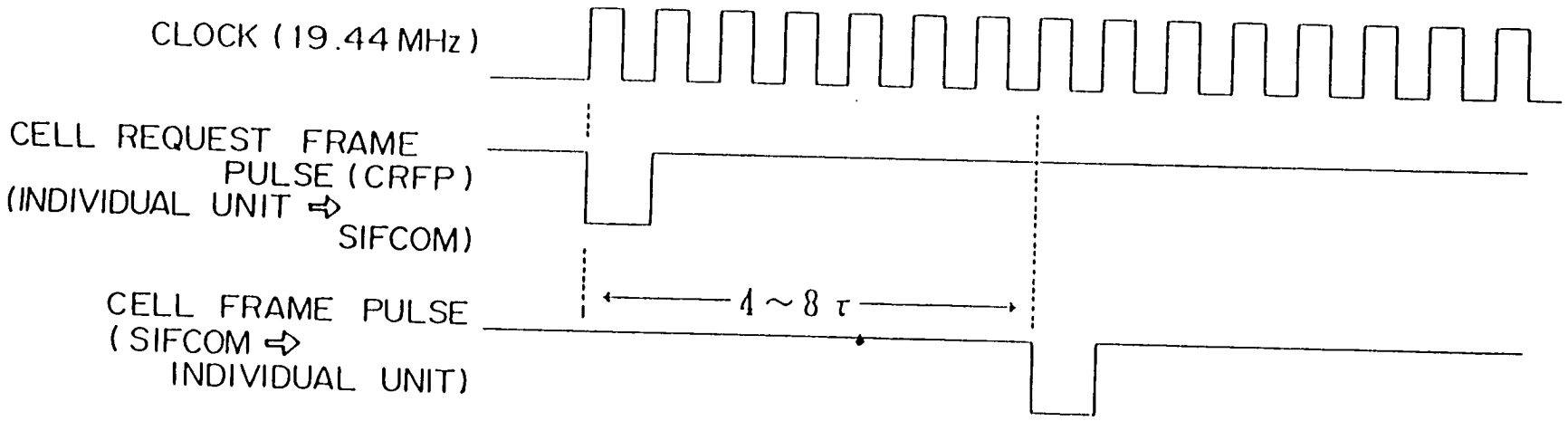

CLOCK (19.44 MHz)
CELL REQUEST FRAME PULSE (CRFP) (INDIVIDUAL UNIT ⇨ SIFCOM)
CELL FRAME PULSE (SIFCOM ⇨ INDIVIDUAL UNIT)
4 ~ 8 τ

FIG. 104

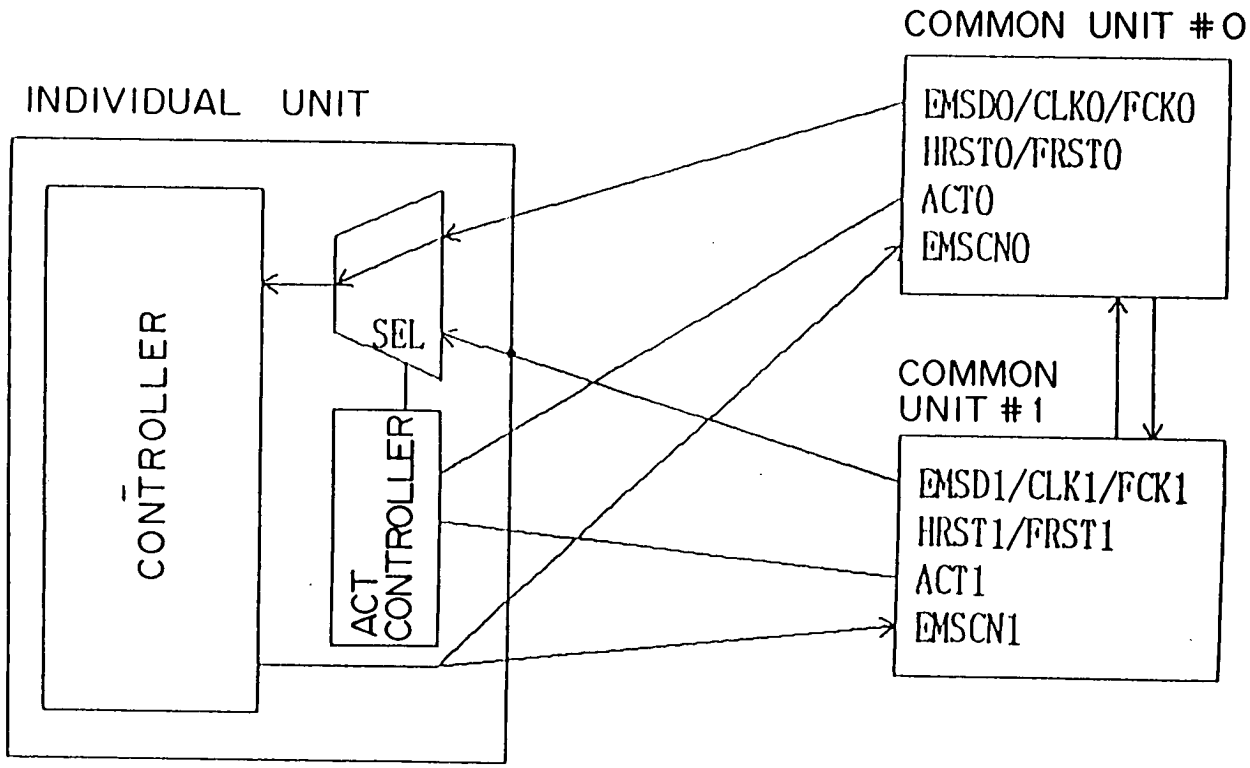
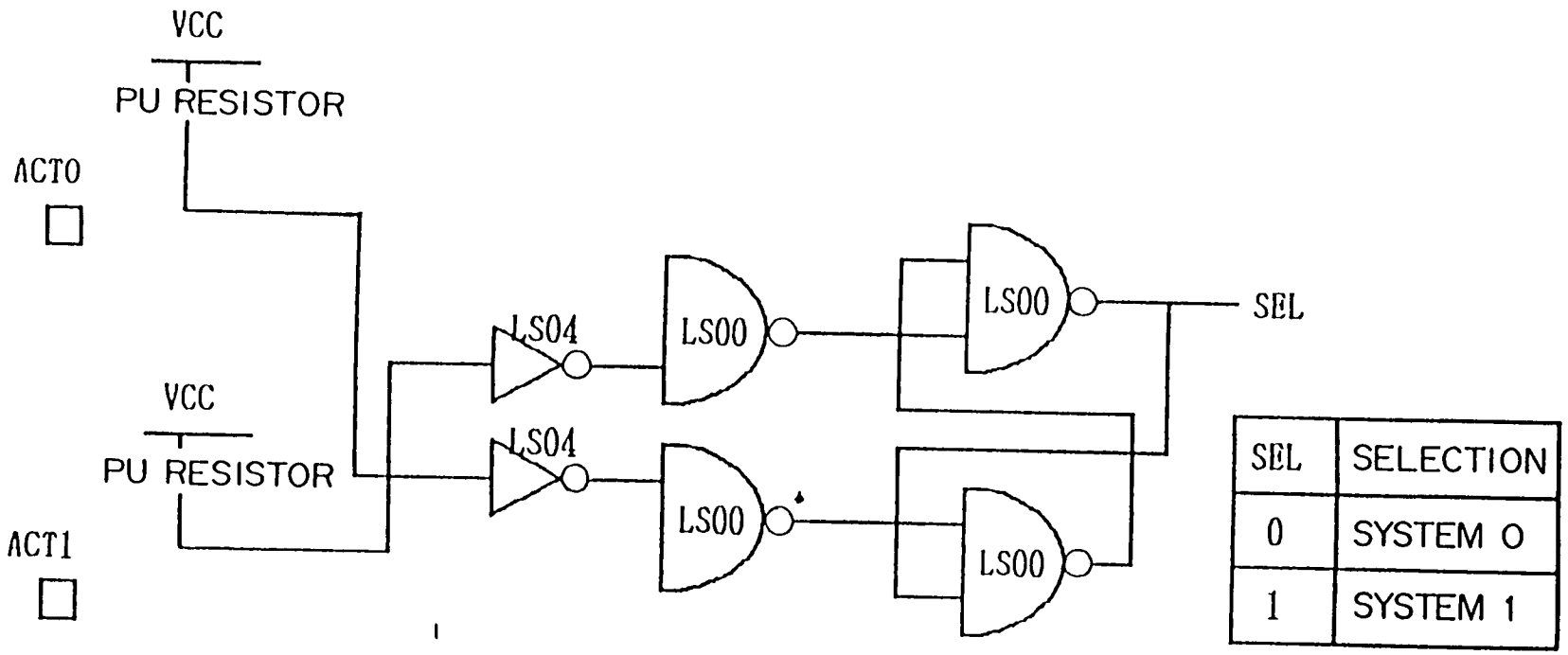

COMMON UNIT #0
INDIVIDUAL UNIT
EMSDO/CLKO/FCKO
HRSTO/FRSTO
ACTO
EMSCNO
CONTROLLER
SEL
ACT CONTROLLER
COMMON UNIT #1
EMSD1/CLK1/FCK1
HRST1/FRST1
ACT1
EMSCN1

FIG. 105

ACT0	ACT1	SYSTEM SELECTION
H	H	MAINTAINING PREVIOUS STATE
H	L	#1 ACT
L	H	#0 ACT
L	L	MAINTAINING PREVIOUS STATE

FIG. 106



SEL	SELECTION
0	SYSTEM 0
1	SYSTEM 1

FIG. 107

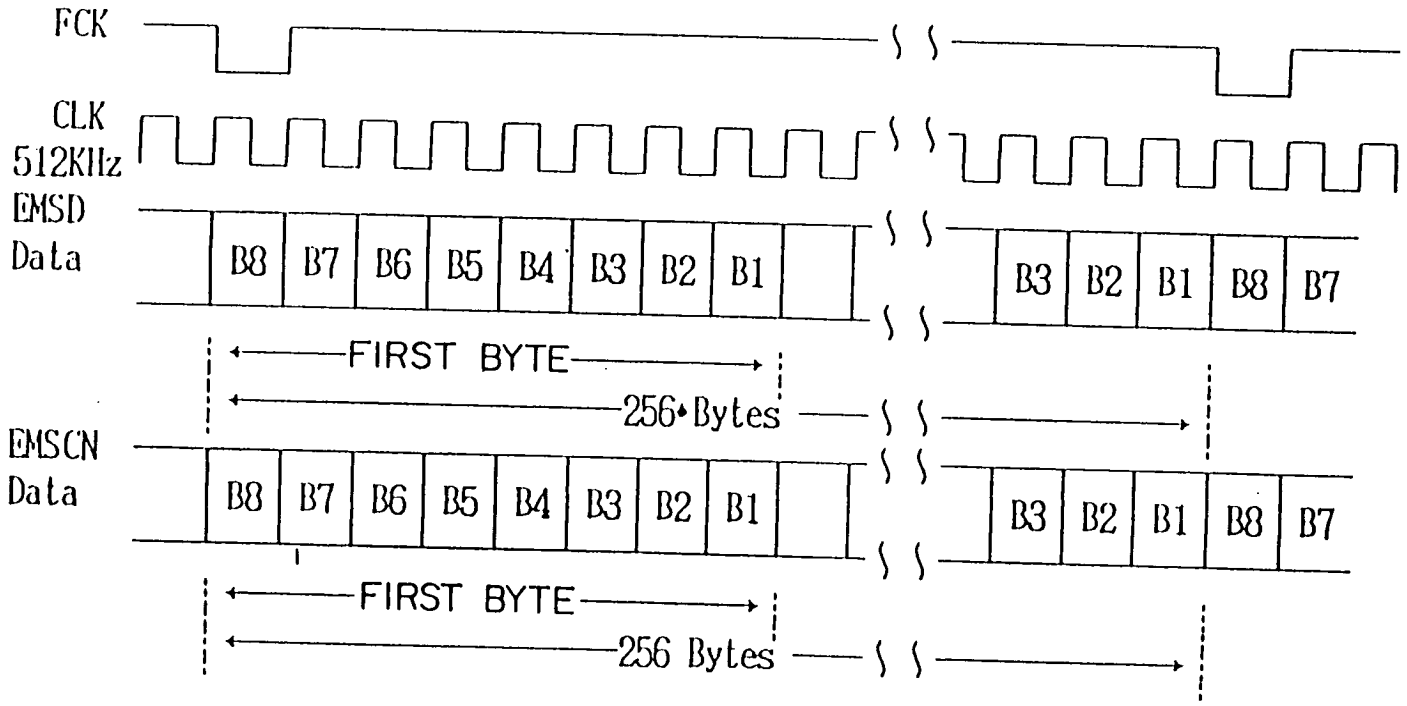

FCK
CLK
512KHz
EMSD
Data
B8
B7
B6
B5
B4
B3
B2
B1
B3
B2
B1
B8
B7
FIRST BYTE
256 Bytes
EMSCN
Data
B8
B7
B6
B5
B4
B3
B2
B1
B3
B2
B1
B8
B7
FIRST BYTE
256 Bytes

FIG. 108

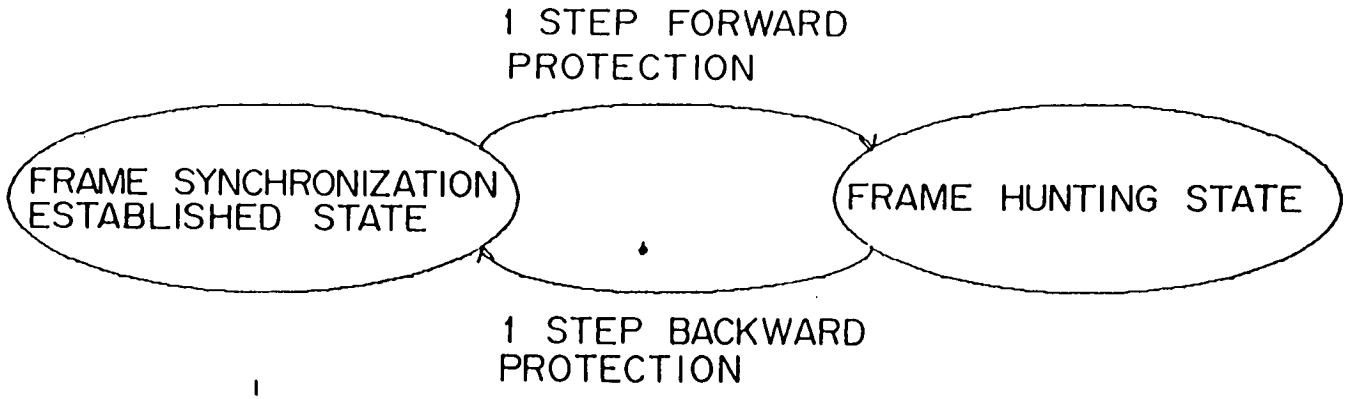
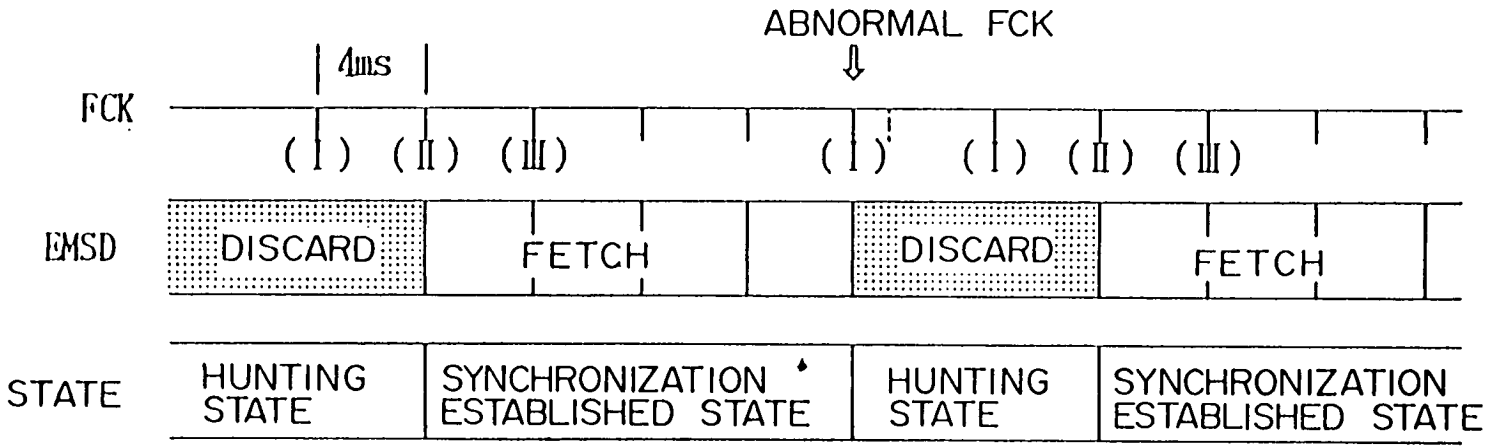

1 STEP FORWARD
PROTECTION
FRAME SYNCHRONIZATION
ESTABLISHED STATE
FRAME HUNTING STATE
1 STEP BACKWARD
PROTECTION

FIG. 109



(I) FRAME SYNCHRONIZATION START REFRENCE FCK
(II) FIRST NORMAL FCK
(III) SECOND NORMAL FCK

FIG. 11O

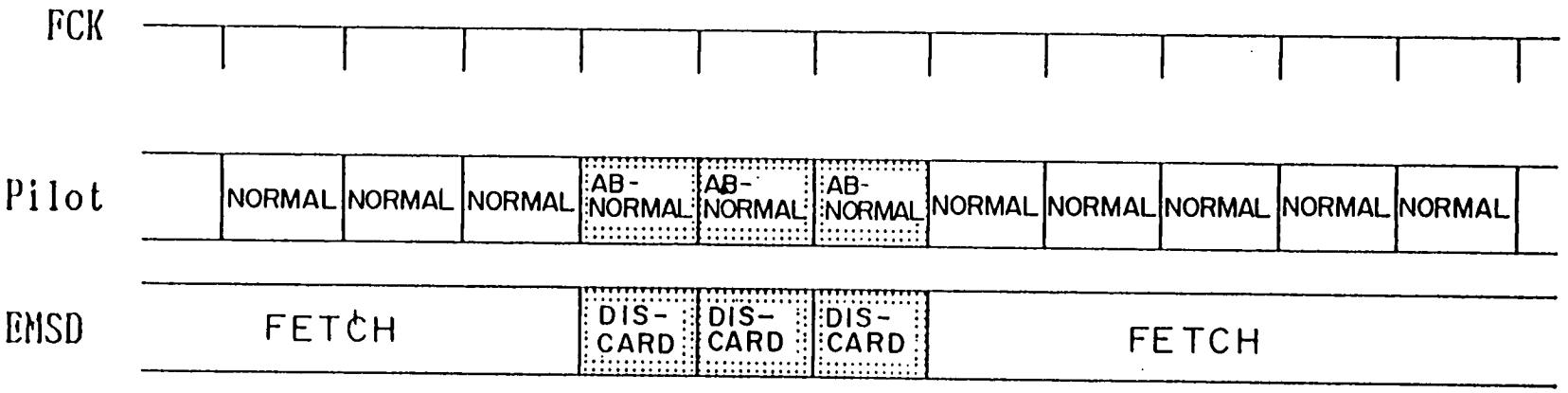

FCK
Pilot
NORMAL
NORMAL
NORMAL
AB-NORMAL
AB-NORMAL
AB-NORMAL
NORMAL
NORMAL
NORMAL
NORMAL
NORMAL
EMSD
FETCH
DIS-CARD
DIS-CARD
DIS-CARD
FETCH

FIG. 111

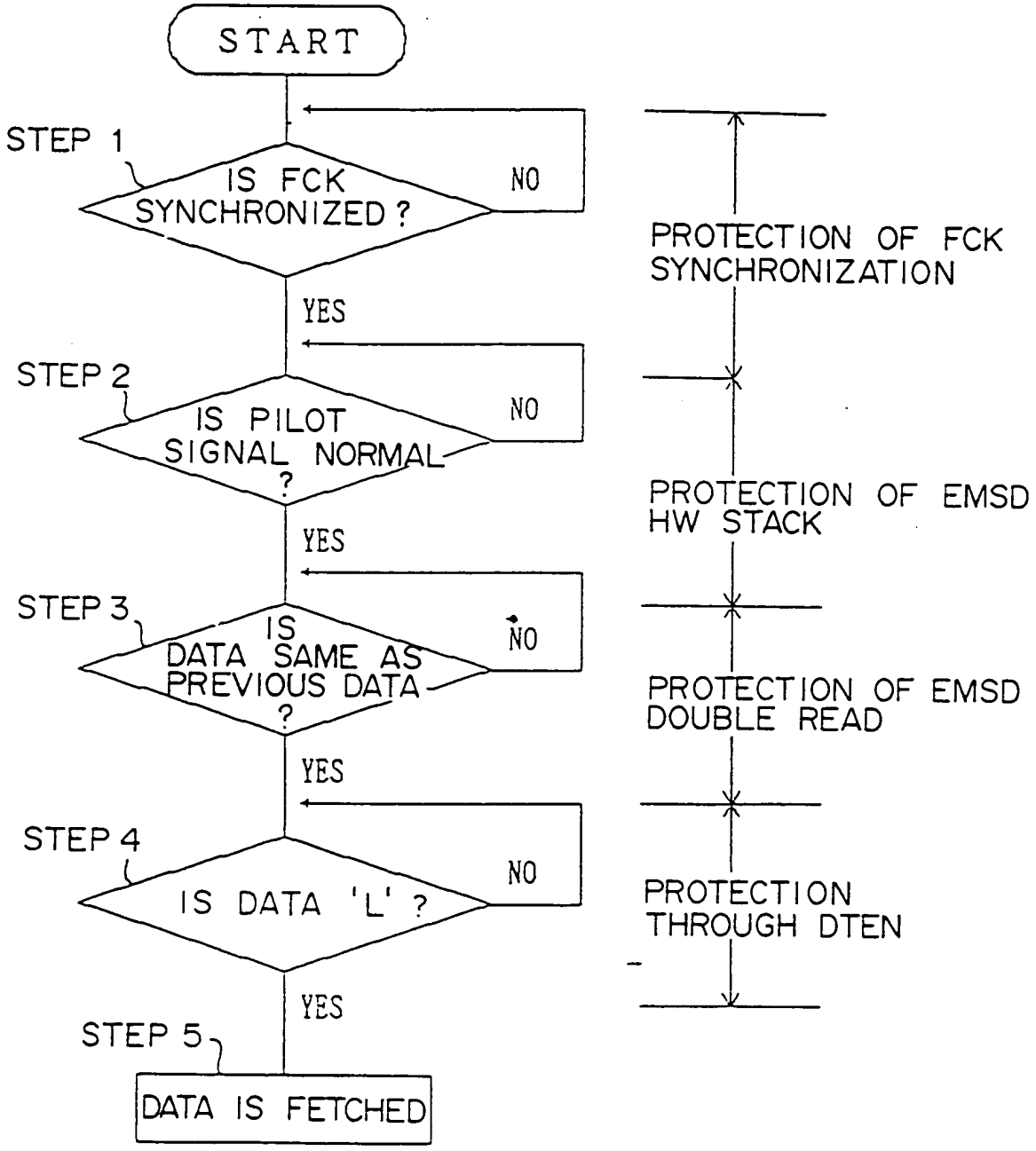
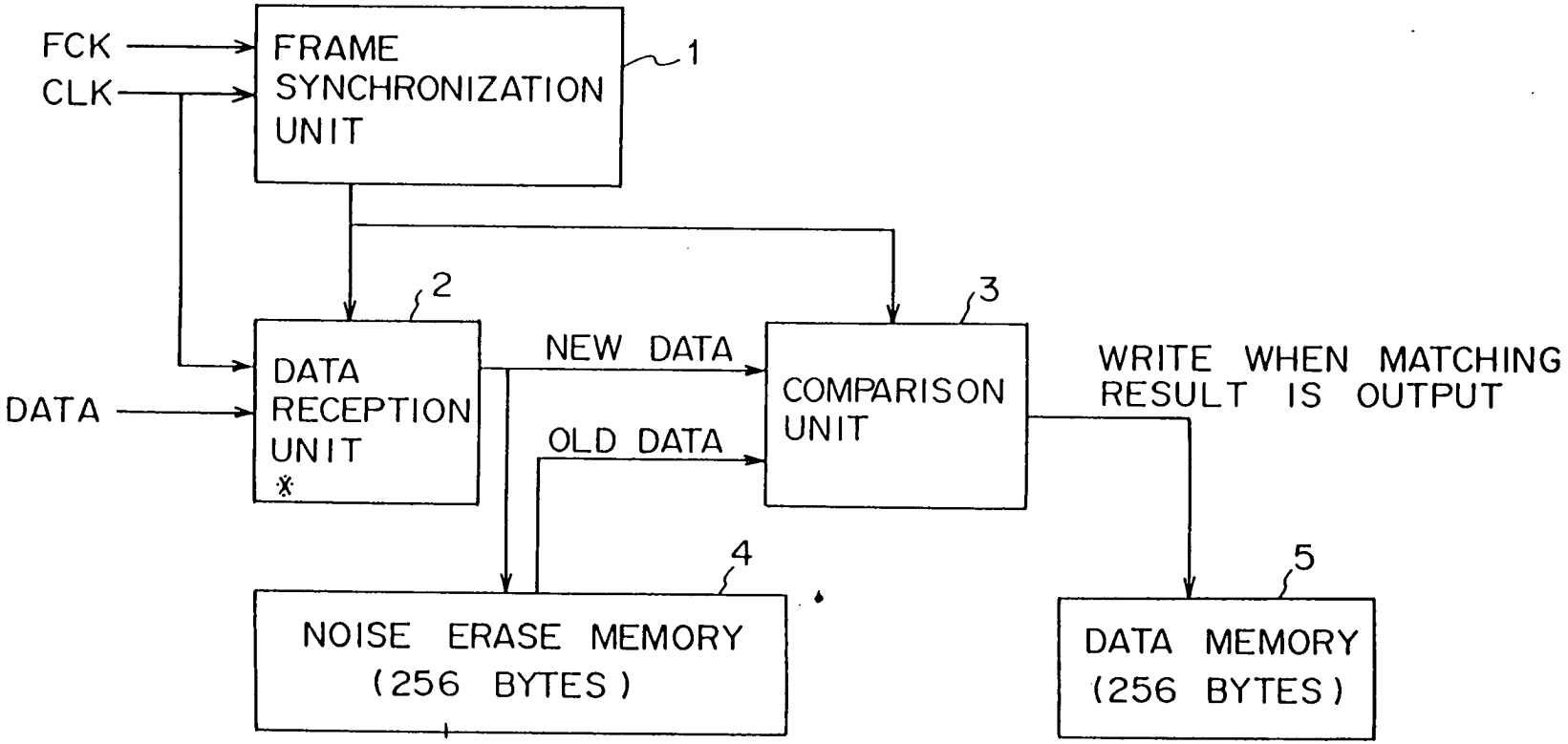

START
STEP 1
IS FCK SYNCHRONIZED ?
NO
YES
STEP 2
IS PILOT SIGNAL NORMAL ?
NO
YES
STEP 3
IS DATA SAME AS PREVIOUS DATA ?
NO
YES
STEP 4
IS DATA 'L' ?
NO
YES
STEP 5
DATA IS FETCHED
PROTECTION OF FCK SYNCHRONIZATION
PROTECTION OF EMSD HW STACK
PROTECTION OF EMSD DOUBLE READ
PROTECTION THROUGH DTEN

FIG. 112



※ : PILOT SIGNAL IS CHECKED AND DTEM MONITOR IS PERFOMED IN THIS BLOCK.

FIG. 113

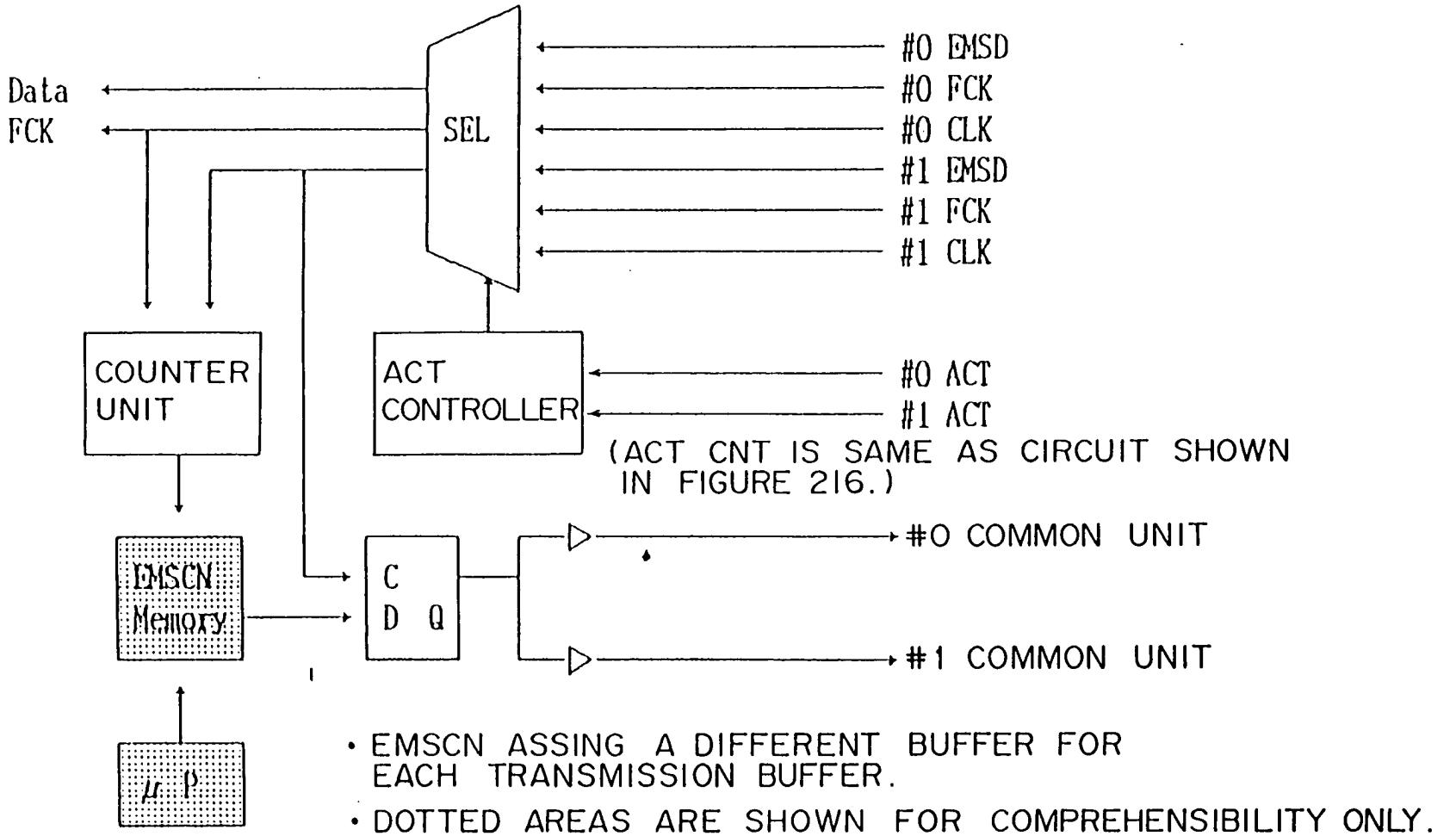

Data
FCK
SEL
#0 EMSD
#0 FCK
#0 CLK
#1 EMSD
#1 FCK
#1 CLK
COUNTER UNIT
ACT CONTROLLER
#0 ACT
#1 ACT
(ACT CNT IS SAME AS CIRCUIT SHOWN IN FIGURE 216.)
EMSCN Memory
C
D Q
#0 COMMON UNIT
#1 COMMON UNIT
μ P
• EMSCN ASSING A DIFFERENT BUFFER FOR EACH TRANSMISSION BUFFER.
• DOTTED AREAS ARE SHOWN FOR COMPREHENSIBILITY ONLY.

FIG. 114

FAULT	INDIVIDUAL UNIT		COMMON UNIT	
	FAULT DETECTING METHOD	FAULT NOTIFYING METHOD	FAULT DETECTING METHOD	TYPE OF FAULT
EMSD HW STACK	PLTO/1 ASYNCHRONIZATION	EMSCN(PLTF)	EMSCN(PLTF)	EMSD HW STACK
512 CLOCK STACK	INDIVIDUAL UNIT LOCKED	EMSCN STACK	EMSCN PLTO/1 STACK	EMSCN HW STACK
FCK STACK	FCK STACK	EMSCN(SYNCF)	EMSCN(SYNCF)	FCK ASYNCHRONIZATION
EMSCN HW STACK			EMSCN PLTO/1 STACK	EMSCN HW STACK

FIG. 115

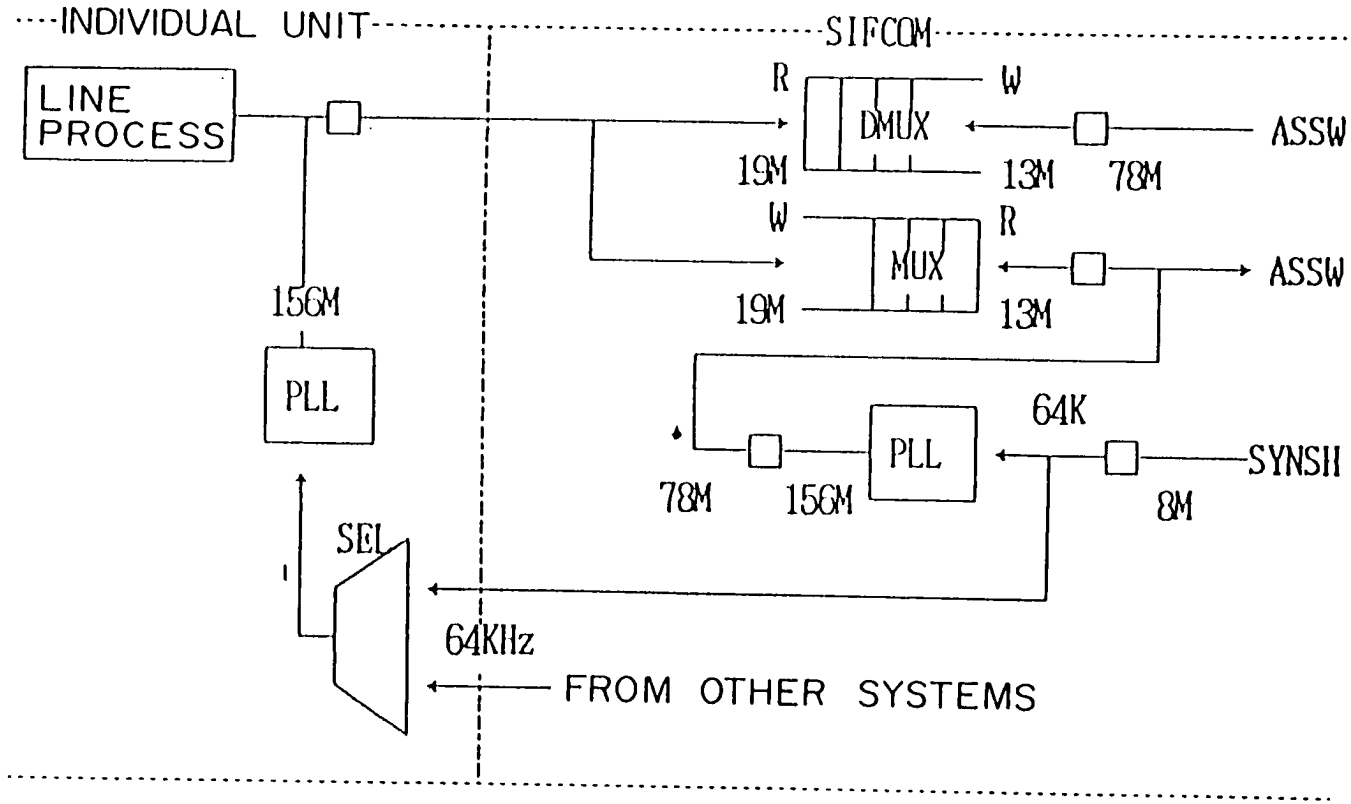

INDIVIDUAL UNIT
SIFCOM
LINE PROCESS
R
W
DMUX
ASSW
19M
13M
78M
W
R
MUX
ASSW
19M
13M
156M
PLL
64K
PLL
SYNSH
78M
156M
8M
SEL
64KHz
FROM OTHER SYSTEMS

FIG. 116

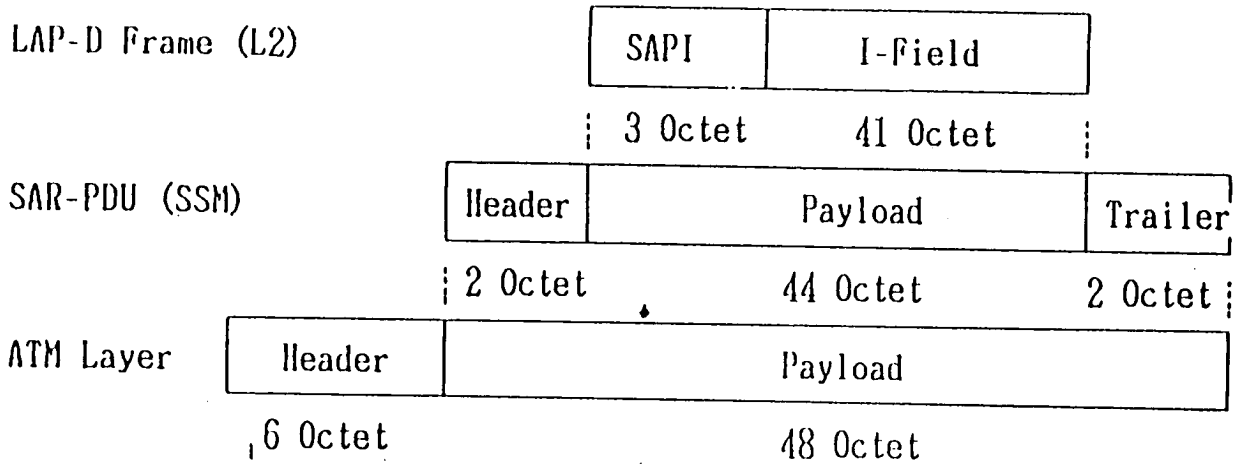
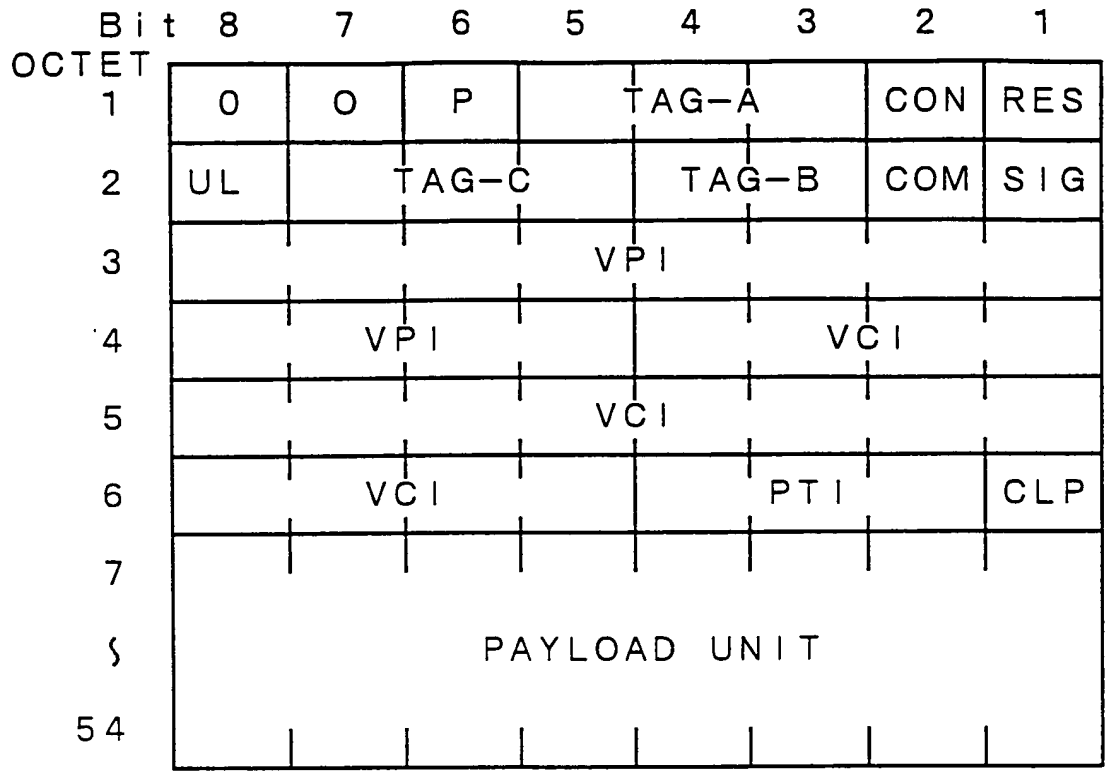

LAP-D Frame (L2)
SAPI
I-Field
3 Octet
41 Octet
SAR-PDU (SSM)
Header
Payload
Trailer
2 Octet
44 Octet
2 Octet
ATM Layer
Header
Payload
6 Octet
48 Octet

FIG. 117



O : INTERNAL CELL INDICATOR.
INTRA-STATION COMMUNICATIONS CELL IS FIXED TO "1".

P : QUALITY INDICATOR.
HIGH QUALITY IS FIXED TO "1" BY FIRMWARE.

CON : HIGH PRIORITY CLASS.
HIGH PRIORITY IS FIXED TO "1" BY FIRMWARE.

RES : FORCED BLANK CELL INDICATOR. FIXED TO "0".

COM : COMMON UNIT SIGNALLING SPECIFICAON OF "1"
(COMMON UNIT IS SPECIFIED).

SIG : SIGNALING SPECIFICATION TAG OF "1" (SIGNALING).

VPI : FIXED VALUE IS DEFINED
WHEN INTRA-STATION SIGNALING IS ADOPTED.

VCI : FIXED VALUE IS DEFINED
WHEN INTRA-STATION SIGNALING IS ADOPTED.

PTI : FIXED VALUE OF "000"

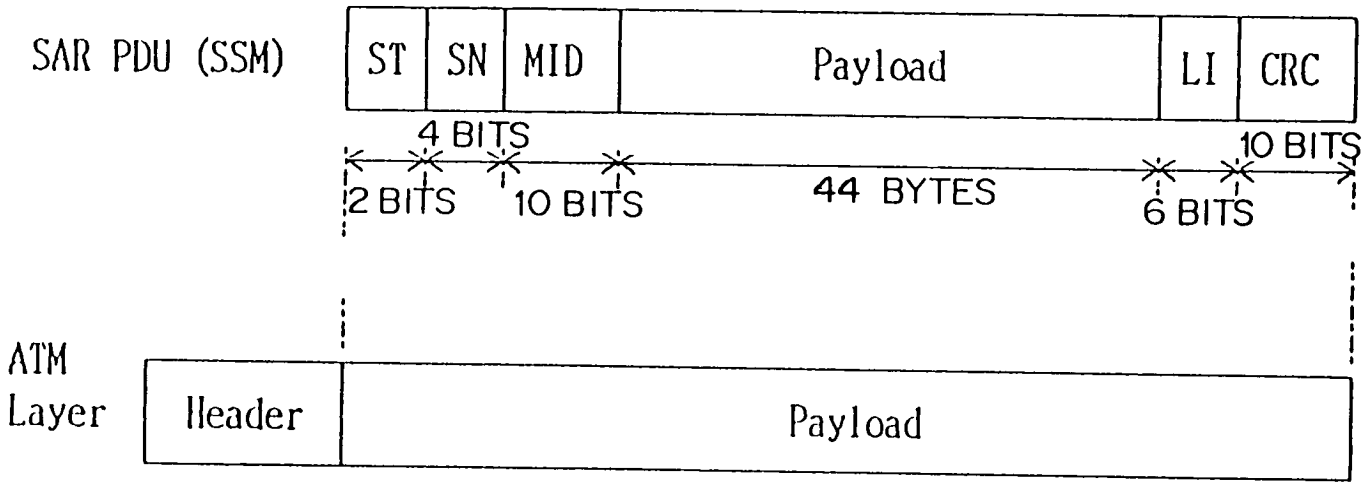
CLP : FIXED VALUE OF "0"

TAG-A : CELL ROUTING INDICATOR

TAG-B : CELL ROUTING INDICATOR

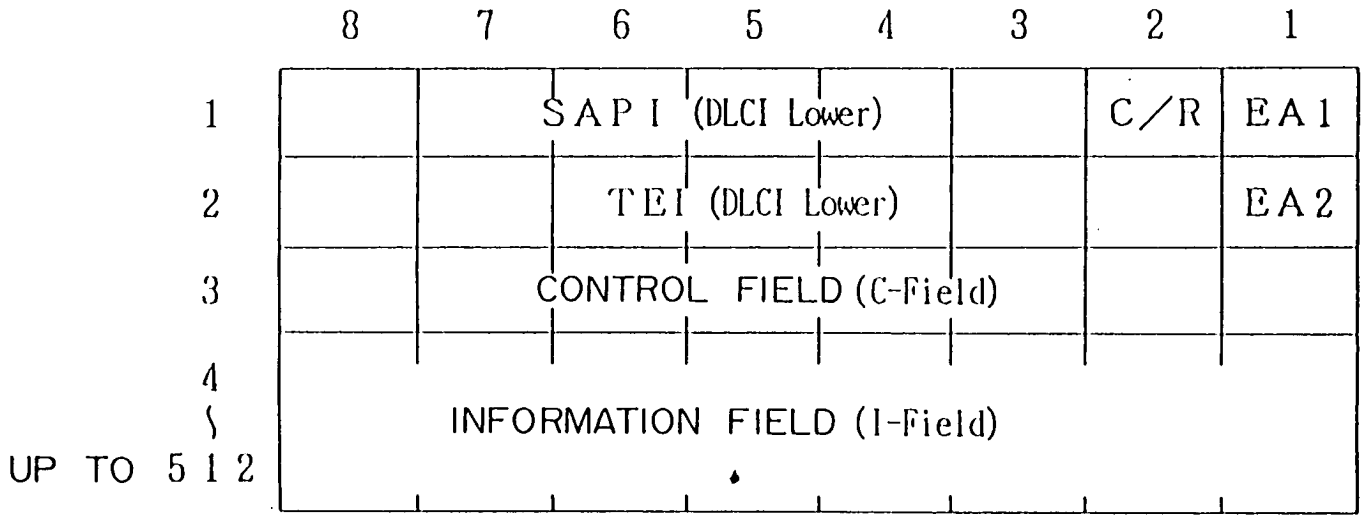
TAG-C : CELL ROUTING INDICATOR

FIG. 118



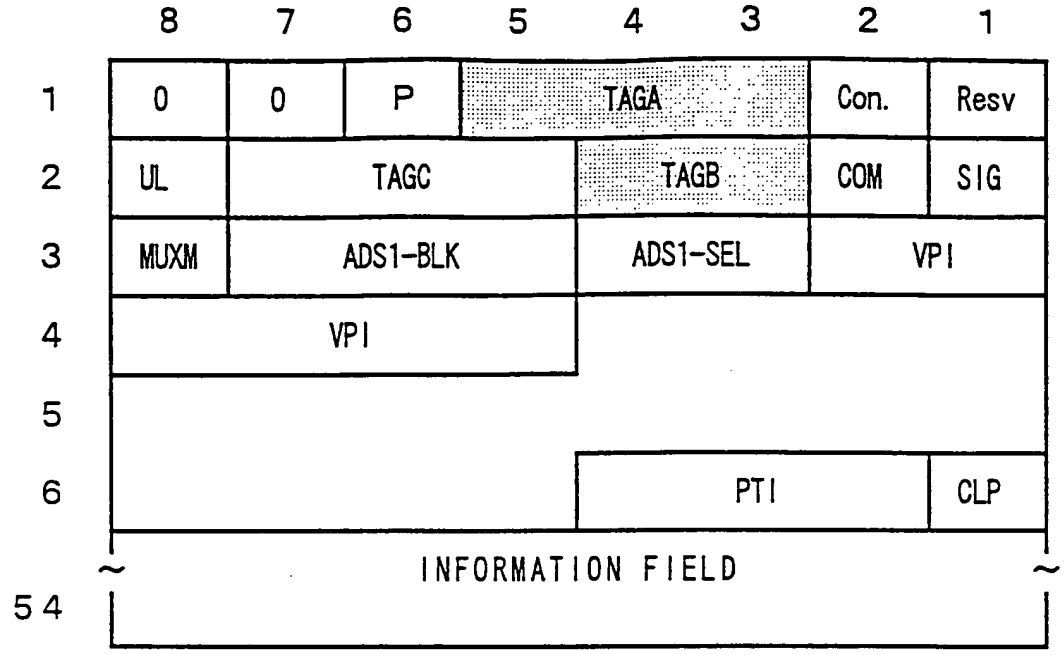
ST : SEGMENT TYPE (BOM = "00" / COM = "01" / EOM = "10" / SSM = "11")
SN : SEQUENCE NUMBER ("0000" ⇨ "1111" CYCLIC INCREMENT)
MID : NOT DEFINED WHEN INTRA-STATION SIGNALING IS ADOPTED (RECEIVED CELL D.C. / TRANSMITTED CELL ALL BITS "0")
LI : LENGTH INDICATOR (SIGNIFICANT BYTE LENGTH INDICATOR IN PAYLOAD (BOM, COM, = "101100" SSM, EOM = OPTIONAL LENGTH)
CRC : CRC (CRC-10 FOR ST, SN, MID, AND PAYLOAD)

FIG. 119



SAPI : ALL BITS ARE SET TO "0" AS FIXED VALUE.
TEI : ALL BITS ARE SET TO "0" AS FIXED VALUE.
C/R : COMMAND = "0" / RESPONSE = "1"
EA1 : EXTENSION ADDRESS "0" AS FIXED VALUE.
EA2 : EXTENSION ADDRESS "1" AS FIXED VALUE.
CONTROL FIELD : SABM = "01111111" / UA = "01110011" /
UI = "00000011" / RR = "00000001"

FIG. 120



0 : FIXED VALUE (COPY INDICATOR.
"0" INDICATES ONE TO ONE TRANSMISSION)

0 : INTERNAL TEST CELL INDICATOR ("0" INDICATES A USER CELL WHILE "1" INDICATES INTERNAL CELL)

P : HIGH PRIORITY CLASS ("0" FOR HIGHER PRIORITY; AND "1" FOR LOWER PRIORITY.)

Con. : CONGESTION CONTROL (IMPORTANT CALLS FROM POLICE AND FIRE DEPARTMENTS ARE IDENTIFIED)

Resv : RESERVE BITS
USED TO IDENTIFY INSIGNIFICANT CELL WHEN SYSTEMS ARE SWITCHED IN BSGCSH.

TAGA : 2.4G 4×4 HIGHWAY IS SELECTED IN SW (AHM SPECIFICATION)
(2 BITS ONLY ARE UNED IN 3 BITS. POSITION AND POLARITY OF REMAINING ONE BIT ARE NOT CHECKED.)

TAGB : 2.4G 622M×4 HIGHWAY IS SELECTED IN SW (AHM SPECIFICATION)
USED AS UL IN RMXSH

TAGC : SELECTING 622M → 156M HIGHWAY -

UL : HIGHER/LOWER ORDER IN DAISY CHAIN

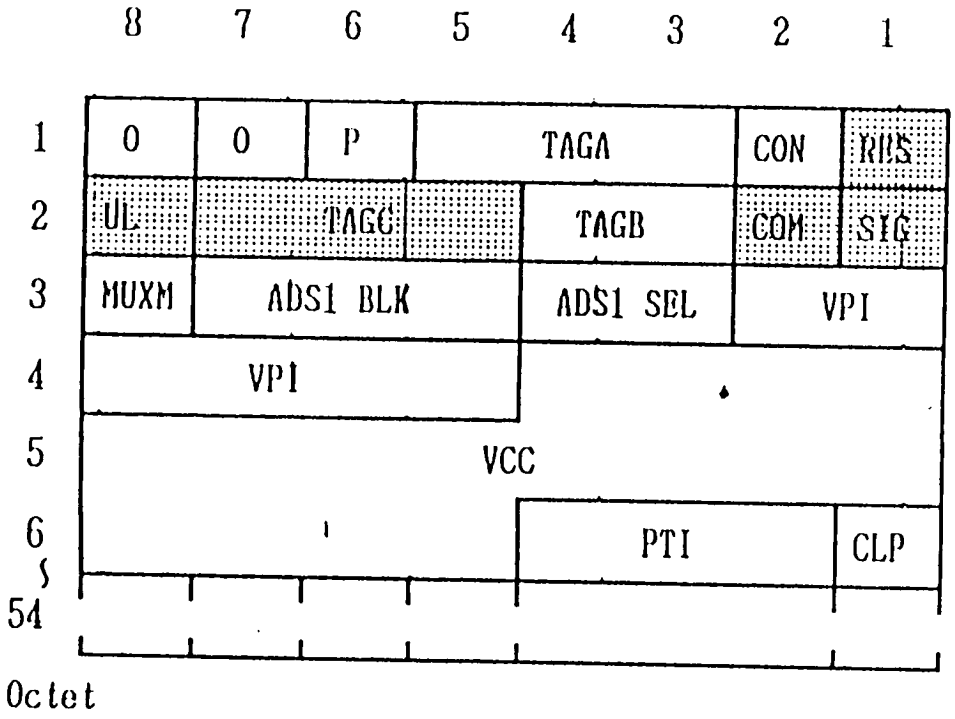
COM : SELECTING COMMON UNIT
USED TO IDENTIFY CELL FROM SIMPLEX/DUPLEX DEVICE IN BSGCSH.

SIG : IDENTIFICATION OF INTRA-STATION LAP CELL

MUXM : FOR DS1 CARDS IN AND AFTER MUX MULTICAST BIT MUX

ADS1-SEL : SELECTING ADSI CARD

FIG. 121



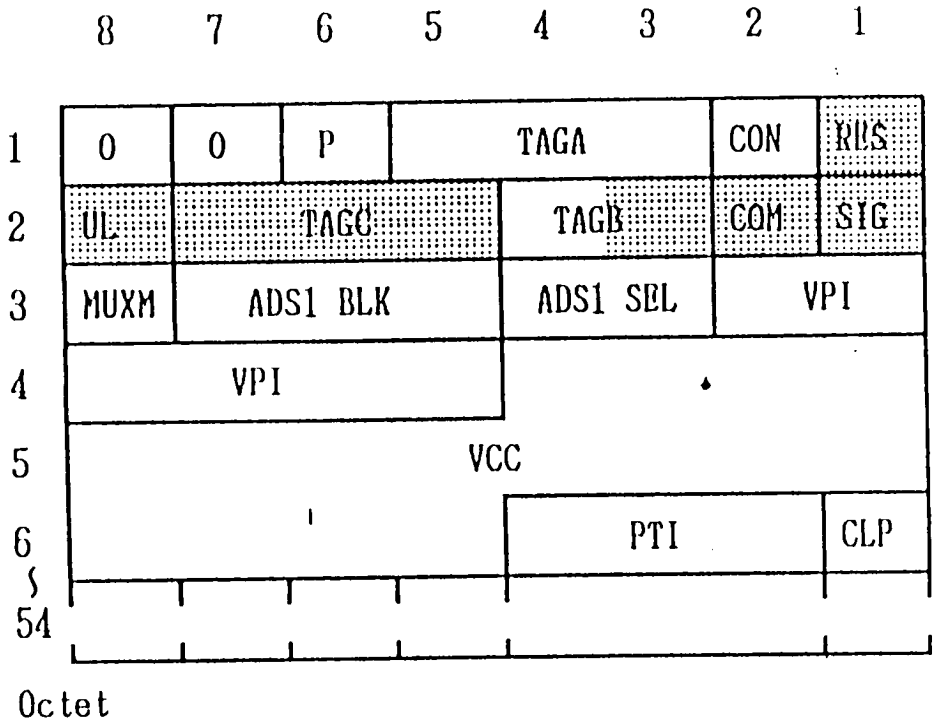
: USED IN SIFCOM

SIG, UL, TAGC, COM :
TAG FOR HIGHWAYS OF OR SMALLER THAN 622M.

FIG. 122

SIG	UL	TAGC	COM	TRANSMISSION LINE
0/1	0	000	0	SIFSHH0 LINE0/SIGNALING
0/1	0	001	0	SIFSHH0 LINE1/SIGNALING
		⟆		⟆
0/1	0	111	0	SIFSHH0 LINE7/SIGNALING
0/1	1	000	0	SIFSHH1 LINE0/SIGNALING
0/1	1	001	0	SIFSHH1 LINE1/SIGNALING
		⟆		⟆
0/1	1	111	0	SIFSHH1 LINE7/SIGNALING
1	0	000	1	SIFSHH0 COM SIGNALING
1	1	000	1	SIFSHH1 COM SIGNALING

FIG. 123



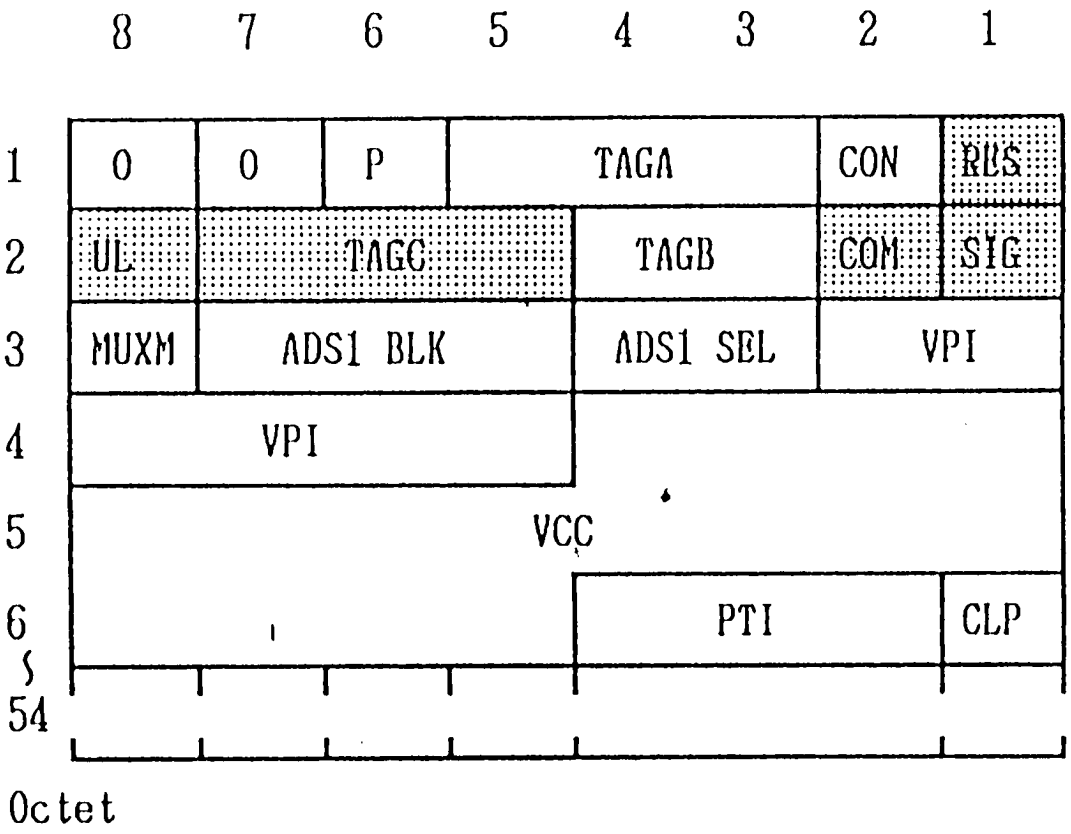
: USED IN RMUXCOM

SIG, UL, TAGB, TAGC,
COM :
TAG FOR HIGHWAYS OF SMALLER THAN 622M (ONLY LOWEST BIT OF TAGB IS USED)

FIG. 124

SIG	UL	TAGB	TAGC	COM	TRANSMISSION LINE
0/1	0	0	000	0	RMUXSH#0 LINE0 / SIGNALING
0/1	0	0	001	0	RMUXSH#0 LINE1 / SIGNALING
			⟆		⟆
0/1	0	0	111	0	RMUXSH#0 LINE7 / SIGNALING
0/1	1	0	000	0	RMUXSH#1 LINE0 / SIGNALING
0/1	1	0	001	0	RMUXSH#1 LINE1 / SIGNALING
			⟆		⟆
0/1	1	0	111	0	RMUXSH#1 LINE7 / SIGNALING
0/1	1	1	000	0	RMUXSH#2 LINE0 / SIGNALING
0/1	1	1	001	0	RMUXSH#2 LINE1 / SIGNALING
			⟆		⟆
0/1	1	1	111	0	RMUXSH#2 LINE7 / SIGNALING
1	0	0	000	1	RMUXSH#0 COM SIGNALING
1	1	0	000	1	RMUXSH#1 COM SIGNALING
1	1	1	000	1	RMUXSH#2 COM SIGNALING

FIG. 125



: USING BSGC-COM

SIG, UL, TAGC :
TAG FOR HIGHWAYS OF OR SMALLER THAN 622M.

COM :
SIGNALING CELL FROM SIMPLEX / DUPLEX UNITS

RES :
WHEN SYSTEMS ARE SWITCHED

FIG. 126

SIG	UL	TAGC	TRANSMISSION LINE
0	0	000	BSGCSH#0/LINE0
0	0	001	BSGCSH#0/LINE1
		⟆	⟆
0	0	111	BSGCSH#0/LINE7
0	1	000	BSGCSH#1/LINE0
0	1	001	BSGCSH#1/LINE1
		⟆	⟆
0	1	111	BSGCSH#1/LINE7
1	0	000	BSGCSH#2/LINE0
1	0	001	BSGCSH#2/LINE1
		⟆	⟆
1	0	111	BSGCSH#2/LINE7
1	1	000	BSGCSH#3/LINE0
1	1	001	BSGCSH#3/LINE1
		⟆	⟆
1	1	111	BSGCSH#3/LINE7

FIG. 127

SIG	ADSI BLK	ADSI SEL	
0	000 ~	0 0 ~ 1 1	USER CELL TO DTC 0/ Line 0 ~ USER CELL TO DTC 0/ Line 3
0	111	0 0 ~ 1 1	USER CELL TO DTC 7/ Line 0 ~ USER CELL TO DTC 7/ Line 3
1	000 ~	0 0 ~ 1 1	LAP CELL TO DTC 0/ Line 0 ~ LAP CELL TO DTC 0/ Line 3
1	111	0 0 ~ 1 1	LAP CELL TO DTC 7/ Line 0 ~ LAP CELL TO DTC 7/ Line 3

FIG. 128

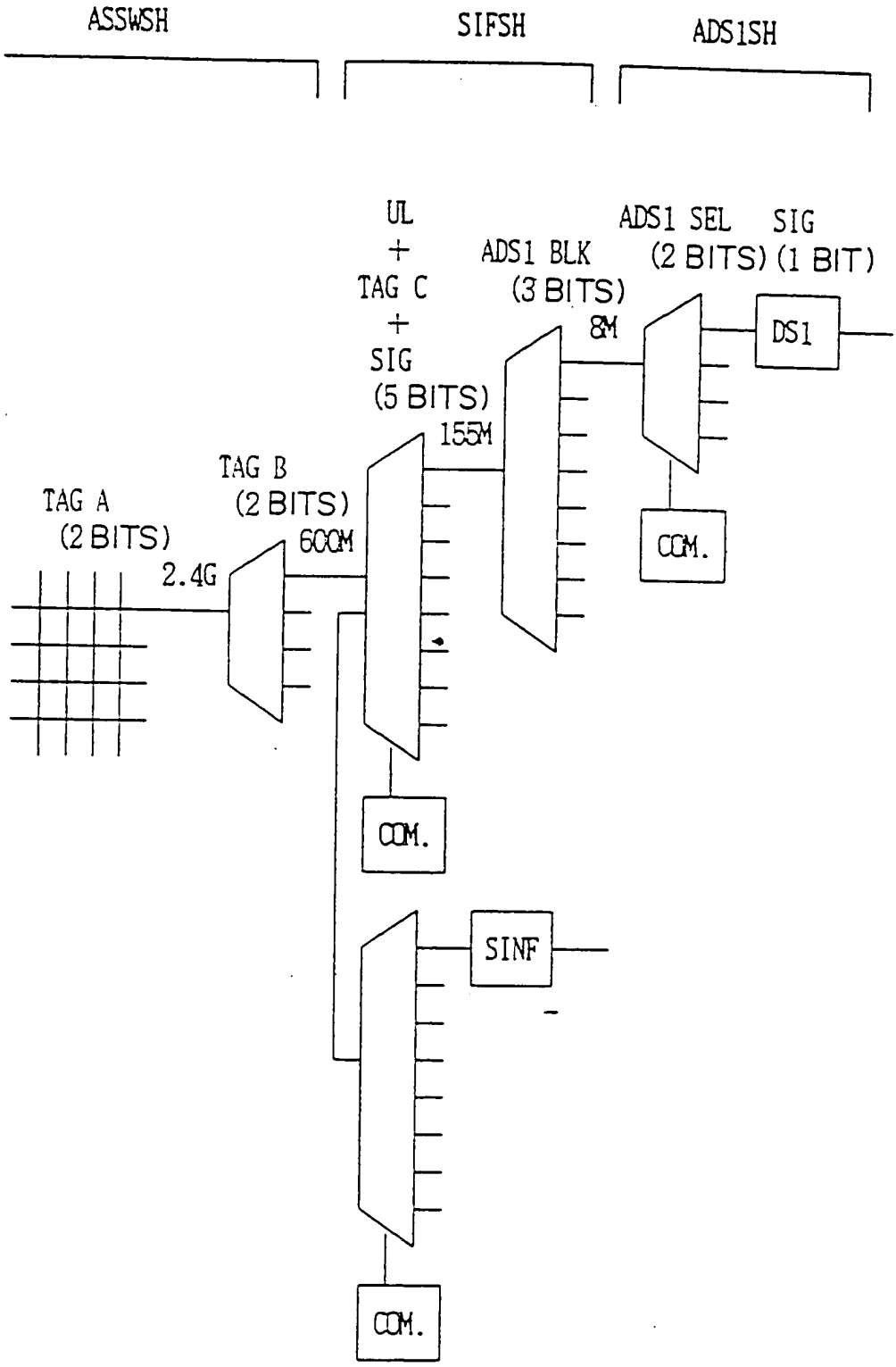

ASSWSH
SIFSH
ADS1SH
UL
+
TAG C
+
SIG
(5 BITS)
ADS1 BLK
(3 BITS)
ADS1 SEL
(2 BITS)
SIG
(1 BIT)
8M
DS1
155M
TAG B
(2 BITS)
TAG A
(2 BITS)
600M
2.4G
COM.
COM.
SINF
COM.

FIG. 129

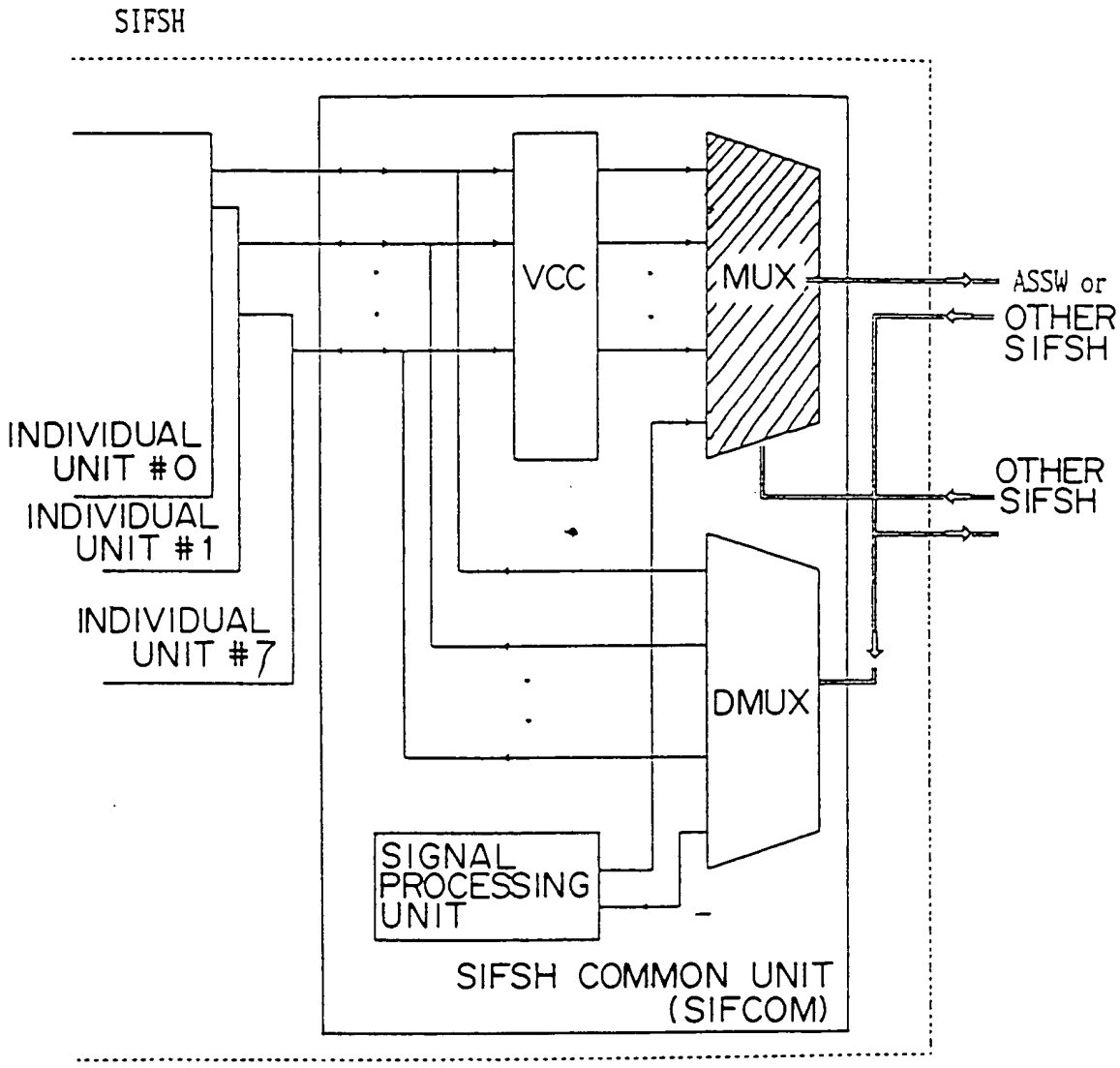
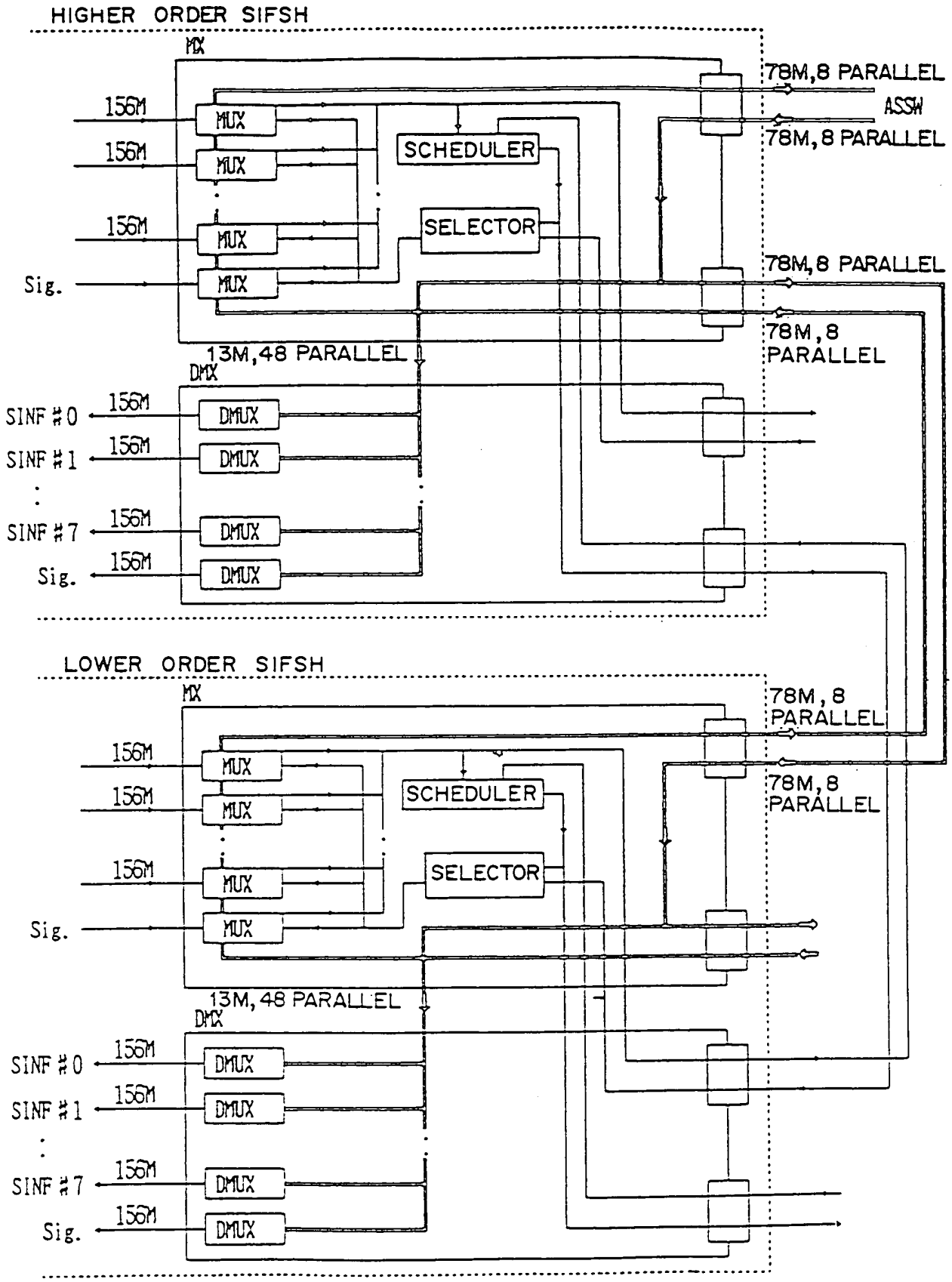

SIFSH
VCC
MUX
ASSW or
OTHER
SIFSH
OTHER
SIFSH
INDIVIDUAL
UNIT #0
INDIVIDUAL
UNIT #1
INDIVIDUAL
UNIT #7
DMUX
SIGNAL
PROCESSING
UNIT
SIFSH COMMON UNIT
(SIFCOM)

FIG. 130



SELECTOR : LOWER ORDER DEVICE IN DAISY CHAIN SELECTS SIGNAL FROM HIGHER ORDER.

FIG. 131

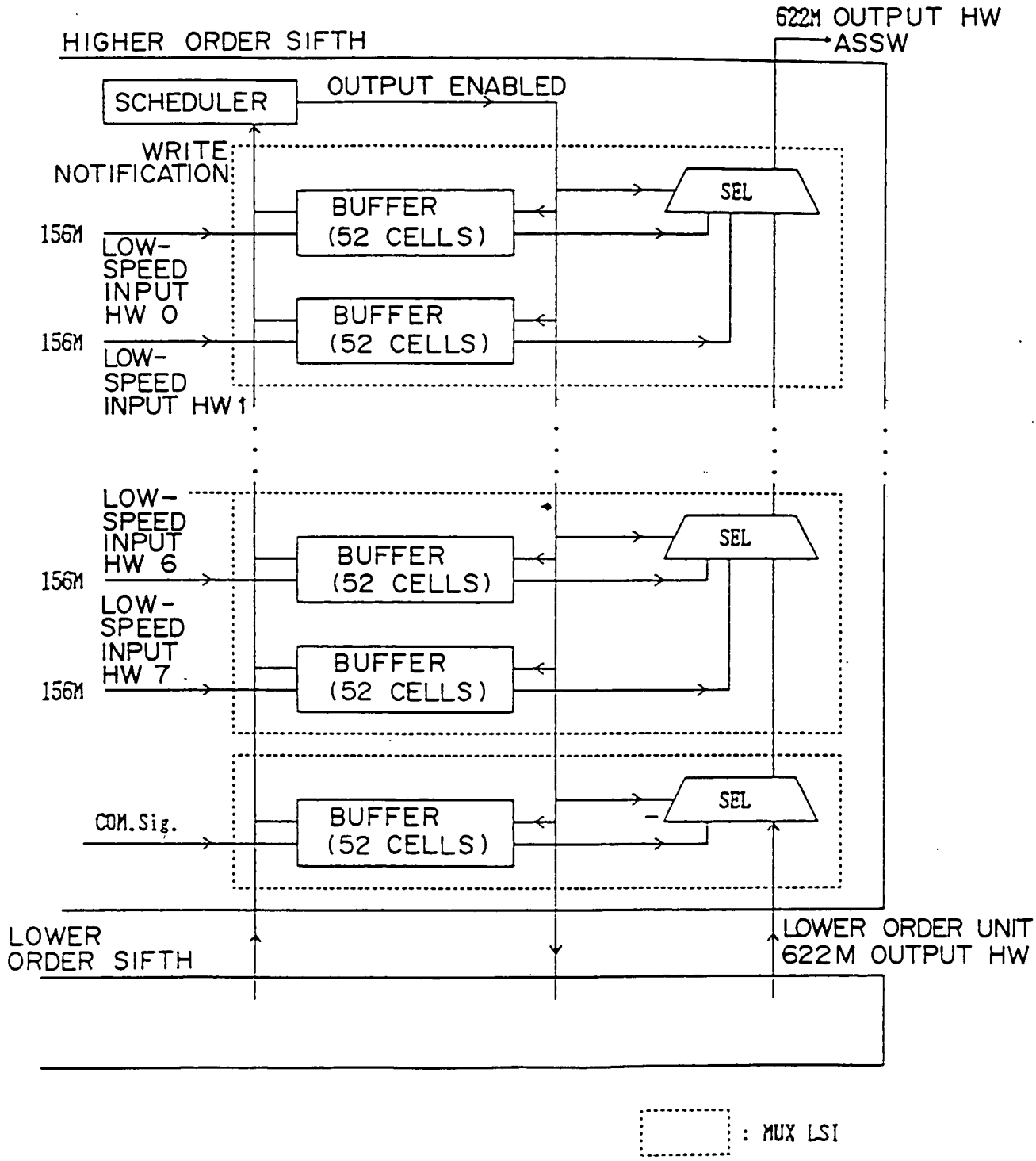

HIGHER ORDER SIFTH
622M OUTPUT HW
ASSW
SCHEDULER
OUTPUT ENABLED
WRITE NOTIFICATION
156M
LOW-SPEED INPUT HW 0
156M
LOW-SPEED INPUT HW 1
BUFFER (52 CELLS)
BUFFER (52 CELLS)
SEL
LOW-SPEED INPUT HW 6
156M
LOW-SPEED INPUT HW 7
156M
BUFFER (52 CELLS)
BUFFER (52 CELLS)
SEL
COM.Sig.
BUFFER (52 CELLS)
SEL
LOWER ORDER SIFTH
LOWER ORDER UNIT 622M OUTPUT HW
: MUX LSI

FIG. 132

6692E0 ET2220

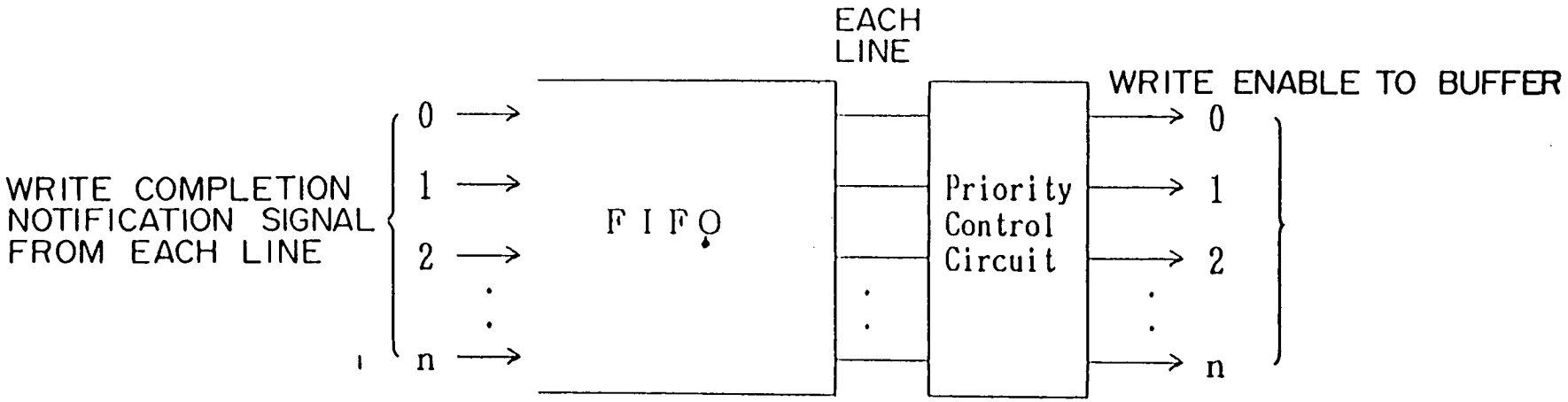
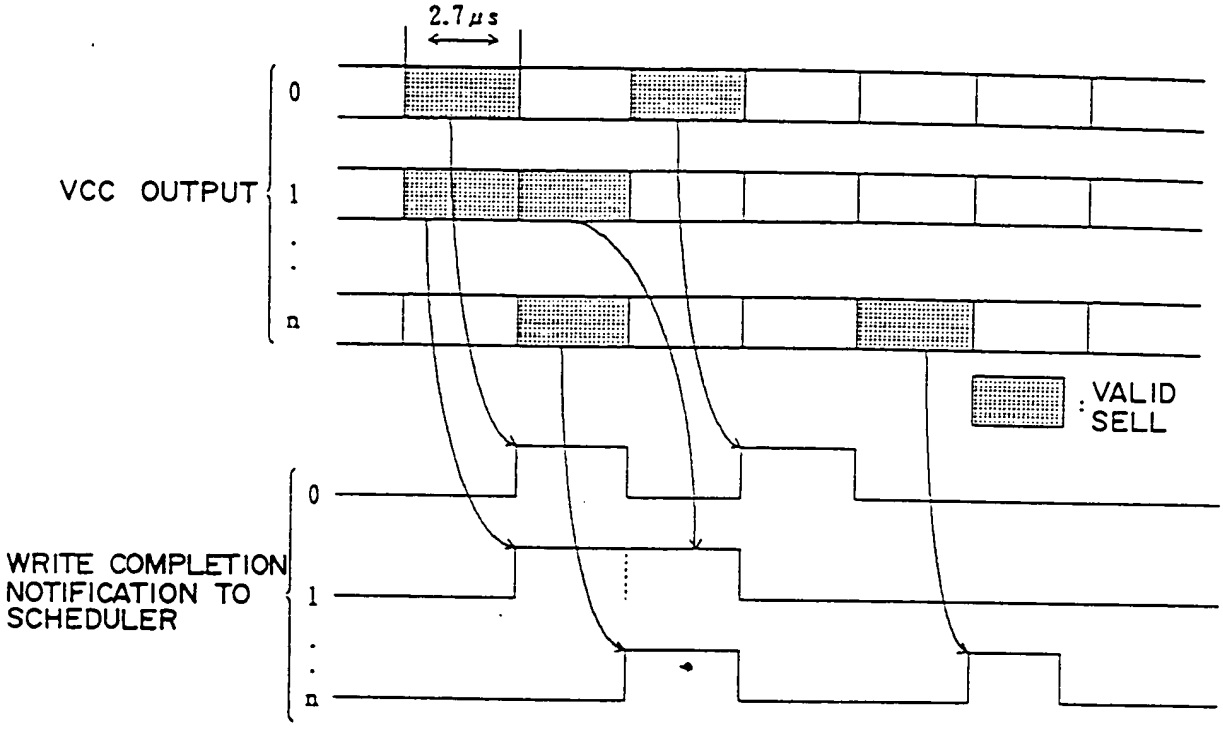


FIG. 133

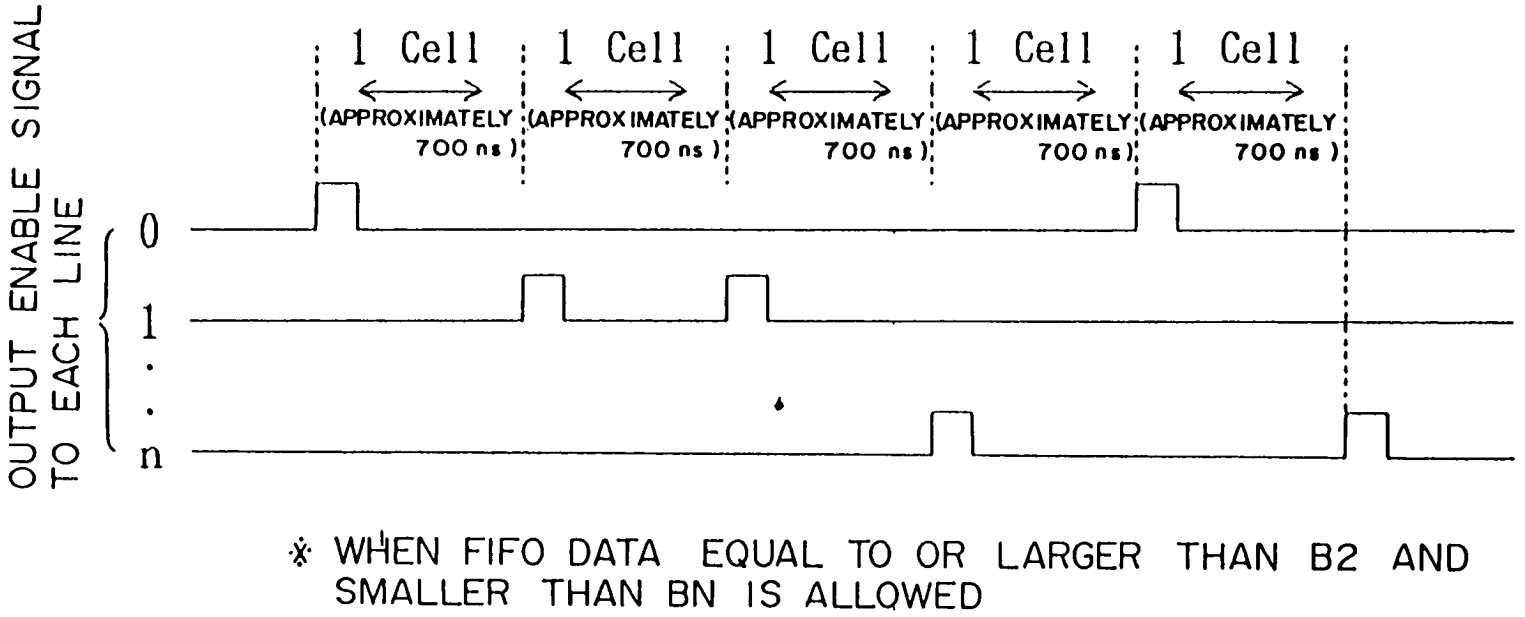


WRITE FIFO IN SCHEDULER

LINE	SCHEDULER FIFO	t6	t4	t3	t2	
0		0	1	0	1	b0
1		0	0	1	1	b1
:						:
n		1	0	1	0	bn

※ NO DATA IS WRITTEN TO FIFO AT TIMING AT WHICH NO CELLS EXIST IN ALL LINES.

FIG. 134



※ WHEN FIFO DATA EQUAL TO OR LARGER THAN B2 AND SMALLER THAN BN IS ALLOWED

FIG. 135

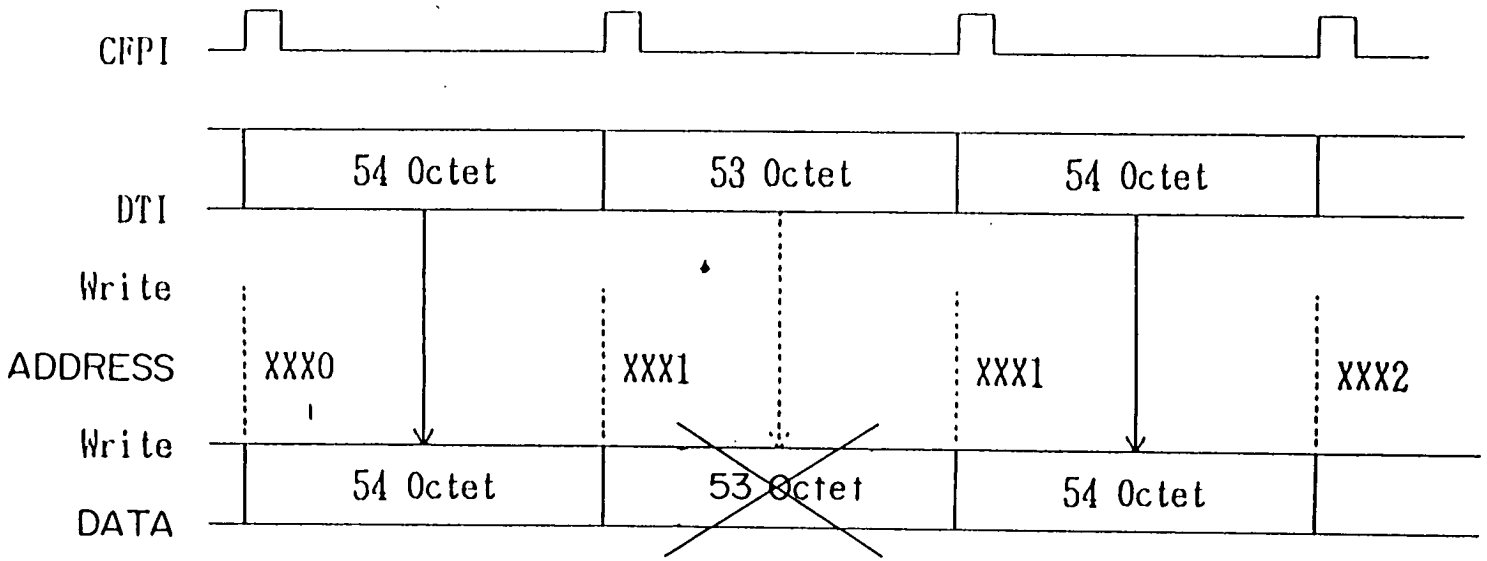

CFPI
DTI
54 Octet
53 Octet
54 Octet
Write
ADDRESS
XXX0
XXX1
XXX1
XXX2
Write
DATA
54 Octet
53 Octet
54 Octet

FIG. 136

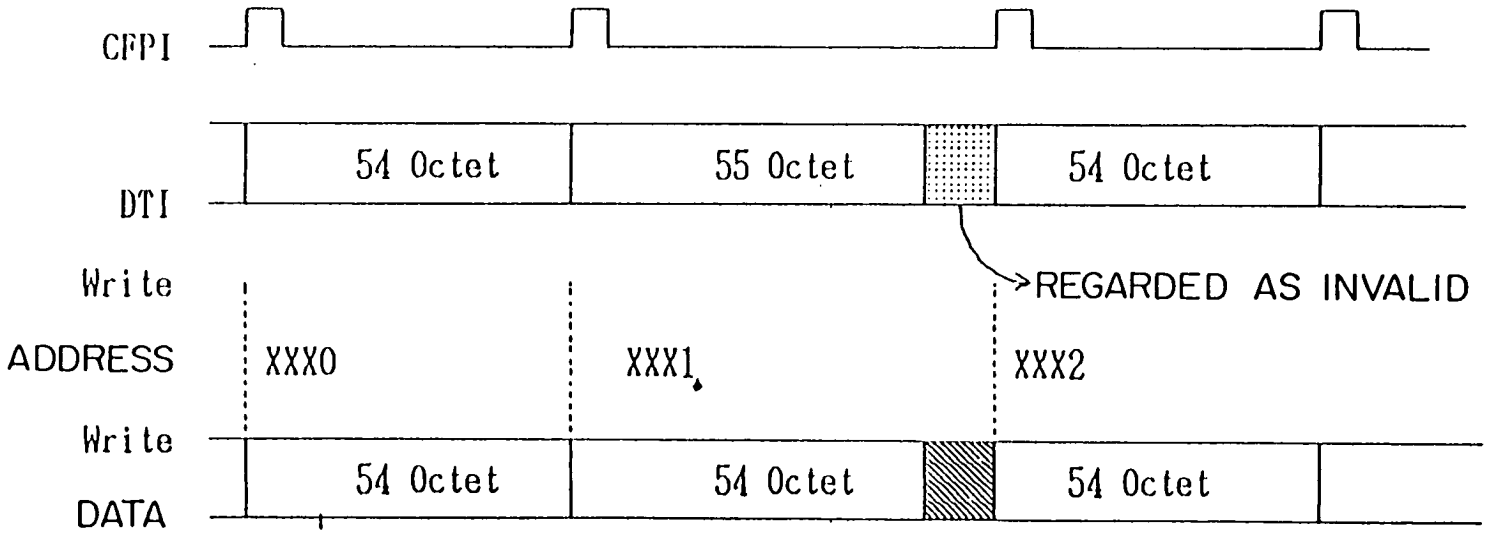

CPPI
DTI
54 Octet
55 Octet
54 Octet
REGARDED AS INVALID
Write
ADDRESS
XXX0
XXX1
XXX2
Write
DATA
54 Octet
54 Octet
54 Octet

FIG. 137

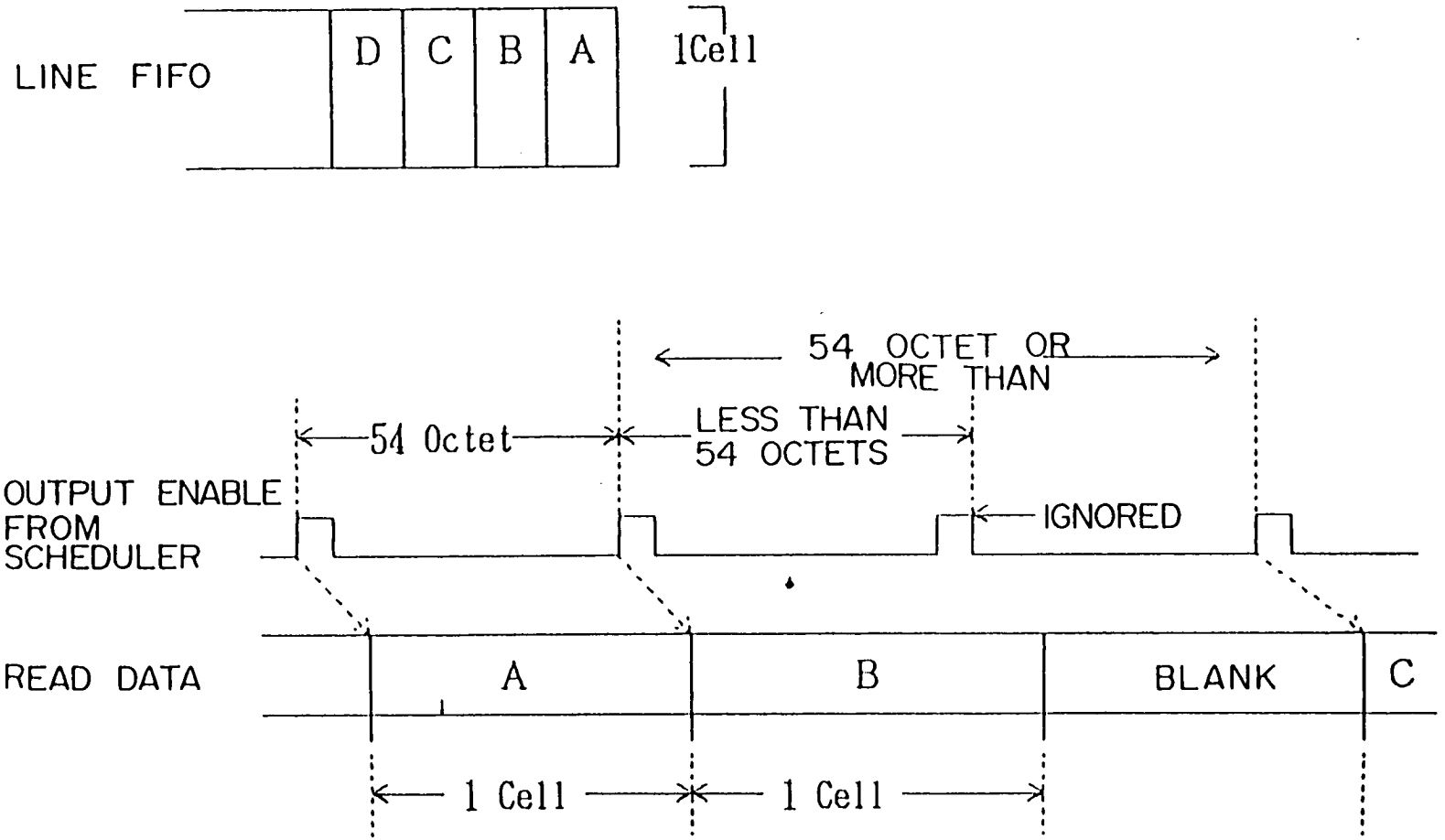
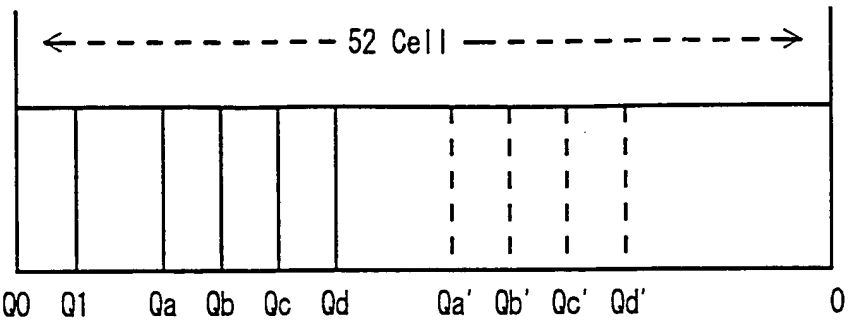

LINE FIFO
D
C
B
A
1Cell
54 OCTET OR MORE THAN
54 Octet
LESS THAN 54 OCTETS
OUTPUT ENABLE FROM SCHEDULER
IGNORED
READ DATA
A
B
BLANK
C
1 Cell
1 Cell

FIG. 138



Q0 : PHYSICAL MAXIMUM OF BUFFER
Q1 : PHYSICAL MAXIMUM OF BUFFER
Qa : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "0"
Qb : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "1"
Qc : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "0"
Qd : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "1"
Qa' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "0"
Qb' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "1"
Qc' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "0"
Qd' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "1"

FIG. 139

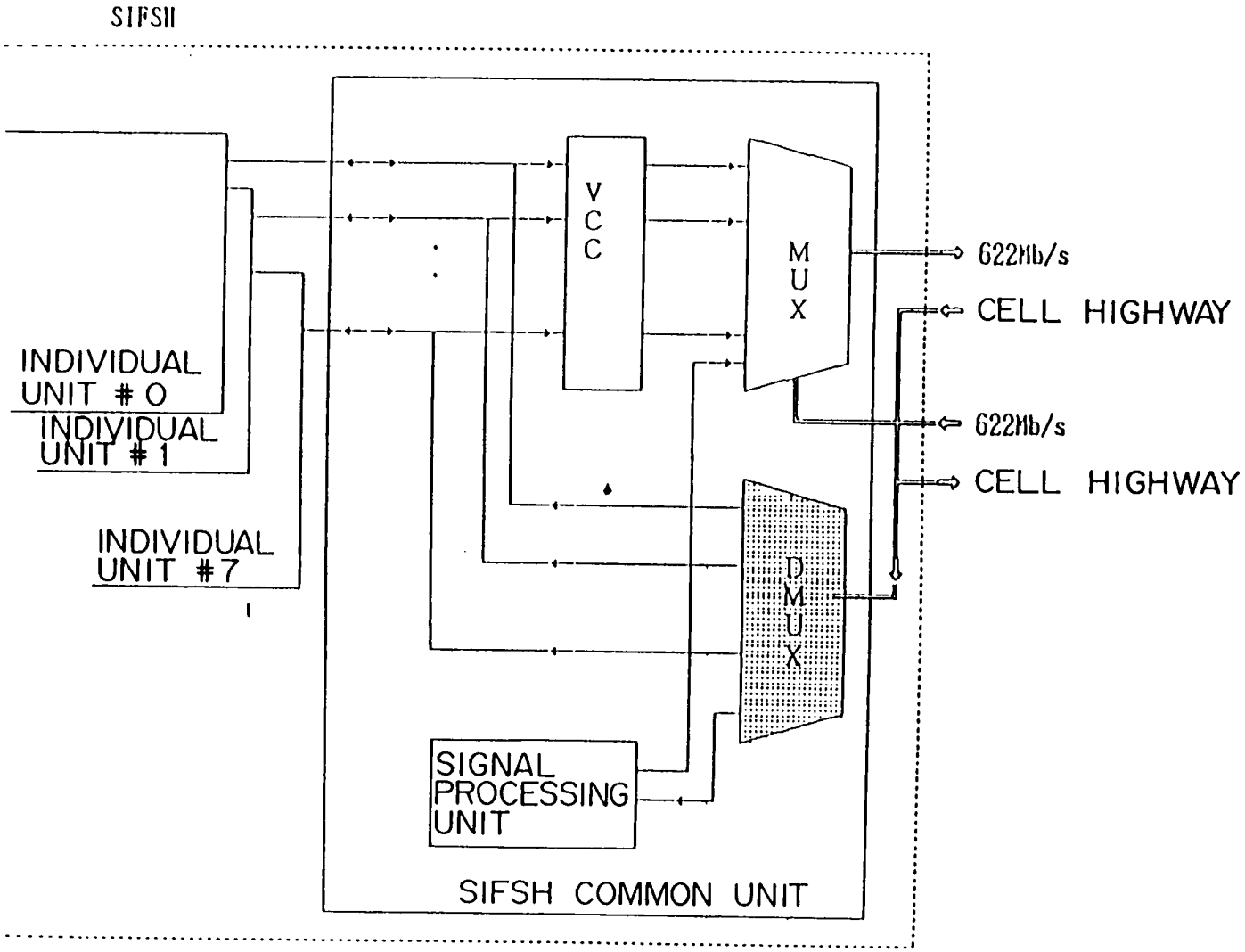

SIFSH
INDIVIDUAL UNIT # 0
INDIVIDUAL UNIT #1
INDIVIDUAL UNIT #7
VCC
MUX
DMUX
622Mb/s
CELL HIGHWAY
622Mb/s
CELL HIGHWAY
SIGNAL PROCESSING UNIT
SIFSH COMMON UNIT

FIG. 140

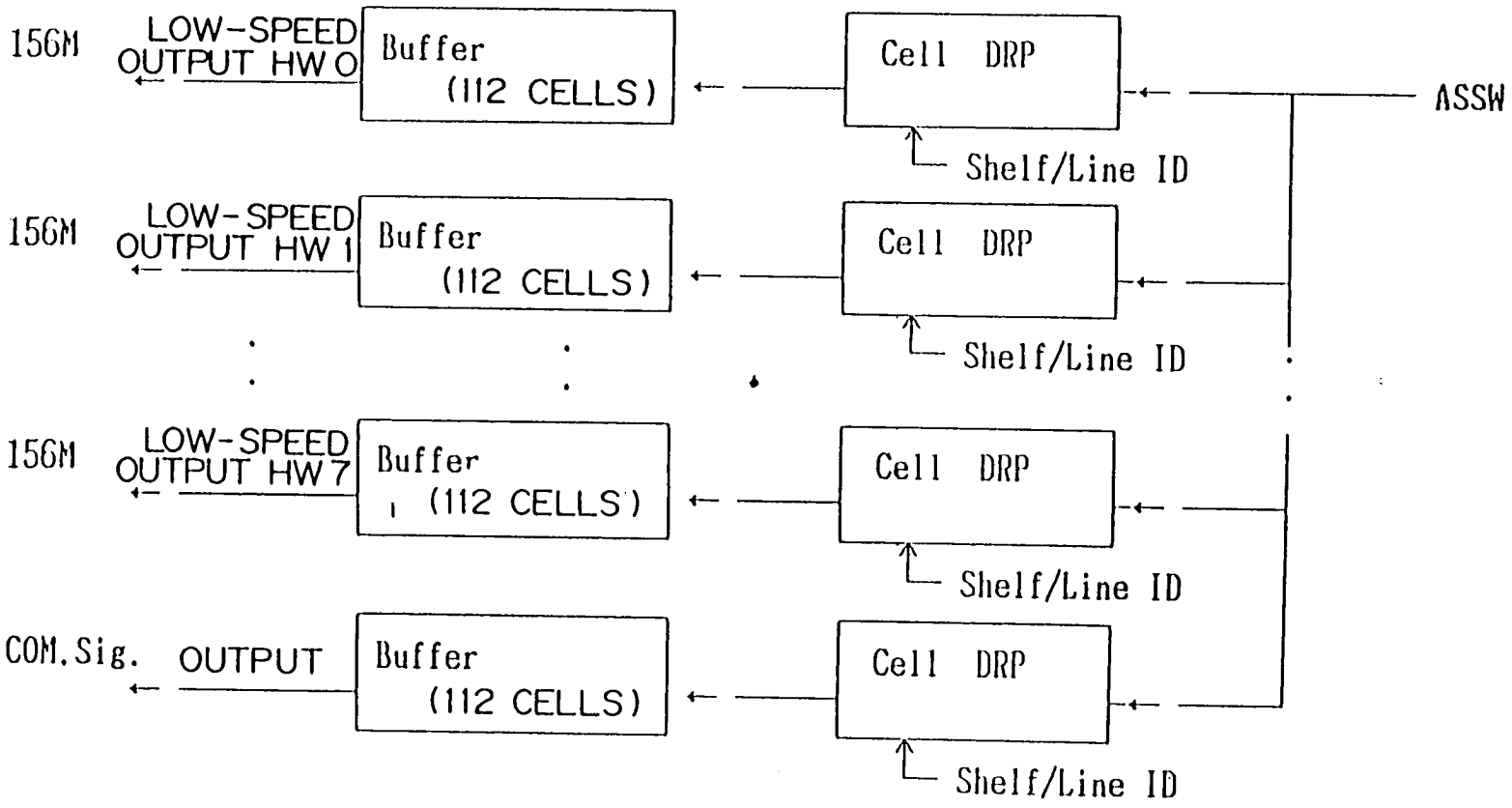
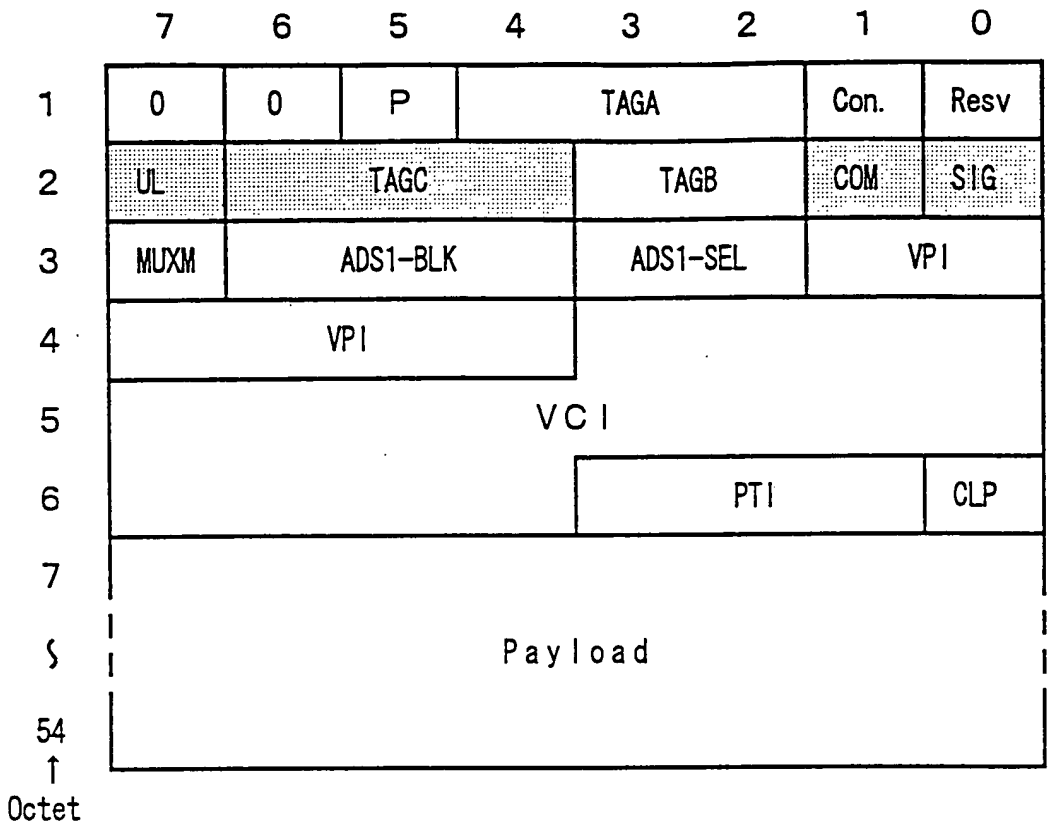

156M
LOW-SPEED OUTPUT HW 0
Buffer (112 CELLS)
Cell DRP
ASSW
Shelf/Line ID
156M
LOW-SPEED OUTPUT HW 1
Buffer (112 CELLS)
Cell DRP
Shelf/Line ID
156M
LOW-SPEED OUTPUT HW 7
Buffer (112 CELLS)
Cell DRP
Shelf/Line ID
COM. Sig.
OUTPUT
Buffer (112 CELLS)
Cell DRP
Shelf/Line ID

FIG. 141



"0" : ONE-TO-ONE COMMUNICATIONS MODE (NO COPY MODE)
O : INTERNAL TEST CELL INDICATOR
("0":USER CELL, "1":INTERNAL CELL)
P : QUALITY INDICATOR
CON : PRIORTY CLASS INDICATOR
RES : RESERVE BITS
PTI : PAYLOAD TYPE
TAGA : 2.4G 4×4 TAG
TAGB : 2.4G → 600M 4 HIGHWAY TAG
COM : SELECTING COMMON UNIT
SIG, UL, TAGC : TAG FOR SMALLER THAN 600M
MUXM : MUX MULTICAST
ADS1 BLK : TAG FROM MUX TO ADS1 BLOCK
ADS1 SEL : TAG TO ADS1
: USED IN SIFCOM DMUX

FIG. 142

SIG	UL	TAGC	COM	TRANSMISSION LINE
0/1	0	0 0 0	0	SIFSH0 Line # 0/Signal
0/1	0	0 0 1	0	〃 Line # 1/Signal
		⟆		⟆
0/1	0	1 1 1	0	SIFSH0 Line # 7/Signal
0/1	1	0 0 0	0	SIFSH1 Line # 0/Signal
0/1	1	0 0 1	0	〃 Line # 1/Signal
		⟆		
0/1	1	1 1 1	0	SIFSH1 Line # 7/Signal
1	0	0 0 0	1	SIFSH0 Common Signal
1	1	0 0 0	1	SIFSH1 Common Signal

FIG. 143

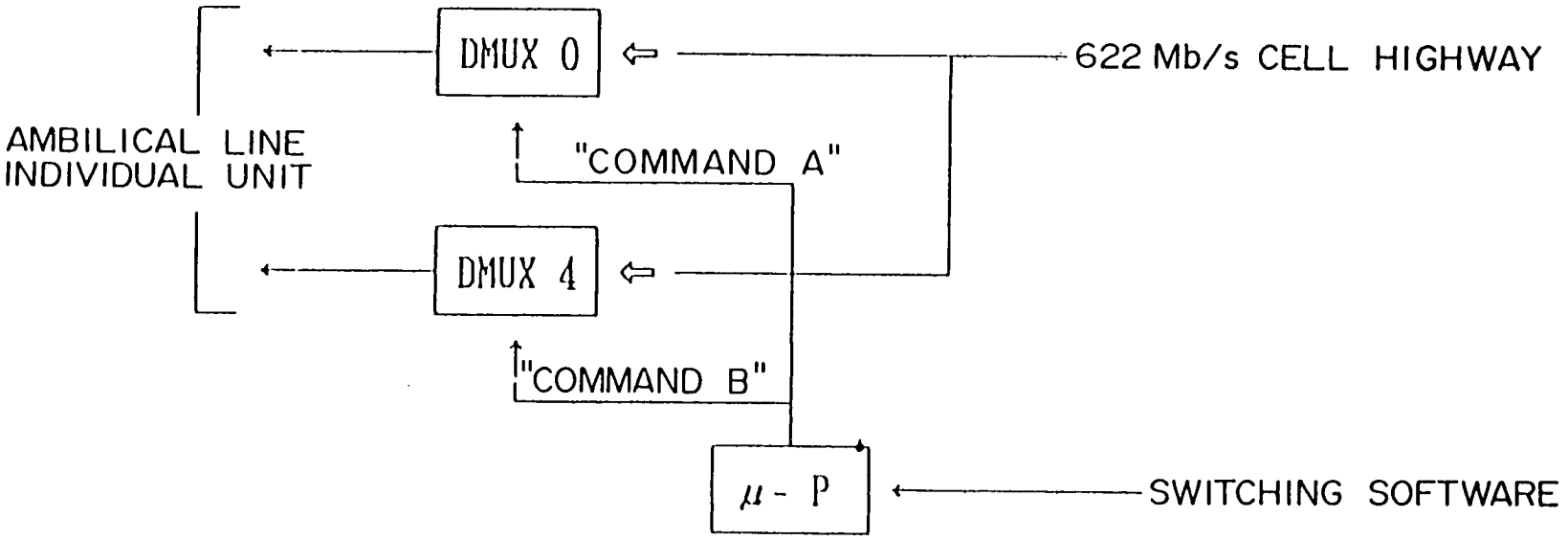
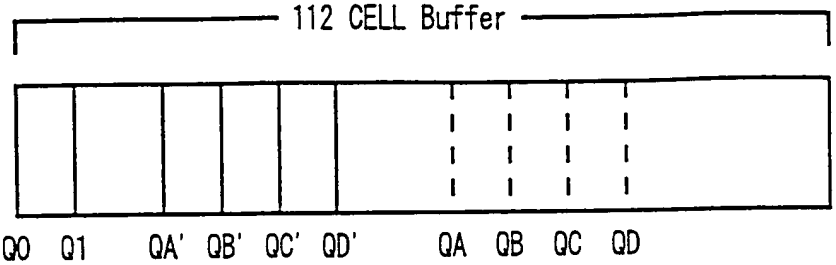

DMUX 0
622 Mb/s CELL HIGHWAY
AMBILICAL LINE
INDIVIDUAL UNIT
"COMMAND A"
DMUX 4
"COMMAND B"
μ - P
SWITCHING SOFTWARE

FIG. 144



Q0 : PHYSICALLY FULL
Q1 : PHYSICALLY FULL
QA : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "0"
QB : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "1"
QC : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "0"
QD : CELL DISCARD PROCESS STARTING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "1"
QA' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "0"
QB' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "0" , "CON" BIT= "1"
QC' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "0"
QD' : CELL DISCARD PROCESS RELEASING THRESHOLD OF CELL HAVING "P" BIT= "1" , "CON" BIT= "1"

FIG. 145

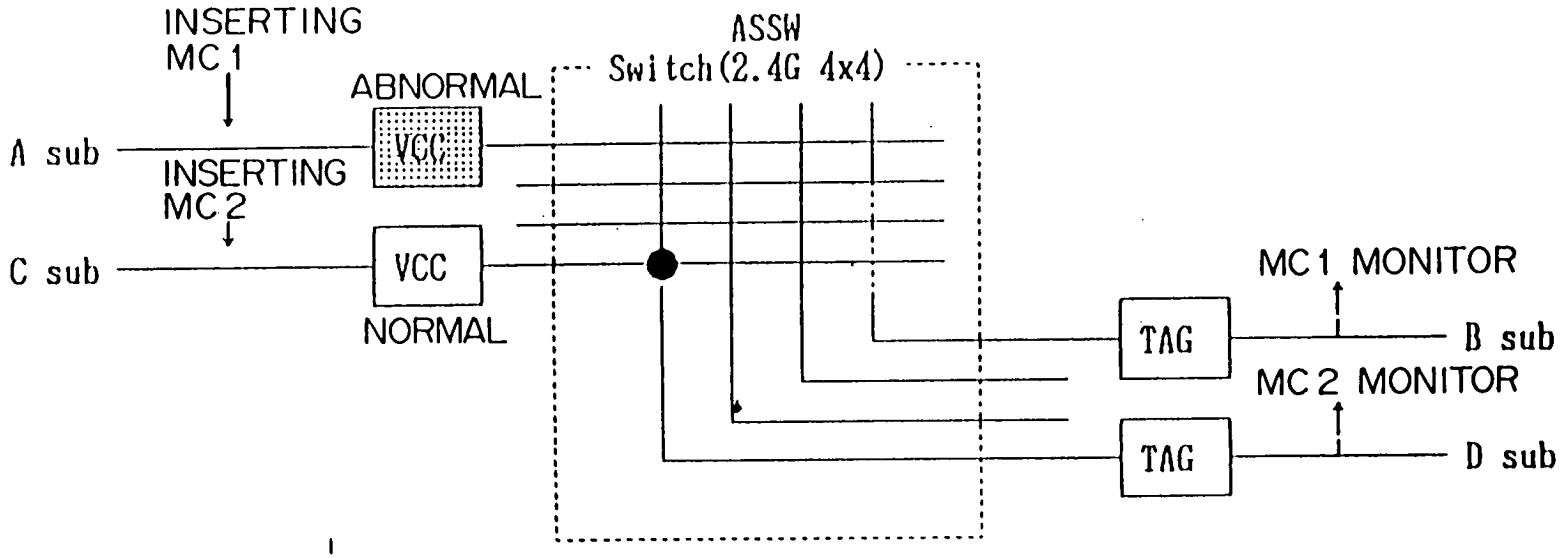

INSERTING
MC1
ABNORMAL
ASSW
Switch(2.4G 4x4)
A sub
VCC
INSERTING
MC2
C sub
VCC
NORMAL
MC1 MONITOR
TAG
B sub
MC2 MONITOR
TAG
D sub

FIG. 146

6692E0 ET2726O

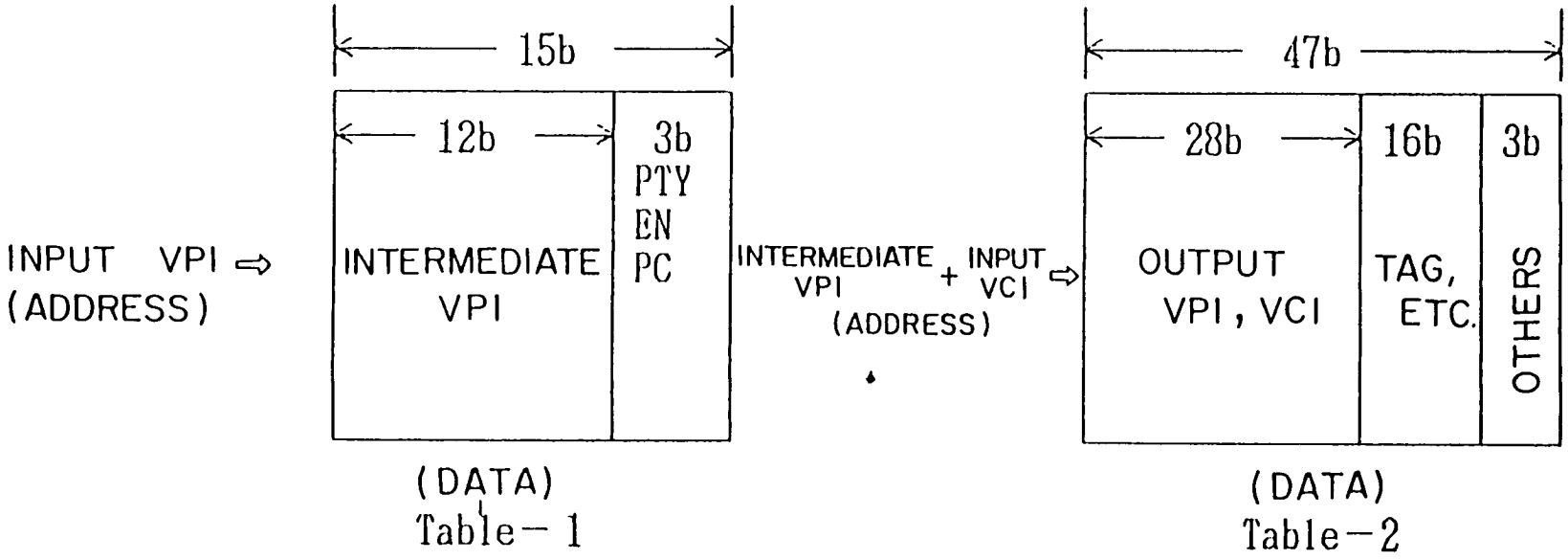


FIG. 147

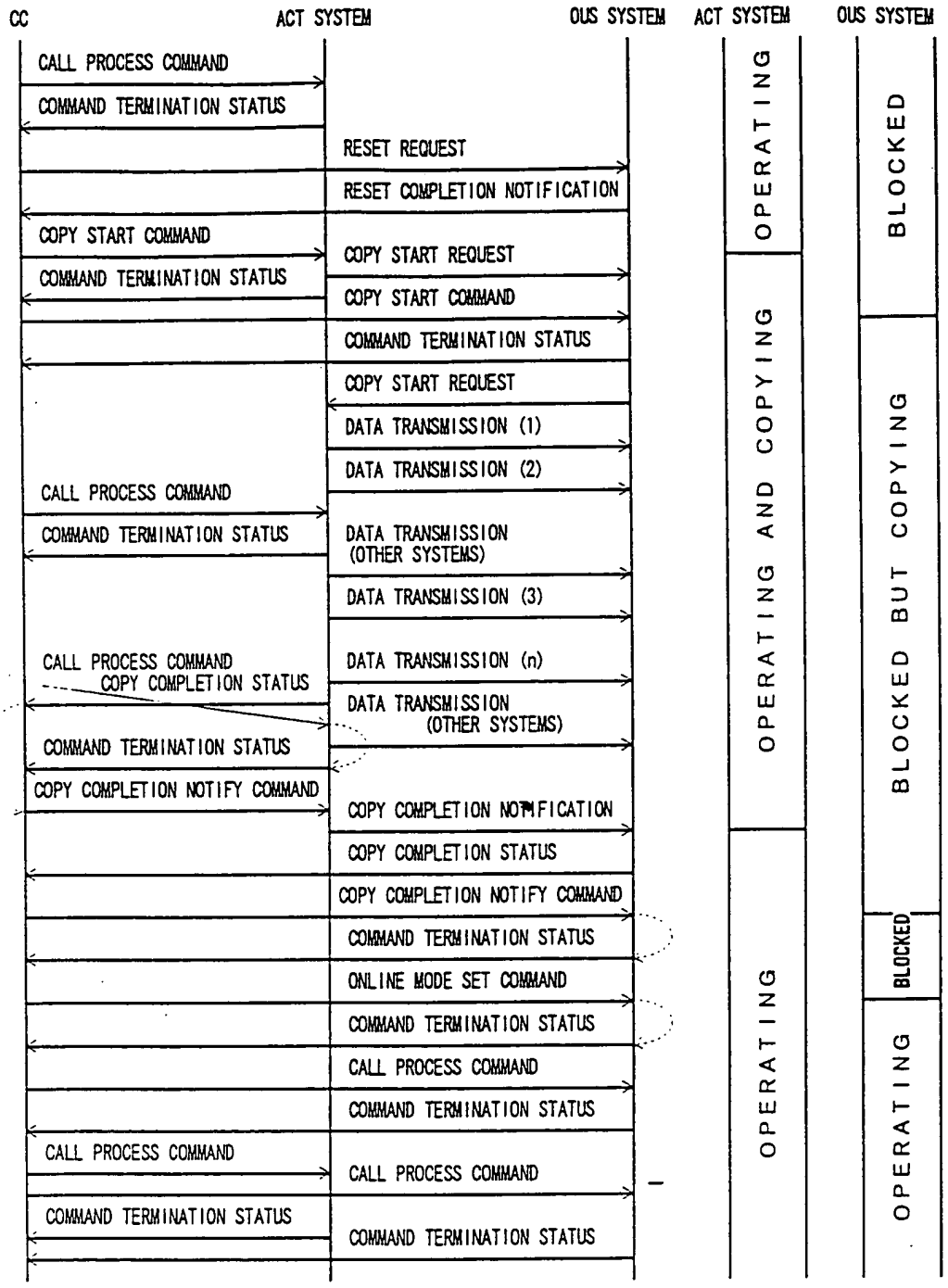

CC
ACT SYSTEM
OUS SYSTEM
ACT SYSTEM
OUS SYSTEM
CALL PROCESS COMMAND
COMMAND TERMINATION STATUS
RESET REQUEST
RESET COMPLETION NOTIFICATION
COPY START COMMAND
COPY START REQUEST
COMMAND TERMINATION STATUS
COPY START COMMAND
COMMAND TERMINATION STATUS
COPY START REQUEST
DATA TRANSMISSION (1)
DATA TRANSMISSION (2)
CALL PROCESS COMMAND
COMMAND TERMINATION STATUS
DATA TRANSMISSION (OTHER SYSTEMS)
DATA TRANSMISSION (3)
CALL PROCESS COMMAND
COPY COMPLETION STATUS
DATA TRANSMISSION (n)
DATA TRANSMISSION (OTHER SYSTEMS)
COMMAND TERMINATION STATUS
COPY COMPLETION NOTIFY COMMAND
COPY COMPLETION NOTIFICATION
COPY COMPLETION STATUS
COPY COMPLETION NOTIFY COMMAND
COMMAND TERMINATION STATUS
ONLINE MODE SET COMMAND
COMMAND TERMINATION STATUS
CALL PROCESS COMMAND
COMMAND TERMINATION STATUS
CALL PROCESS COMMAND
CALL PROCESS COMMAND
COMMAND TERMINATION STATUS
COMMAND TERMINATION STATUS
OPERATING
OPERATING AND COPYING
OPERATING
BLOCKED
BLOCKED BUT COPYING
BLOCKED
OPERATING

FIG. 148

ACT SYSTEM STATUS	OUS SYSTEM STATUS	IS COPY ALLOWED ?	PROCESS OF CC
COPY CIMPLETION REPORT	COPY CIMPLETION REPORT	○	COPY COMPLETION COTIFICATION COMMAND IS ISSUED TO ACT SYSTEM AND OUS SYSTEM.
COPY CIMPLETION REPORT	COPY DISABLED OR NOT REPORTED	×	COPY COMPLETION NOTIFICATION COMMAND IS ISSUED TO ACT SYSTEM. OUT SYSTEM IS RESET AND RETRIED. IF RETRY IS ALLOWED, VCC IS INDIVIDUALLY SET IN OUS SYSTEM.
COPY DISABLED OR NOT REPORTED	COPY CIMPLETION REPORT	×	
COPY DISABLED OR NOT REPORTED	COPY DISABLED OR NOT REPORTED	×	

FIG. 149

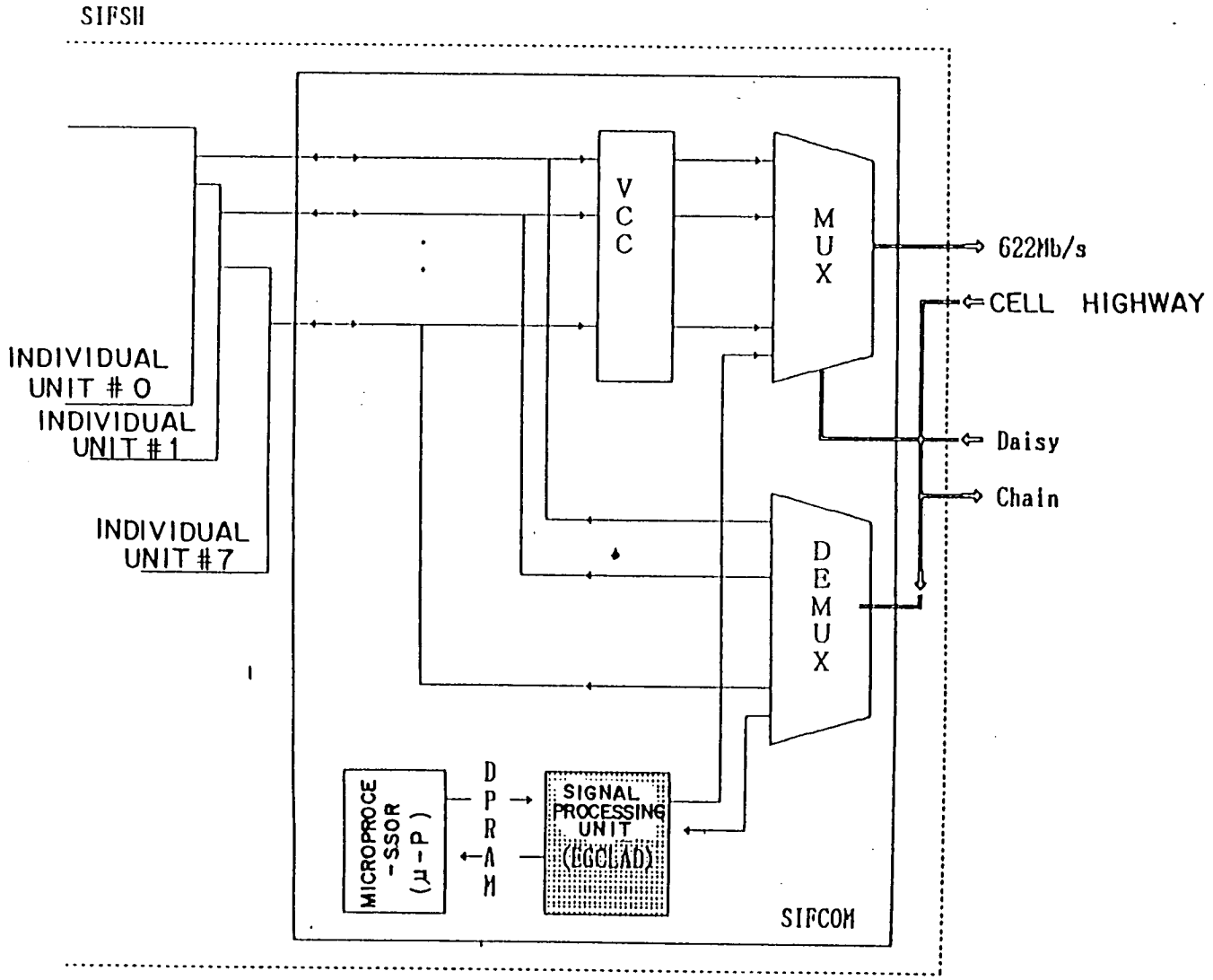
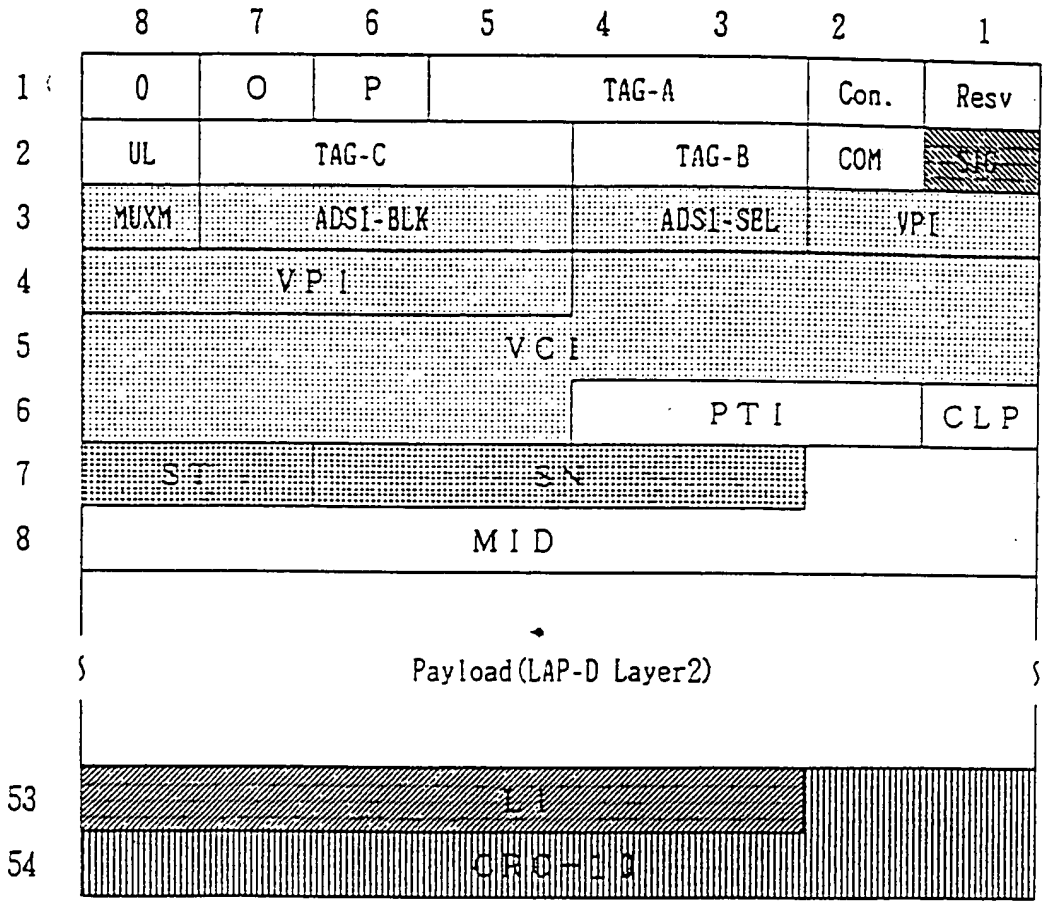

SIFSH
INDIVIDUAL UNIT # 0
INDIVIDUAL UNIT #1
INDIVIDUAL UNIT #7
VCC
MUX
DEMUX
622Mb/s
CELL HIGHWAY
Daisy
Chain
MICROPROCE -SSOR (μ-P)
DPRAM
SIGNAL PROCESSING UNIT (EGCLAD)
SIFCOM

FIG. 150



: SIGNALLING BIT CHECK AREA
: VPI / VCI MATCHING-DETECTION AREA
: SEQUENCE CHECK AREA
: FRAME CHECK AREA
: CRC CHECK AREA

FIG. 151

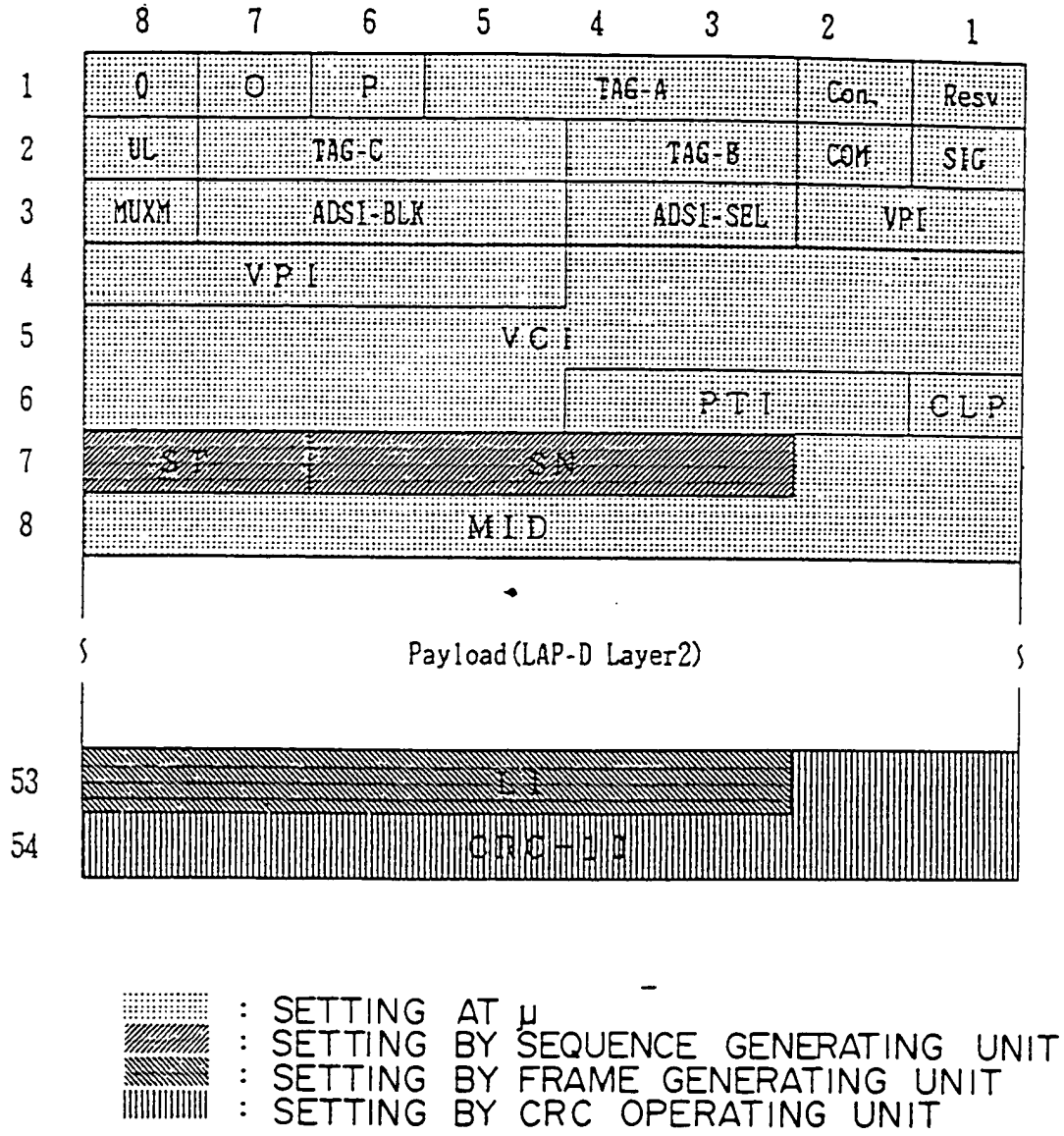

8 7 6 5 4 3 2 1
1 0 0 P TAG-A Con. Resv
2 UL TAG-C TAG-B COM SIG
3 MUXM ADSI-BLK ADSI-SEL VPI
4 VPI
5 VCI
6 PTI CLP
7 SN
8 MID
Payload(LAP-D Layer2)
53
54
: SETTING AT μ
: SETTING BY SEQUENCE GENERATING UNIT
: SETTING BY FRAME GENERATING UNIT
: SETTING BY CRC OPERATING UNIT

FIG. 152

669260 EP2726060

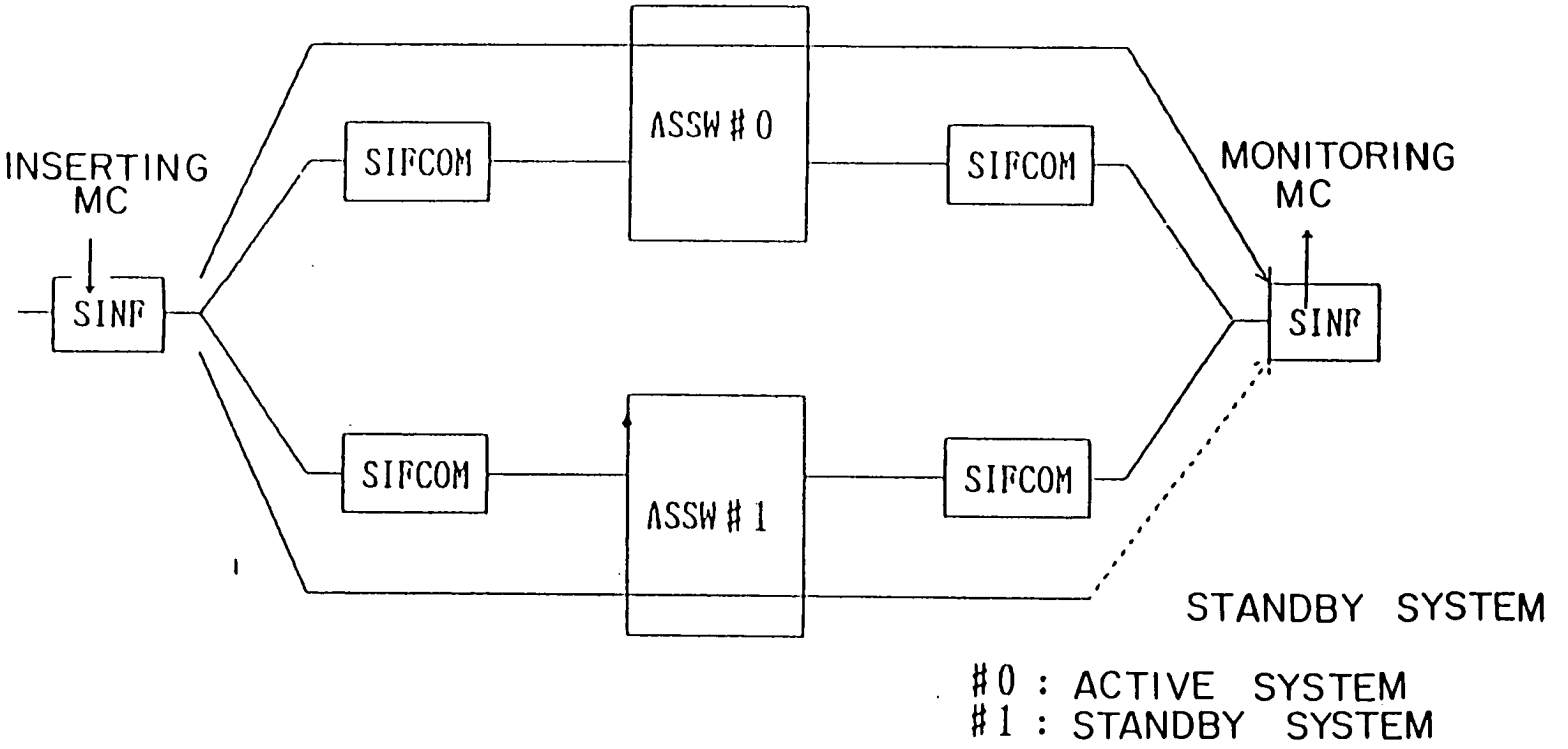


FIG. 153

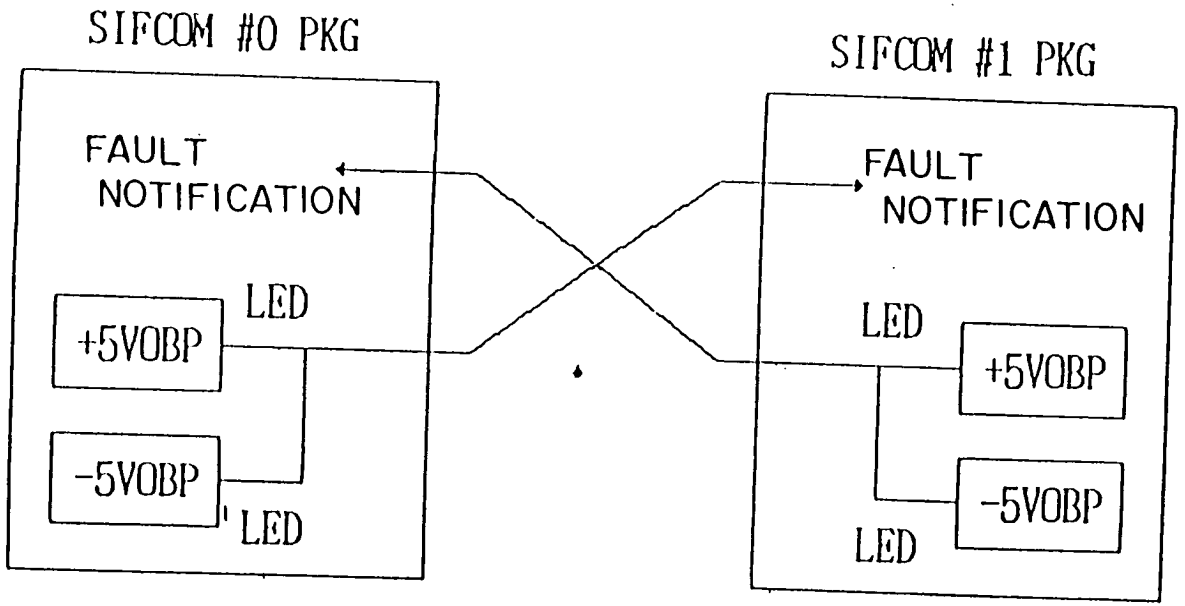

SIFCOM #0 PKG
FAULT NOTIFICATION
LED
+5VOBP
-5VOBP
LED
SIFCOM #1 PKG
FAULT NOTIFICATION
LED
+5VOBP
-5VOBP
LED

FIG. 155

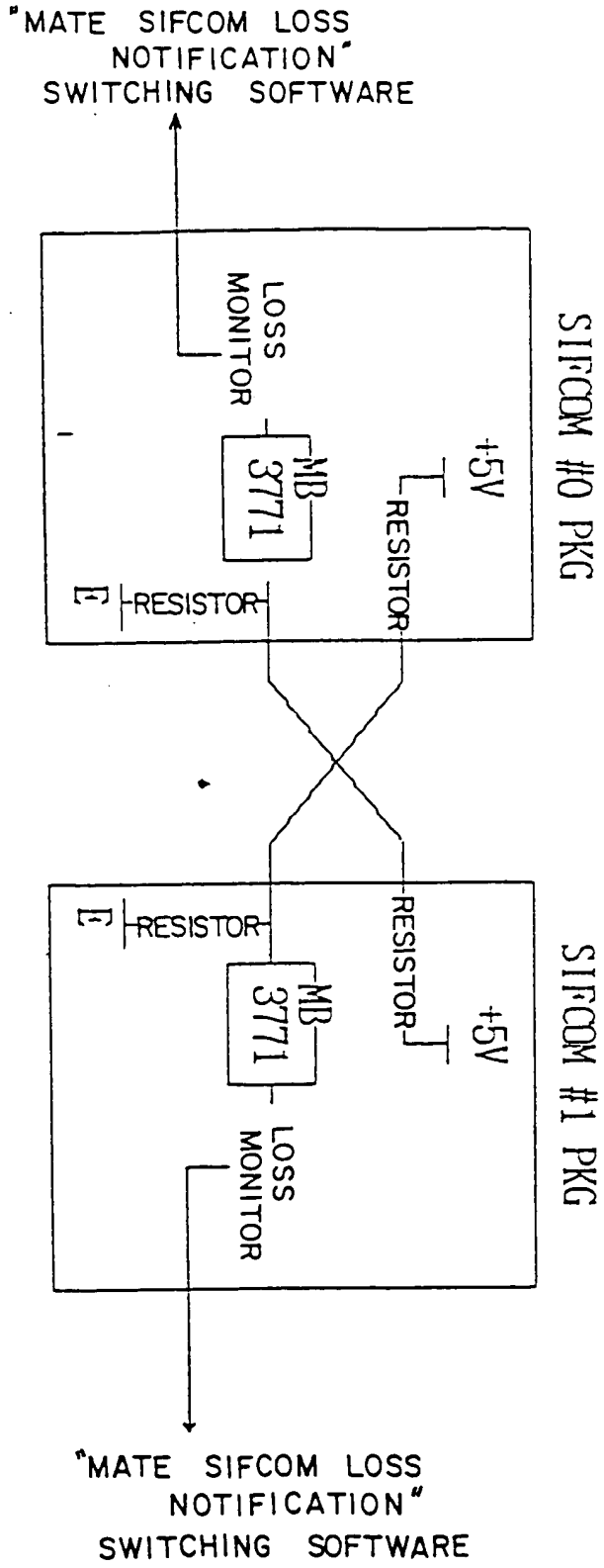

"MATE SIFCOM LOSS NOTIFICATION" SWITCHING SOFTWARE
LOSS MONITOR
MB 3771
+5V
RESISTOR
RESISTOR
SIFCOM #0 PKG
RESISTOR
RESISTOR
MB 3771
+5V
LOSS MONITOR
SIFCOM #1 PKG
"MATE SIFCOM LOSS NOTIFICATION" SWITCHING SOFTWARE

FIG. 156

6698260 "ET22260

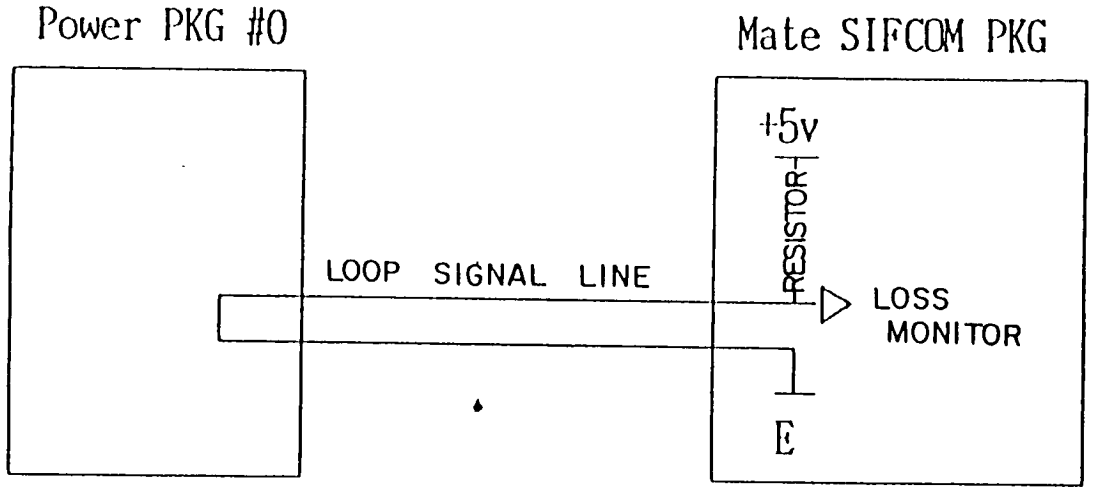


FIG. 157

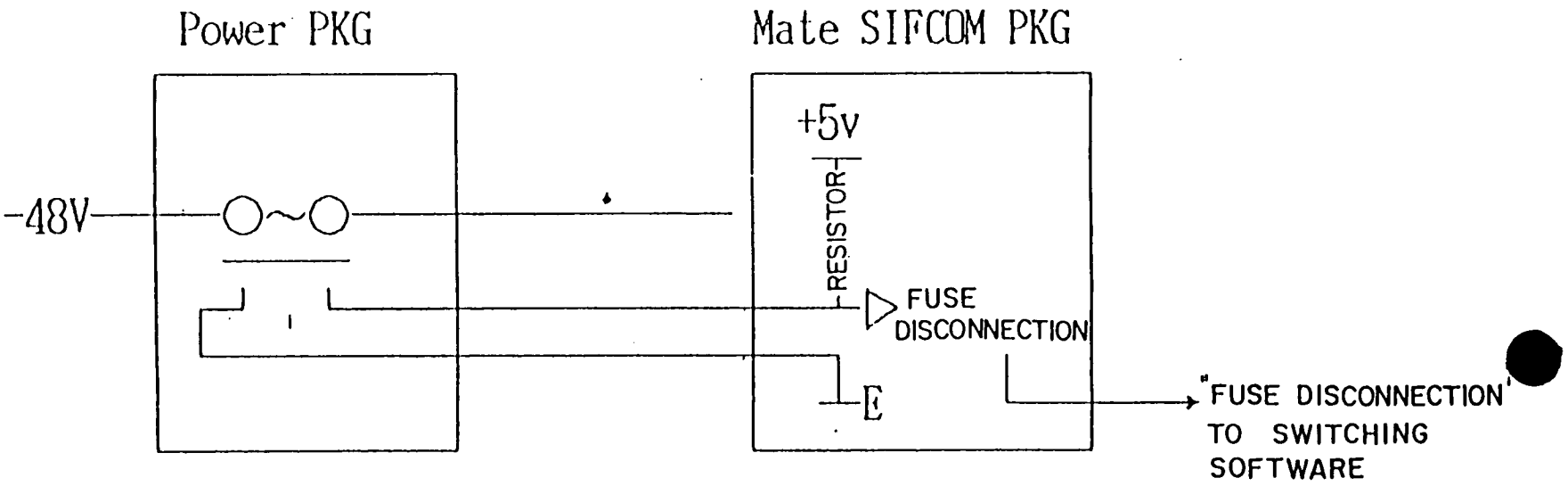

Power PKG
Mate SIFCOM PKG
-48V
+5v
RESISTOR
FUSE
DISCONNECTION
E
"FUSE DISCONNECTION"
TO SWITCHING
SOFTWARE

FIG. 158

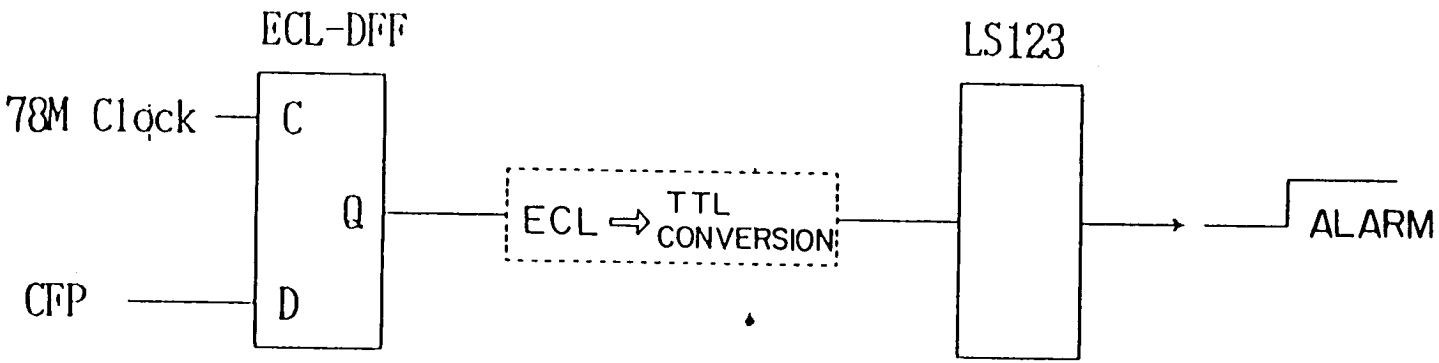


FIG. 159

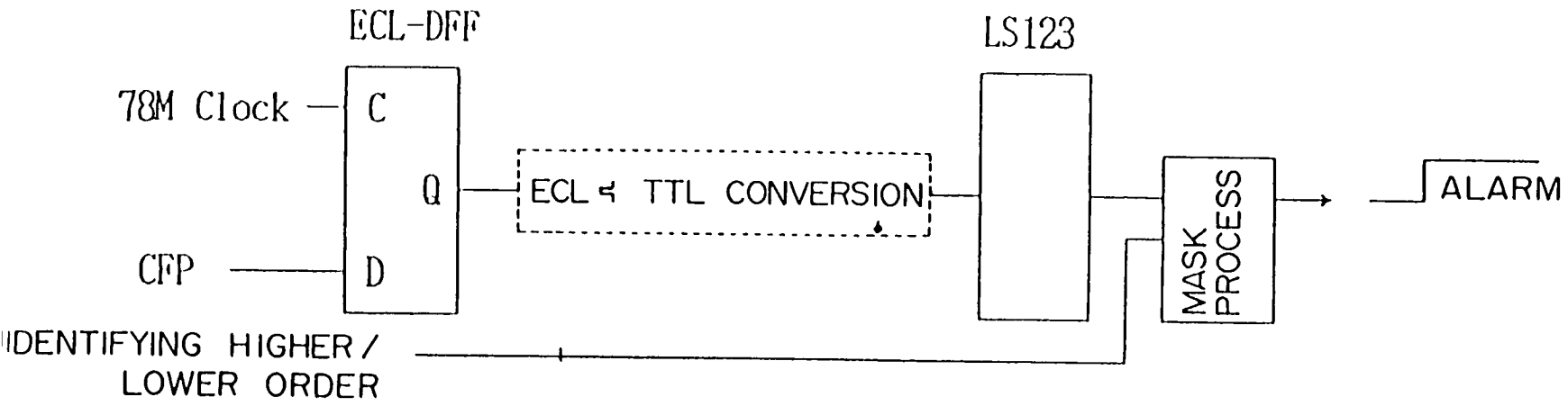

ECL-DFF
LS123
78M Clock
C
Q
CFP
D
ECL ⊰ TTL CONVERSION
MASK PROCESS
ALARM
IDENTIFYING HIGHER / LOWER ORDER

FIG. 160

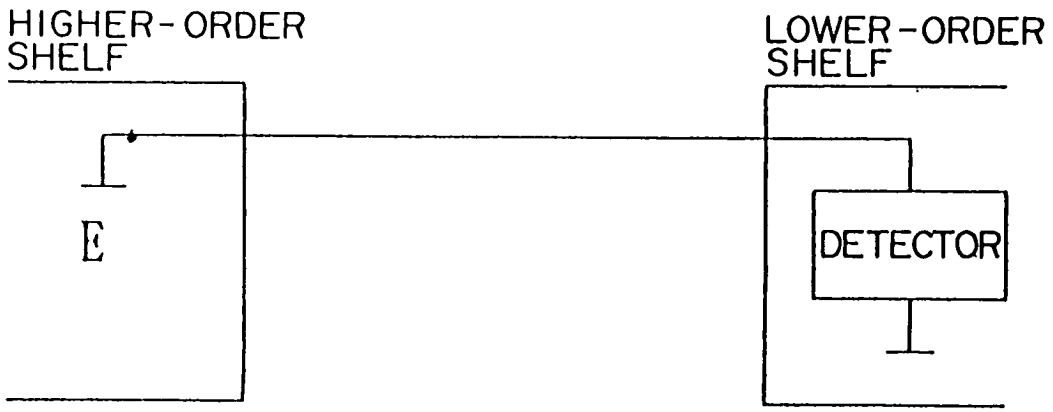


FIG. 161

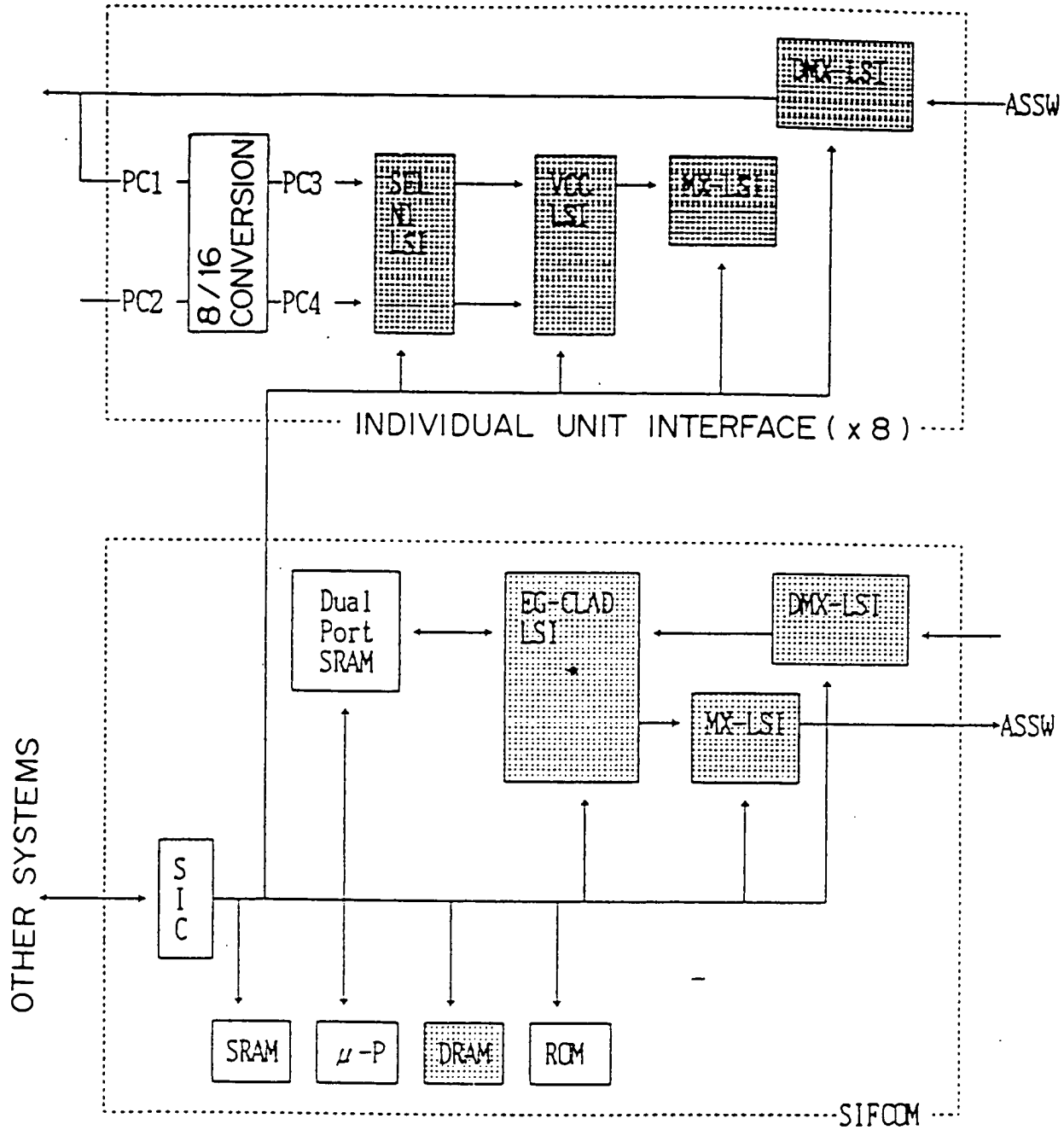

MX-LSI
ASSW
PC1
PC2
8/16 CONVERSION
PC3
PC4
SEL NL LSI
VCC LSI
MX-LSI
INDIVIDUAL UNIT INTERFACE (x 8)
Dual Port SRAM
EG-CLAD LSI
DMX-LSI
MX-LSI
ASSW
OTHER SYSTEMS
S I C
SRAM
μ-P
DRAM
ROM
SIFCOM

FIG. 162

FAULT POINT	DETECTION LOGIC AND DETECTION POINT	FAULT NOTIFICATION	DETECTION CYCLE
OBP FAULT, CLOCK DISCONNECTION, REF. CLOLK DISCONNECTION, WATCH DOG OVERFLOW	MATE SYSTEM SIFCOM FIRMWARE MONITORS PERIODCALLY.	REPORTED FROM SOFTWARE OF MATE SIFCOM	
PARITY ERROR DURING VCC COPY	ACT SYSTEM SIFCOM FIRMWARE MONITORS CONSTANTLY.	REPORTED FROM SOFTWARE OF ACT SYSTEM SIFCOM.	
INDIVIDUAL INTERFACE UNIT HARDWARE FAULT	HOME SYSTEM SIFCOM FIRMWARE MONITORS PERIODICALLY.	REPORTED FROM SOFTWARE OF HOME SYSTEM SIFCOM.	1sec × 2
COMMON UNIT HARDWARE FAULT	HOME SYSTEM SIFCOM FIRMWARE MONITORS PERIODICALLY, AND NOTIFY MATE SYSTEM THROUGH SIC.	REPORTED FROM SOFTWARE OF BOTH SYSTEM SIFCOMS	250ms × 2
-48V DISCONNECTION (POWER PKG MISSING, AMPLIFIER CONNECTOR MISSING)	MATE SIFCOM PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF MATE SIFCOM	250ms × 2
-48V INDIVIDUAL UNIT FUSE DISCONNECTION	SIFCOMS OF BOTH SYSTEMS, PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF HOME SYSTEM SIFCOM.	250ms × 2
-48V COMMON UNIT FUSE DISCONNECTION	MATE SYSTEM SIFCOM PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF HOME SYSTEM SIFCOM.	250ms × 2
SIFCOM PKG MISSING	MATE SYSTEM SIFCOM PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF MATE SIFCOM	250ms × 2

FIG. 163

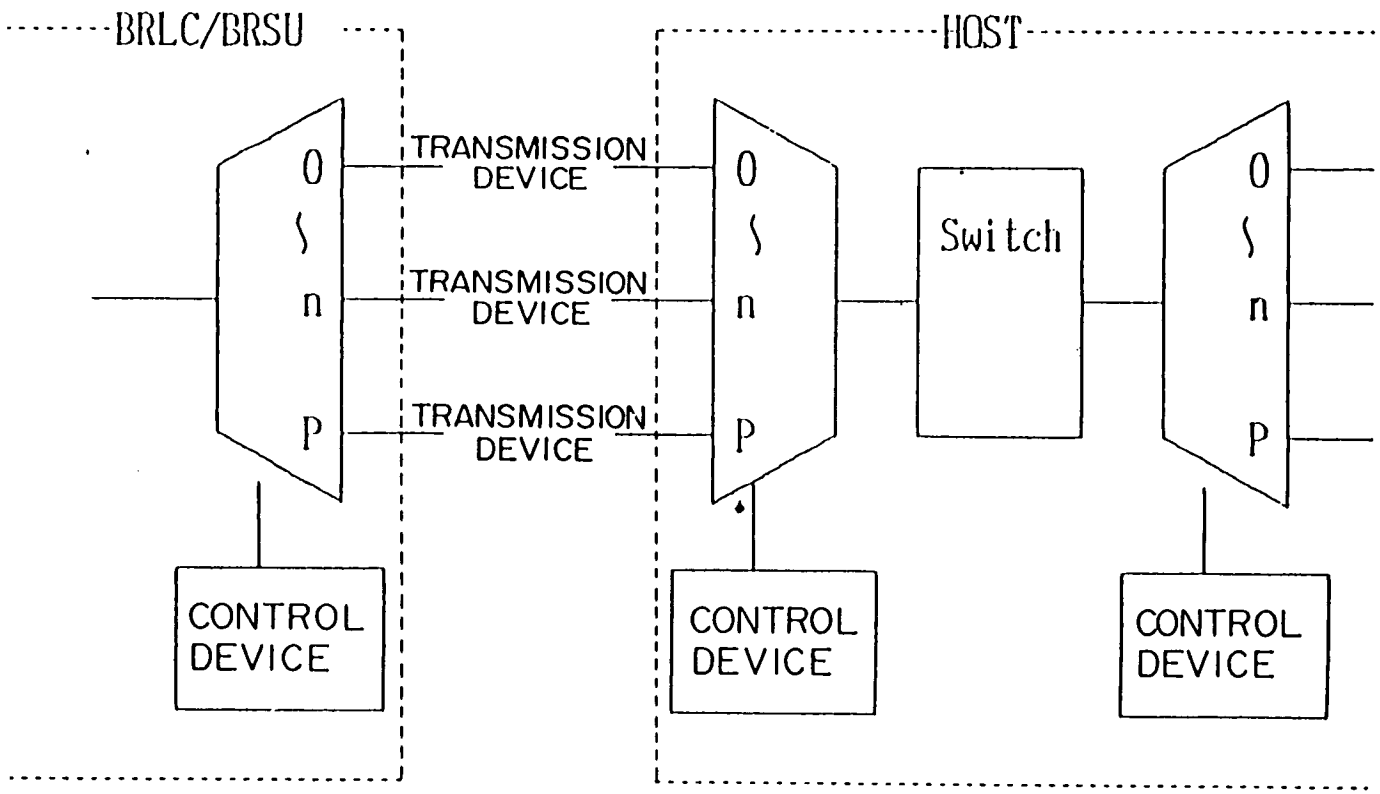

BRLC/BRSU
HOST
0
\
n
P
TRANSMISSION DEVICE
TRANSMISSION DEVICE
TRANSMISSION DEVICE
Switch
CONTROL DEVICE
CONTROL DEVICE
CONTROL DEVICE

FIG. 164

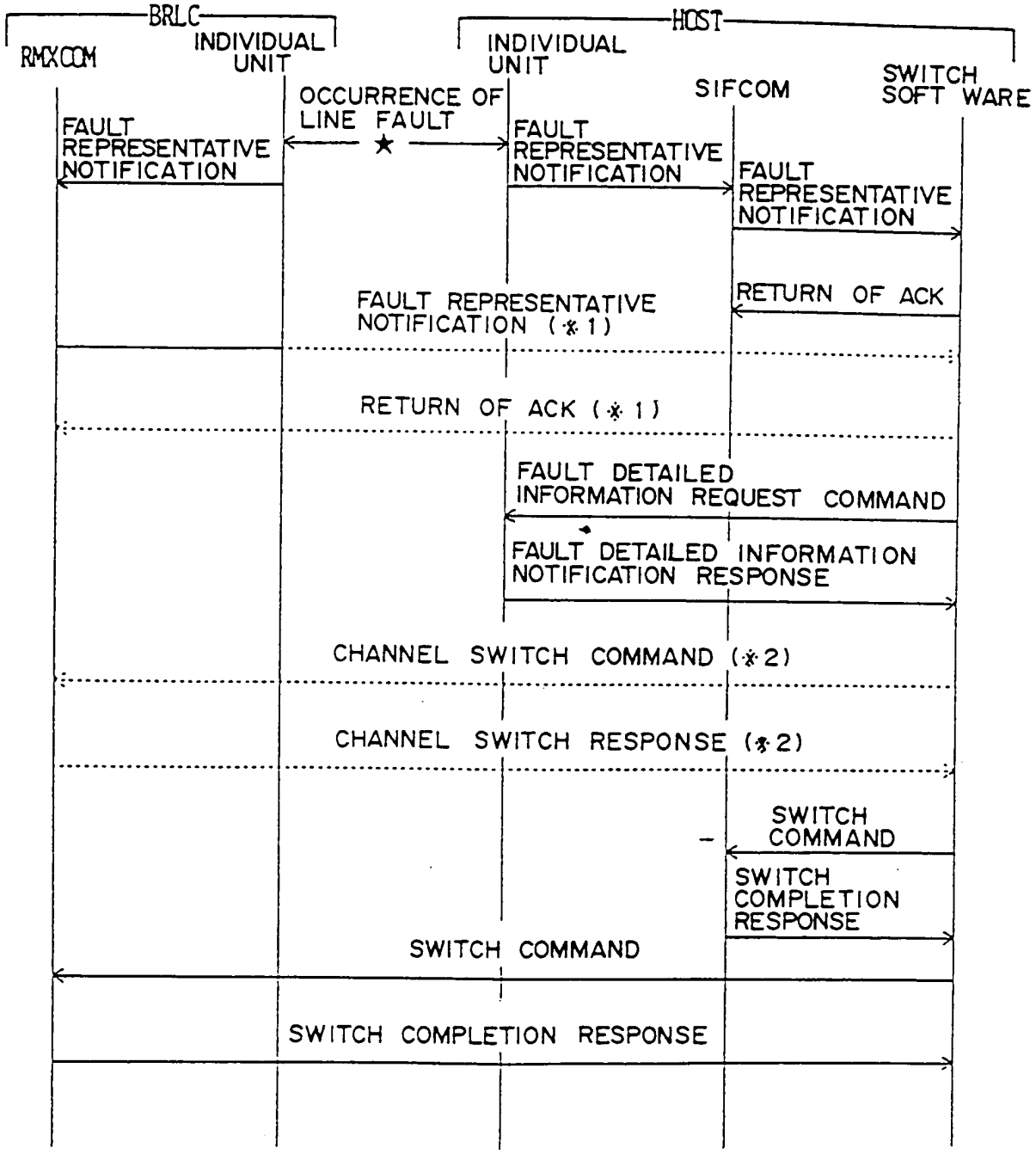
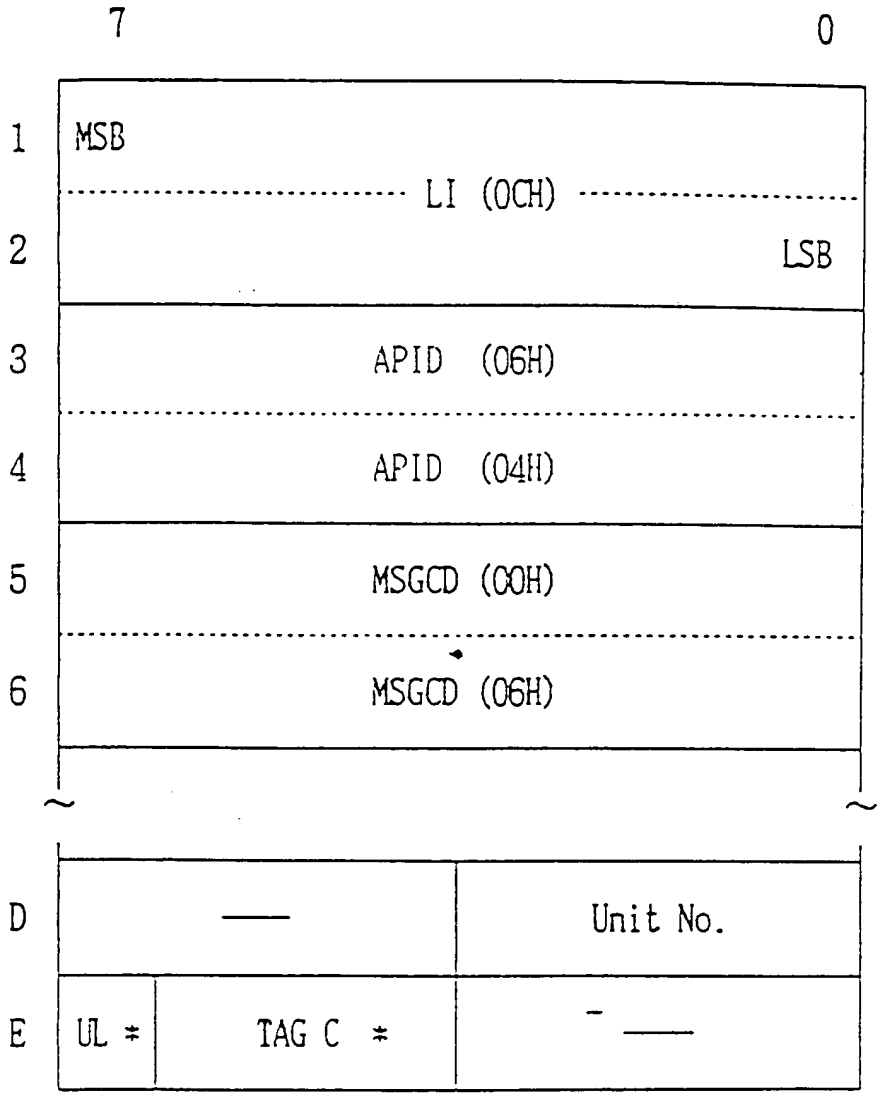

BRLC
HOST
RMXCOM
INDIVIDUAL UNIT
INDIVIDUAL UNIT
SIFCOM
SWITCH SOFT WARE
OCCURRENCE OF LINE FAULT
FAULT REPRESENTATIVE NOTIFICATION
FAULT REPRESENTATIVE NOTIFICATION
FAULT REPRESENTATIVE NOTIFICATION
RETURN OF ACK
FAULT REPRESENTATIVE NOTIFICATION (※1)
RETURN OF ACK (※1)
FAULT DETAILED INFORMATION REQUEST COMMAND
FAULT DETAILED INFORMATION NOTIFICATION RESPONSE
CHANNEL SWITCH COMMAND (※2)
CHANNEL SWITCH RESPONSE (※2)
SWITCH COMMAND
SWITCH COMPLETION RESPONSE
SWITCH COMMAND
SWITCH COMPLETION RESPONSE

FIG. 165



* : VALUES OF UL AND TAG-C TO BE CHANGED

FIG. 166

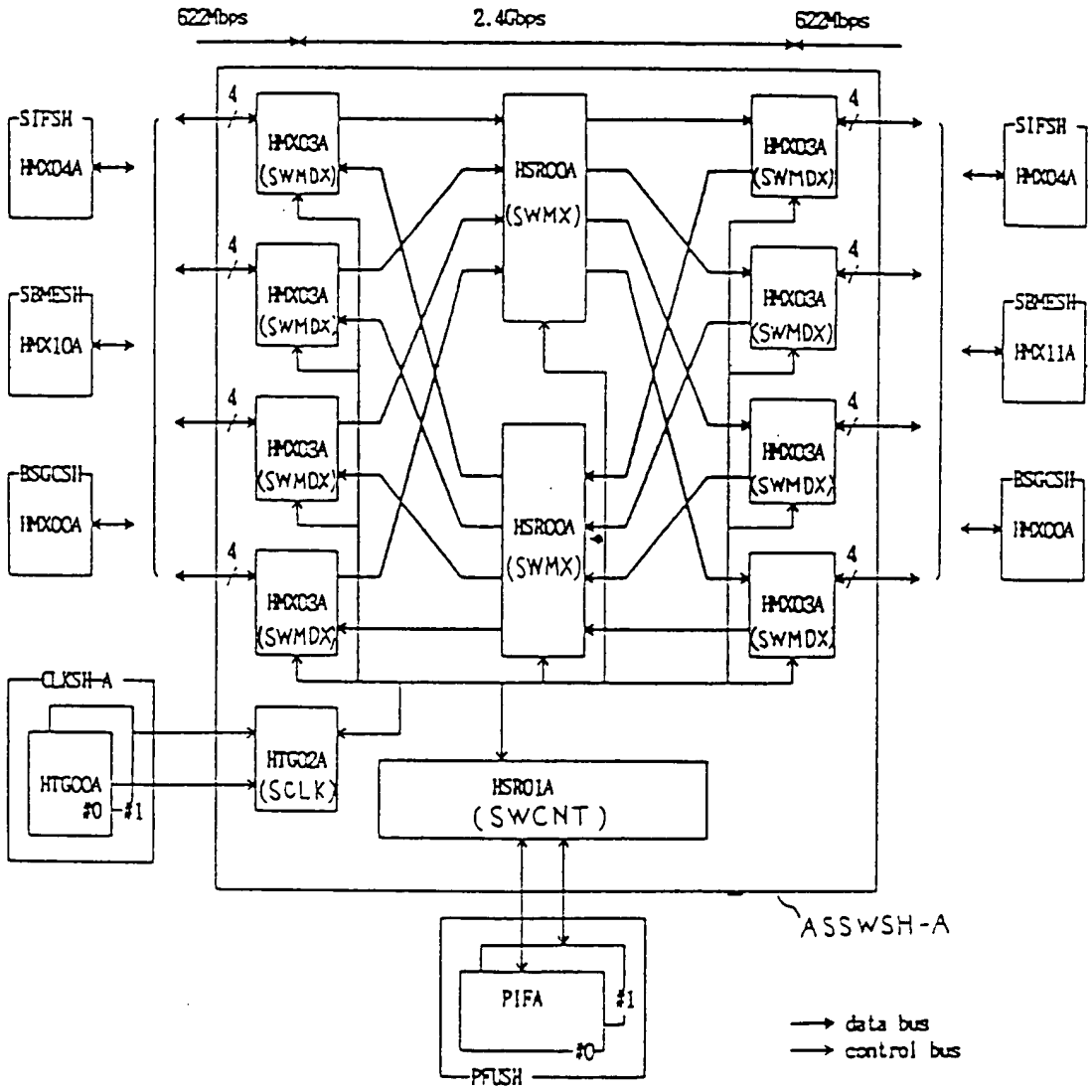

622Mbps
2.4Gbps
622Mbps
SIFSH
HMX04A
SBMESH
HMX10A
BSGCSH
HMX00A
HMX03A
(SWMDX)
HSR00A
(SWMX)
SIFSH
HMX04A
SBMESH
HMX11A
BSGCSH
HMX00A
CLKSH-A
HTG00A
#0
#1
HTG02A
(SCLK)
HSR01A
(SWCNT)
ASSWSH-A
PIFA
#1
#0
PFUSH
data bus
control bus

FIG. 167

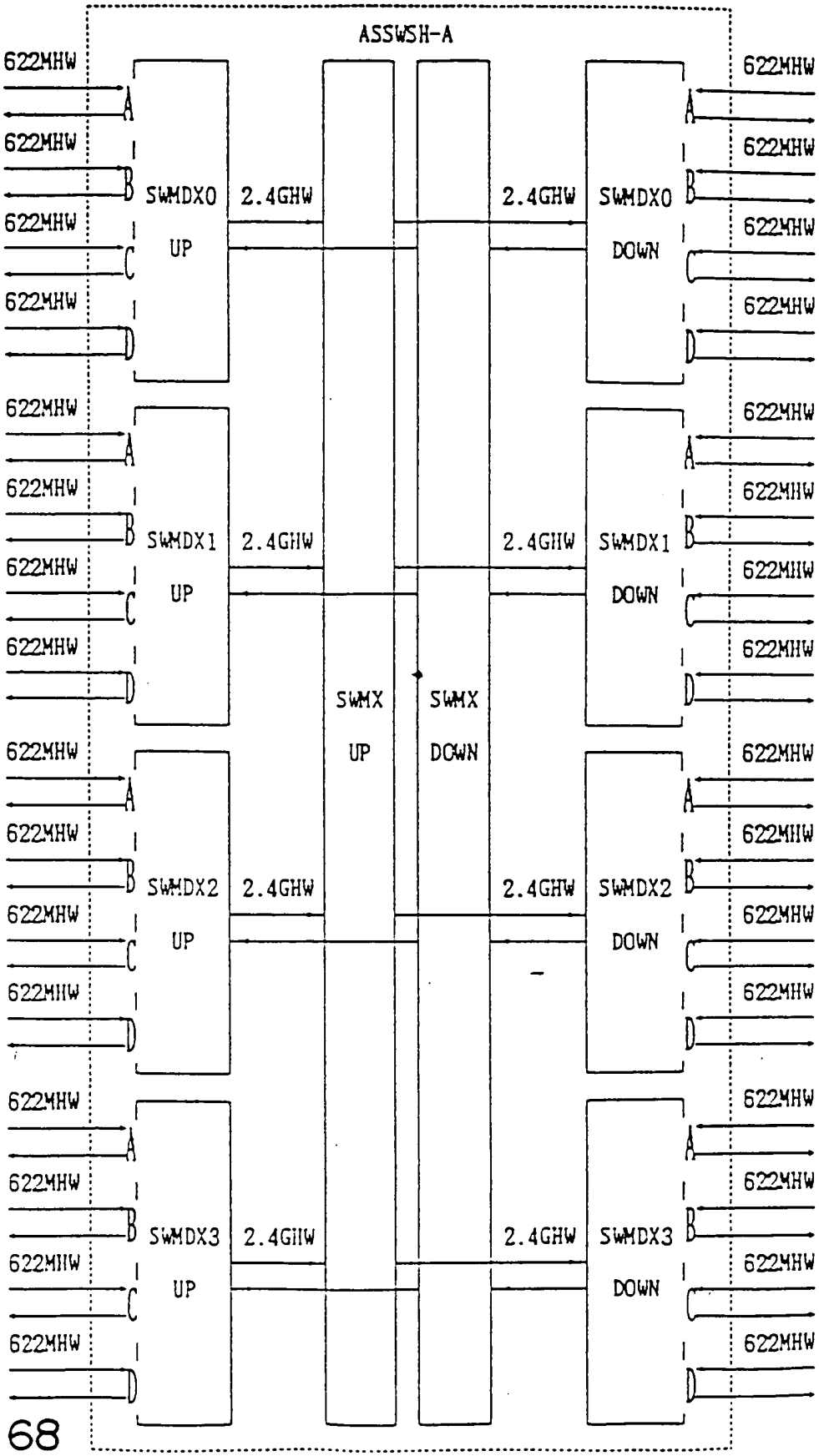
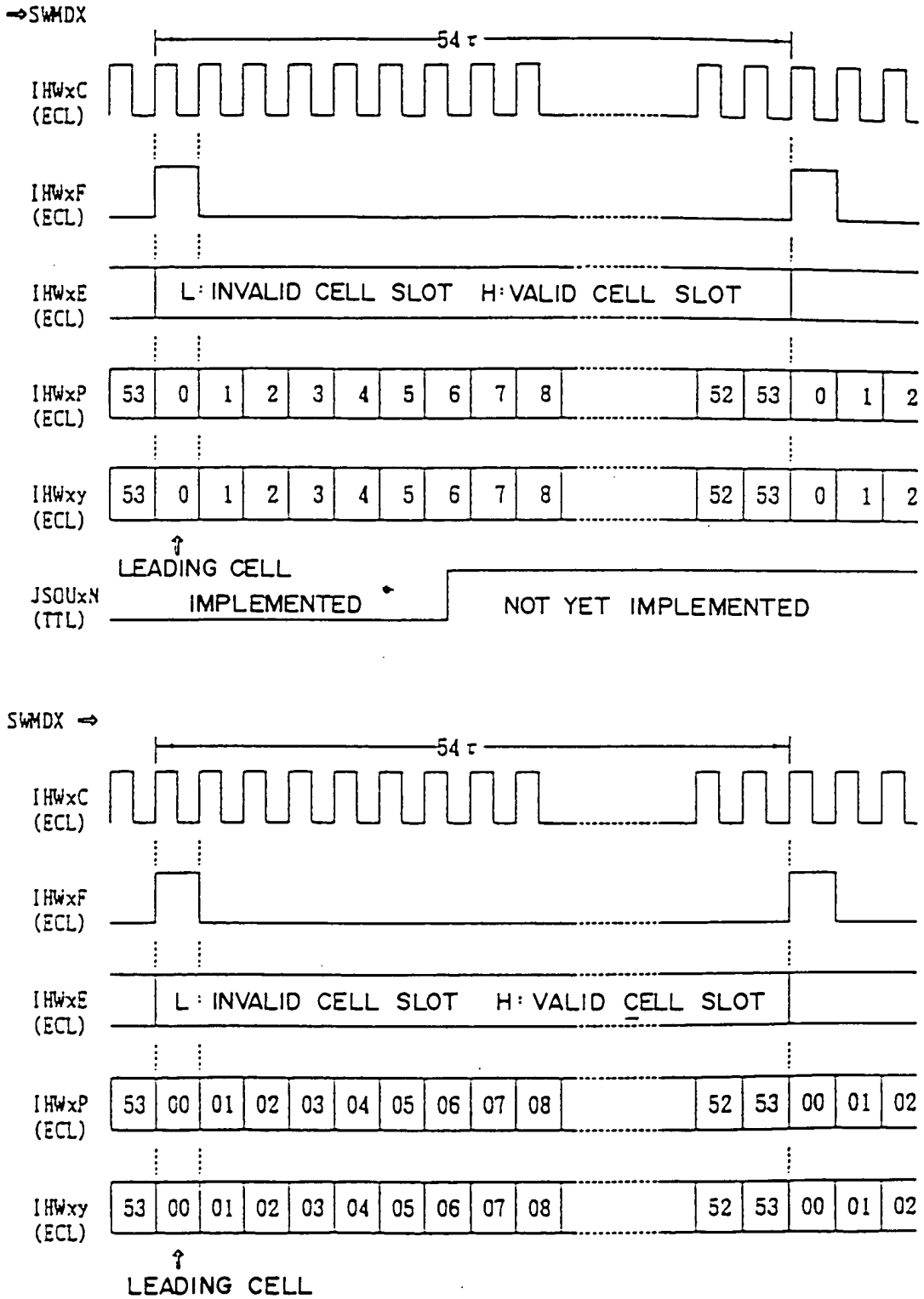
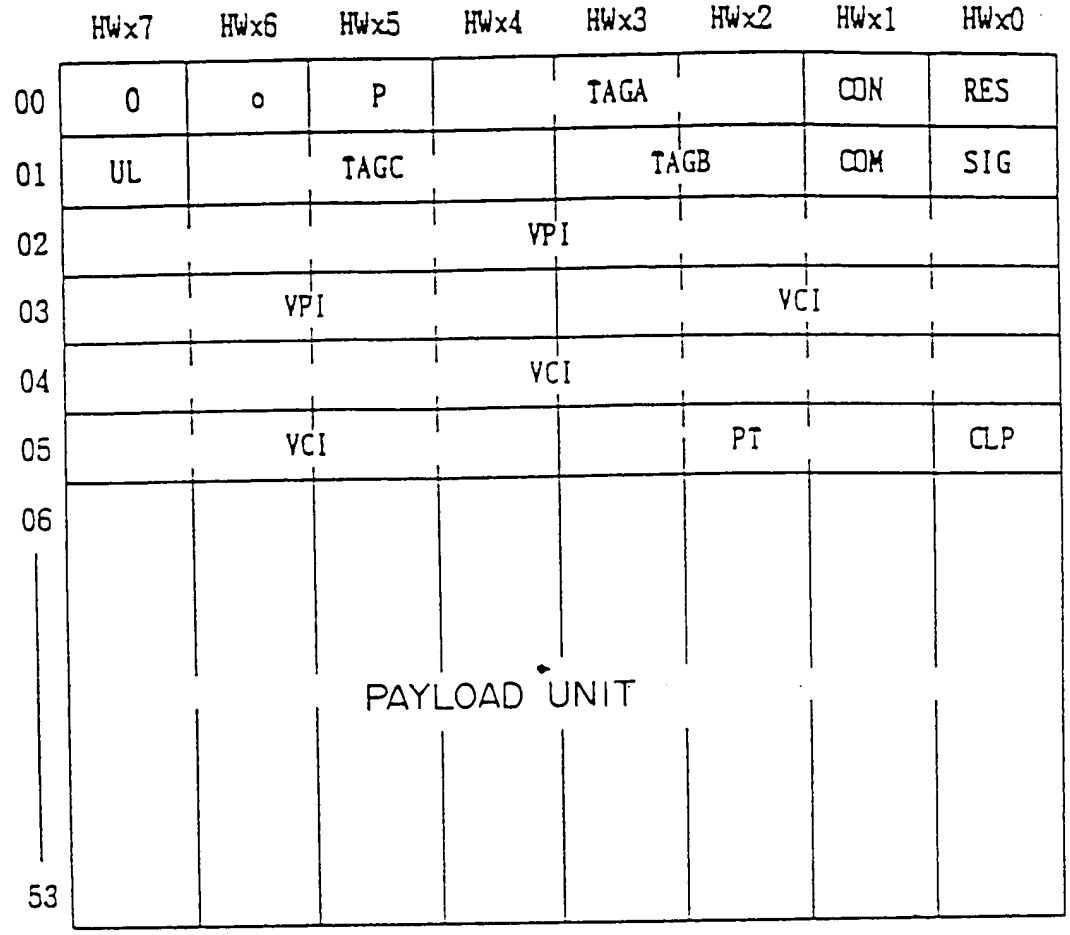

ASSWSH-A
622MHW
A
B
C
D
SWMDX0
UP
SWMDX1
UP
SWMDX2
UP
SWMDX3
UP
2.4GHW
SWMX
UP
SWMX
DOWN
SWMDX0
DOWN
SWMDX1
DOWN
SWMDX2
DOWN
SWMDX3
DOWN

FIG. 168



(x:0~3, y:0~7)

FIG. 169



TAG AREA

0	: Fixed zero (COPY INDICATION 0 REFERS TO 1 : 1 COMMUNICATIONS.)
o	: Test bit
P	: Priority bit (CLPのcopy) (0:High priority)
TAGA	: 2.4G 4x4 Switch TAG
TAGB	: 2.4GHW ⇨ 622MHW Demultiplex TAG
TAGC	: 622MHW ⇨ 155MHW Demultiplex TAG
CON	: Congestion Control bit (IMPORTANT CALL IDENTIFICATION)
RES	: reserve
COM	: COMMON UNIT IDENTIFICATION IN TERMINAL DEVICE (1:COMMON UNIT)
SIG	: INTRA-STATION LAP CELL (1: LAP CELL)

ATM Header AREA

VPI	: Virtual Path Identifier
VCI	: Virtual Channel Identifier
PT	: Payload Type
CLP	: Cell Loss Priority bit

FIG. 170

DIRECTION	SIGNAL NAME	BIT NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	REMARKS
PIFA→ASSW	SRCLKC	1	V11 BALANCE (1:1)	←→ 250nsec	
	SBACK	1			BUS USE RIGHT PERMISSION
	RESET	1			PULSE WIDTH: 500nsec P-ON-R or M-RST
	SYSEL	1			SBY ACT
ASSW→PIFA	SRCLKL	1	V11 BALANCE (1:1)	←→ 250nsec	
	SBRQ	1			BUS USE REQUEST
	ALM	1			NORMAL VALUE ALARM
BI-DIRECTIONAL	SB0 ~ 7	8	V11 BALANCE BI-DIRECTIONAL		
	SBPTY	1			

FIG. 171

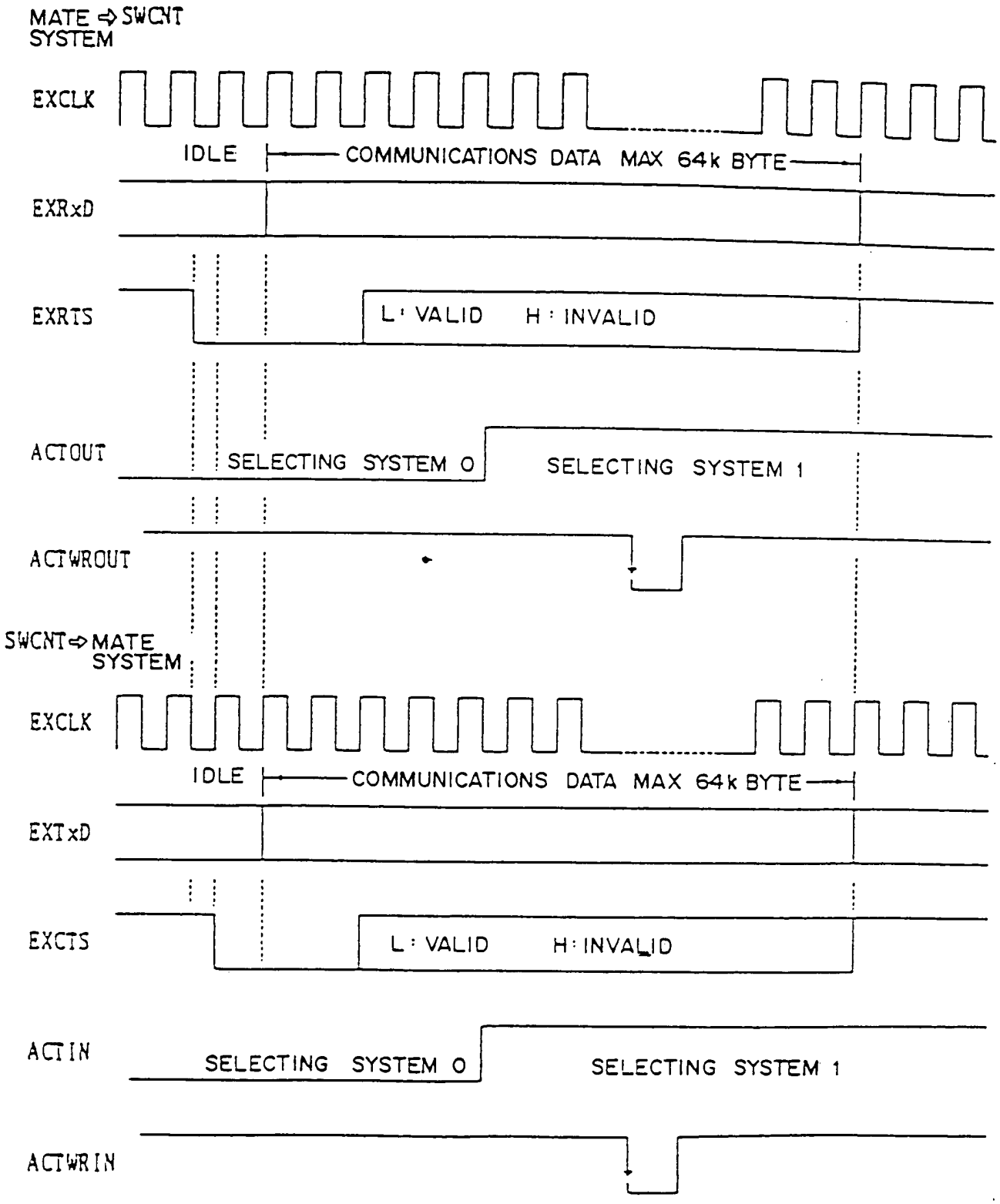

MATE ⇨ SWCNT SYSTEM
EXCLK
IDLE
COMMUNICATIONS DATA MAX 64k BYTE
EXRxD
EXRTS
L : VALID H : INVALID
ACTOUT
SELECTING SYSTEM 0
SELECTING SYSTEM 1
ACTWROUT
SWCNT⇨MATE SYSTEM
EXCLK
IDLE
COMMUNICATIONS DATA MAX 64k BYTE
EXTxD
EXCTS
L : VALID H : INVALID
ACTIN
SELECTING SYSTEM 0
SELECTING SYSTEM 1
ACTWRIN

FIG. 172

6692E0 "ET2Z260

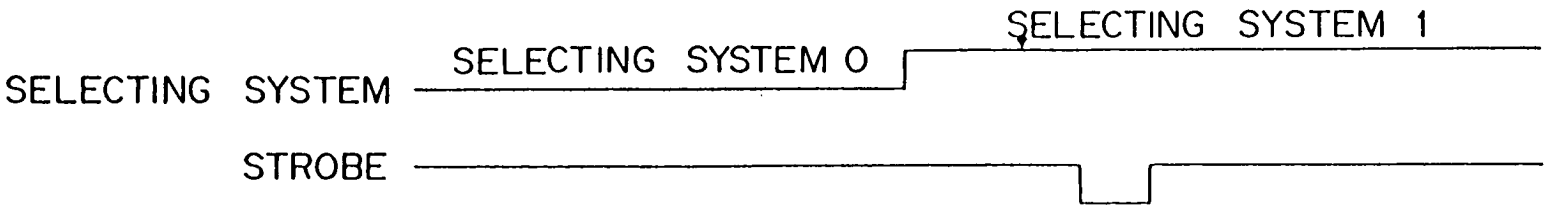


FIG. 173

SYSTEM SELECTION SIGNAL		SELECTION AT TERMINAL DEVICE
HOME SYSTEM SW SELECTION INDICATION	MATE SYSTEM SW SELECTION INDICATION	
SELECTING SYSTEM 0	SELECTING SYSTEM 0	SYSTEM 0
SELECTING SYSTEM 1	SELECTING SYSTEM 1	SYSTEM 1
SELECTING SYSTEM 0	SELECTING SYSTEM 1	RETAINING PREVIOUS STATE
SELECTING SYSTEM 1	SELECTING SYSTEM 0	RETAINING PREVIOUS STATE

FIG. 174

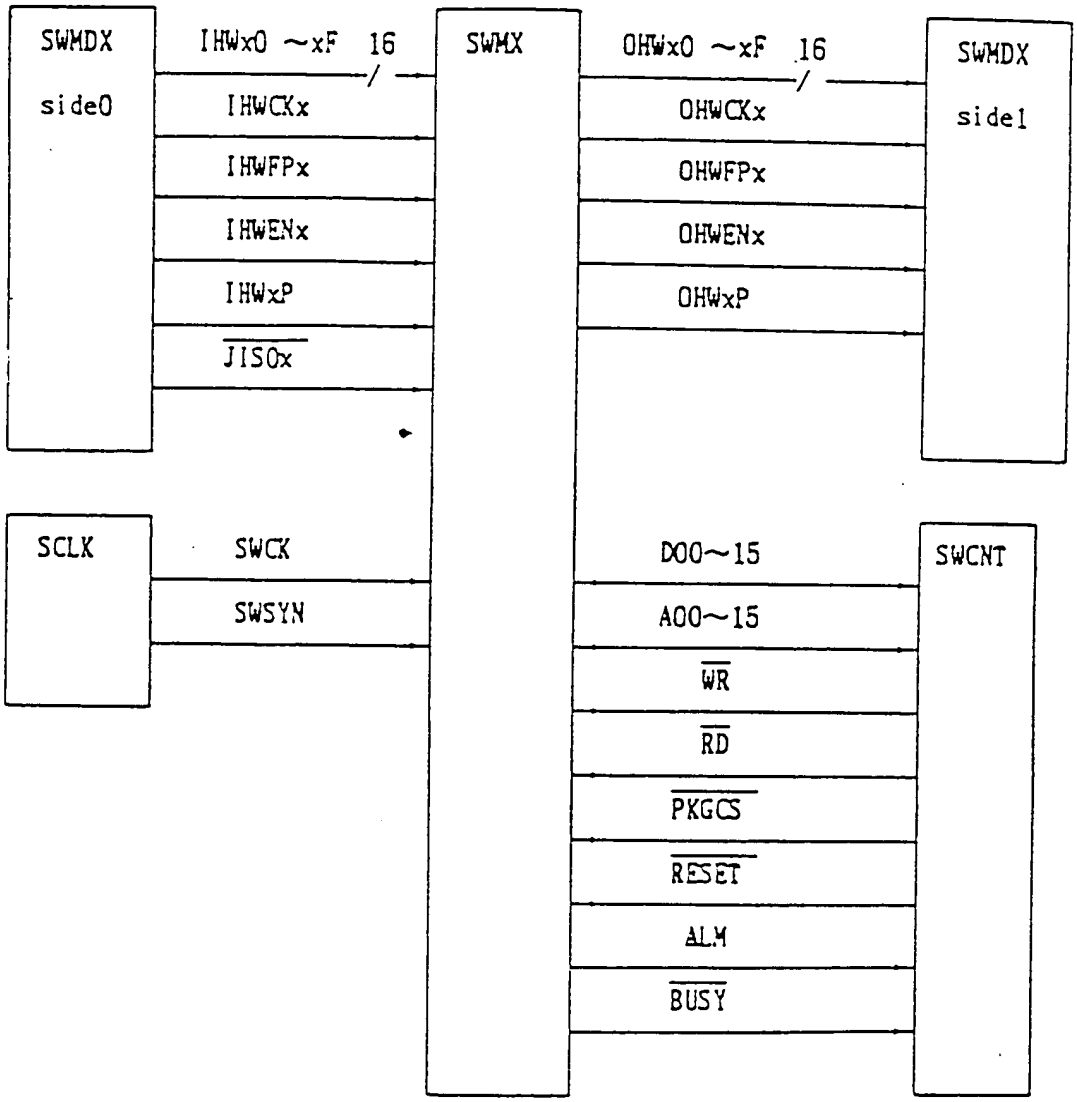

SWMDX
side0
IHWx0 ~xF 16
IHWCKx
IHWFPx
IHWENx
IHWxP
JISOx
SWMX
OHWx0 ~xF 16
OHWCKx
OHWFPx
OHWENx
OHWxP
SWMDX
side1
SCLK
SWCK
SWSYN
D00~15
A00~15
WR
RD
PKGCS
RESET
ALM
BUSY
SWCNT

FIG. 175

SIGNAL NAME	SENDING/RECEIVING	LEVEL	MEANING OF SIGNAL
IHWCKx	RECEIVING	ECL	155.52 MHz INPUT CLOCK
IHWxx		ECL	2.4G INPUT HW 16-BIT PARALLEL DATA
IHWFPx		ECL	INPUT CELL FRAME PULSE
IHWENx		ECL	INPUT CELL ENABLE
IHWxP		ECL	ODD PARITY FOR 16-BIT INPUT DATA
JISOx		TTL	2.4G HW IMPLEMENTATION INDICATION
SWCK		ECL	SW BUFFER READING 155.52 MHz CLOCK
SWSYN		ECL	
OHWCKx	SENDING	ECL	155.52 MHz OUTPUT CLOCK
OHWxx		ECL	2.4G OUTPUT HW 16-BIT PARALLEL DATA
OHWFPx		ECL	OUTPUT CELL FRAME PULSE
OHWENx		ECL	OUTPUT CELL ENABLE
OHWxP		ECL	ODD PARITY FOR 16-BIT OUTPUT DATA
Dxx	BIDIRECTIONAL	TTL	PROCESSOR DATA BUS
Axx		TTL	PROCESSOR ADDRESS BUS
WR		TTL	WRITE REQUEST SIGNAL
RD		TTL	READ REQUEST SIGNAL
PKGCS	RECEIVING	TTL	PACKAGE SELECTION
RESET		TTL	POWER-ON, OR OF M-RST
ALM	SENDING	TTL	NG-OR OF FAULT MONITOR POINT IN EACH PACKAGE
BUSY		TTL	-

FIG. 176

5,550,760 08/27/96

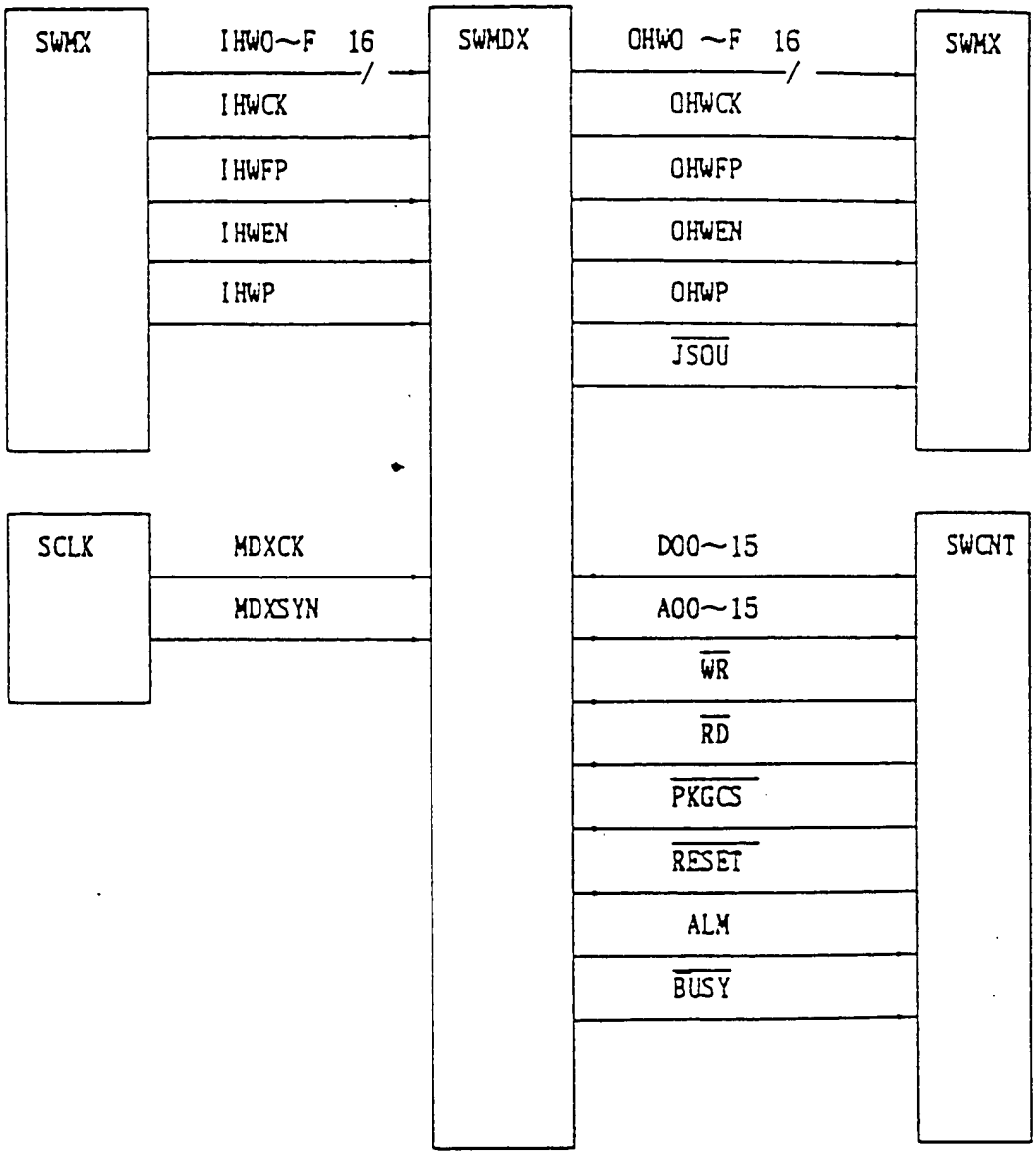


FIG. 177

SIGNAL NAME	SENDING/RECEIVING	LEVEL	MEANING OF SIGNAL
IHWCK	RECEIVING	ECL	155.52 MHz INPUT CLOCK
IHWx		ECL	2.4G INPUT HW 16-BIT PARALLEL DATA
IHWFP		ECL	INPUT CELL FRAME PULSE
IHWEN		ECL	INPUT CELL ENABLE
IHWP		ECL	ODD PARITY FOR 16-BIT INPUT DATA
MDXCK		TTL	MUX BUFFER READING 155.52 MHz CLOCK
MDXSYN		ECL	
OHWCK	SENDING	ECL	155.52 MHz OUTPUT CLOCK
OHWx		ECL	2.4G OUTPUT HW 16-BIT PARALLEL DATA
OHWFP		ECL	OUTPUT CELL FRAME PULSE
OHWEN		ECL	OUTPUT CELL ENABLE
OHWP		ECL	ODD PARITY FOR 16-BIT OUTPUT DATA
JSOU		ECL	2Z4G HW IMPLEMENTATION INDICATION
Dxx	BIDIRECTIONAL	TTL	PROCESSOR DATA BUS
Axx		TTL	PROCESSOR ADDRESS BUS
WR		TTL	WRITE REQUEST SIGNAL
RD		TTL	READ REQUEST SIGNAL
PKGCS	RECEIVING	TTL	PACKAGE SELECTION
RESET		TTL	POWER-ON, OR OF M-RST
ALM	SENDING	TTL	NG-OR OF FAULT MONITOR POINT IN EACH PACKAGE
BUSY		TTL	-

FIG. 178

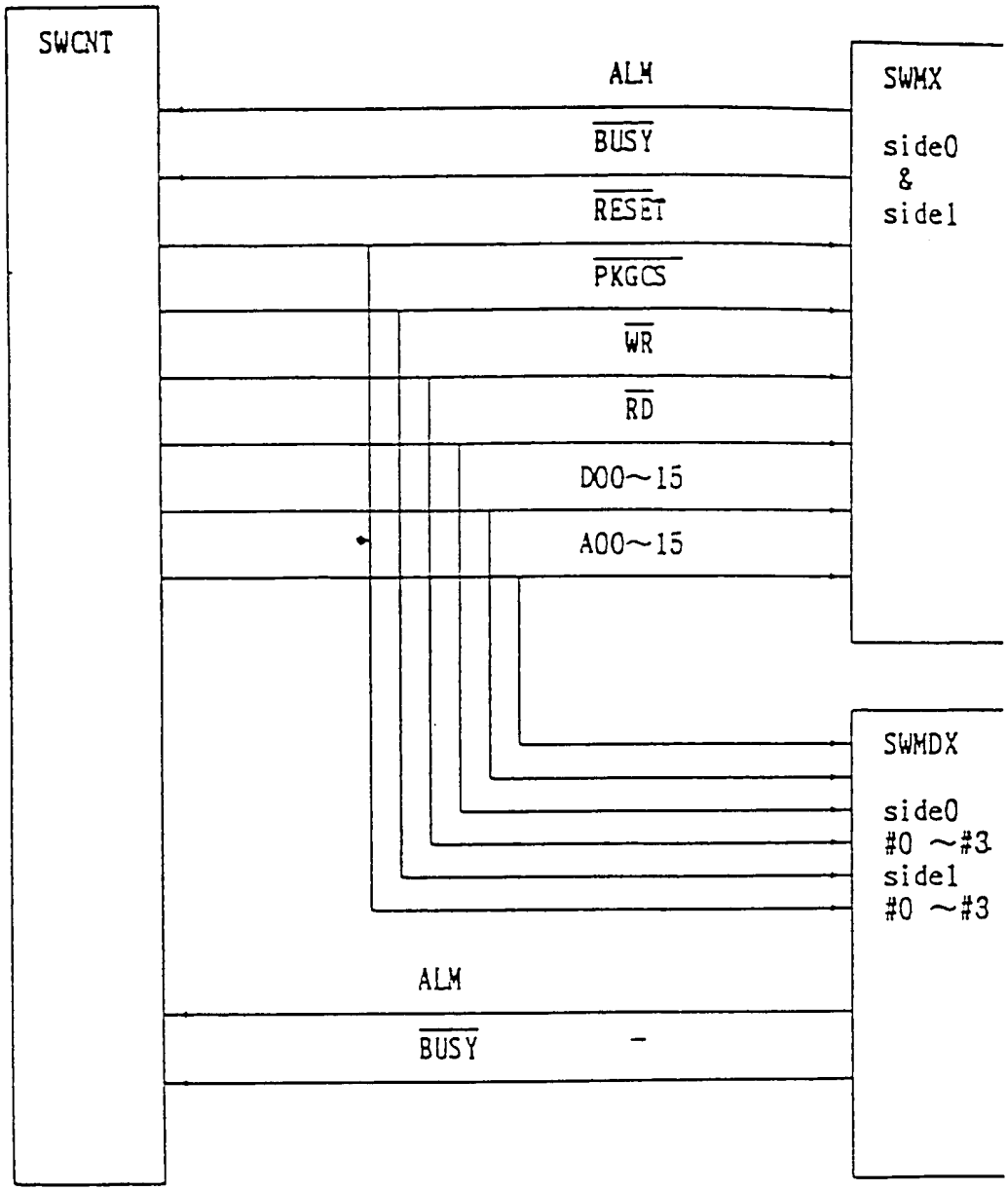

SWCNT
ALM
SWMX
BUSY
side0
&
side1
RESET
PKGCS
WR
RD
D00~15
A00~15
SWMDX
side0
#0 ~#3
side1
#0 ~#3
ALM
BUSY

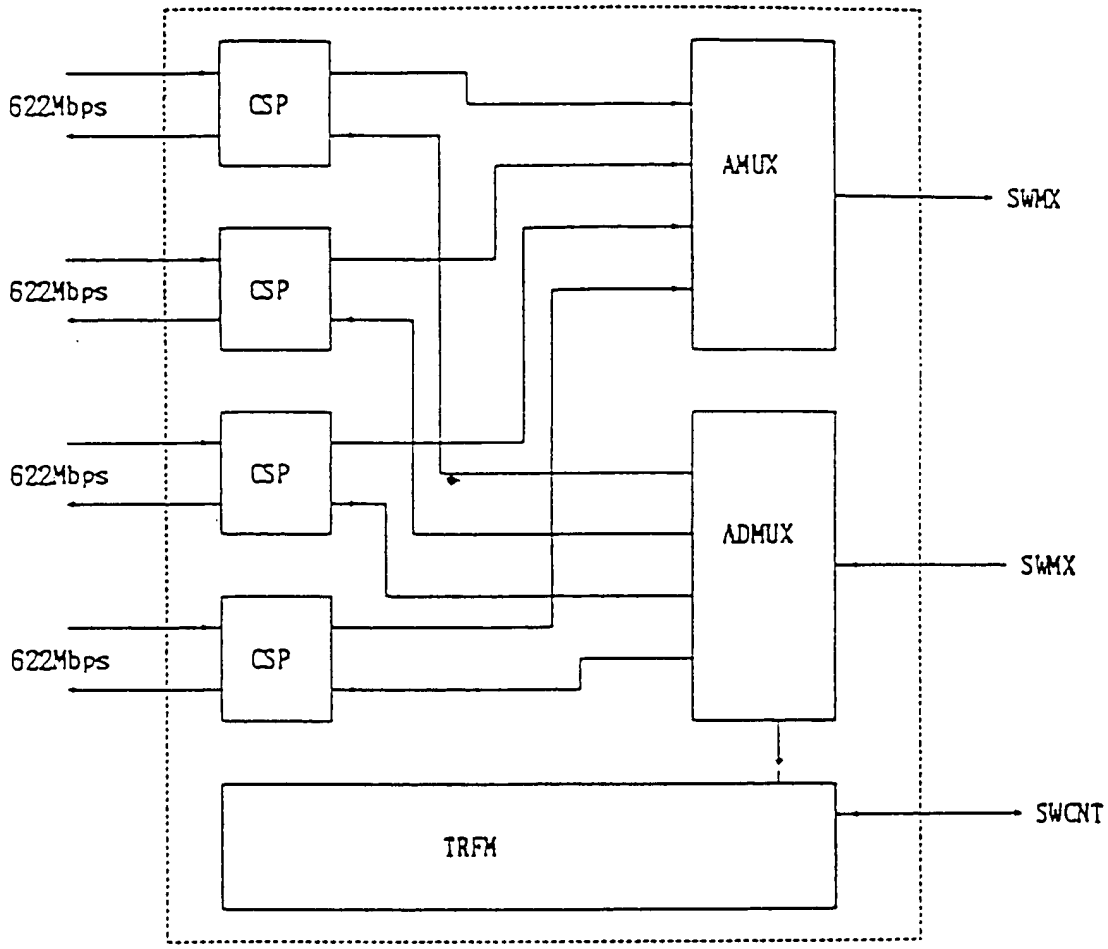
FIG. 179

SIGNAL NAME	SENDING/RECEIVING	LEVEL	MEANING OF SIGNAL
Dxx	BIDIRECTIONAL	TTL	PROCESSOR DATA BUS
Axx		TTL	PROCESSOR ADDRESS BUS
WR		TTL	WRITE REQUEST SIGNAL
RD		TTL	READ REQUEST SIGNAL
PKGCS	SENDING	TTL	PACKAGE SELECTION
RESET		TTL	POWER-ON, OR OF M-RST
ALM	RECEIVING	TTL	NG-OR OF FAULT MONITOR POINT IN EACH PACKAGE
BUSY		TTL	

FIG. 180

BLOCK NAME	FUNCTION
SWMDX	CELLS ARE MULTIPLEXED FROM 620 MBPS FULL ATM HIGHWAY TO 2.4 GBPS HIGHWAY IN SWITCH CELLS ARE DEMULTIPLEXED FRON 2.4 GBPS HIGHWAY IN SWITCH 620 MB S FULL ATM HIGHWAY TRAFFIC MEASUREMENT FUNCTION AND CONGESTION CONTROL FUNCTION
SWMX	4 ×4 SELF-ROUTING IN 2.4 GBPS HIHGWAY CONGESTION CONTROL FUNCTION
SWCNT	INTERFACE WITH DUPLEX CC FAULT MONITOR IN DEVICE
SWTIF	DISTRIBUTING ACT SIGNAL OF DUPLEX SYSTEM TO EACH TERMINAL DEVICE COMMON UNIT
SCLK	SELECTING SYSTEM OF CLK#0/1 GENERATING 155.52 MHZ FROM SELECTED 10.368 MSZ AND DISTRIBUTING IT TO EACH UNIT
POW	NECESSARY POWER SOURCE IS SUPPLIED IN DEVICE

FIG. 181

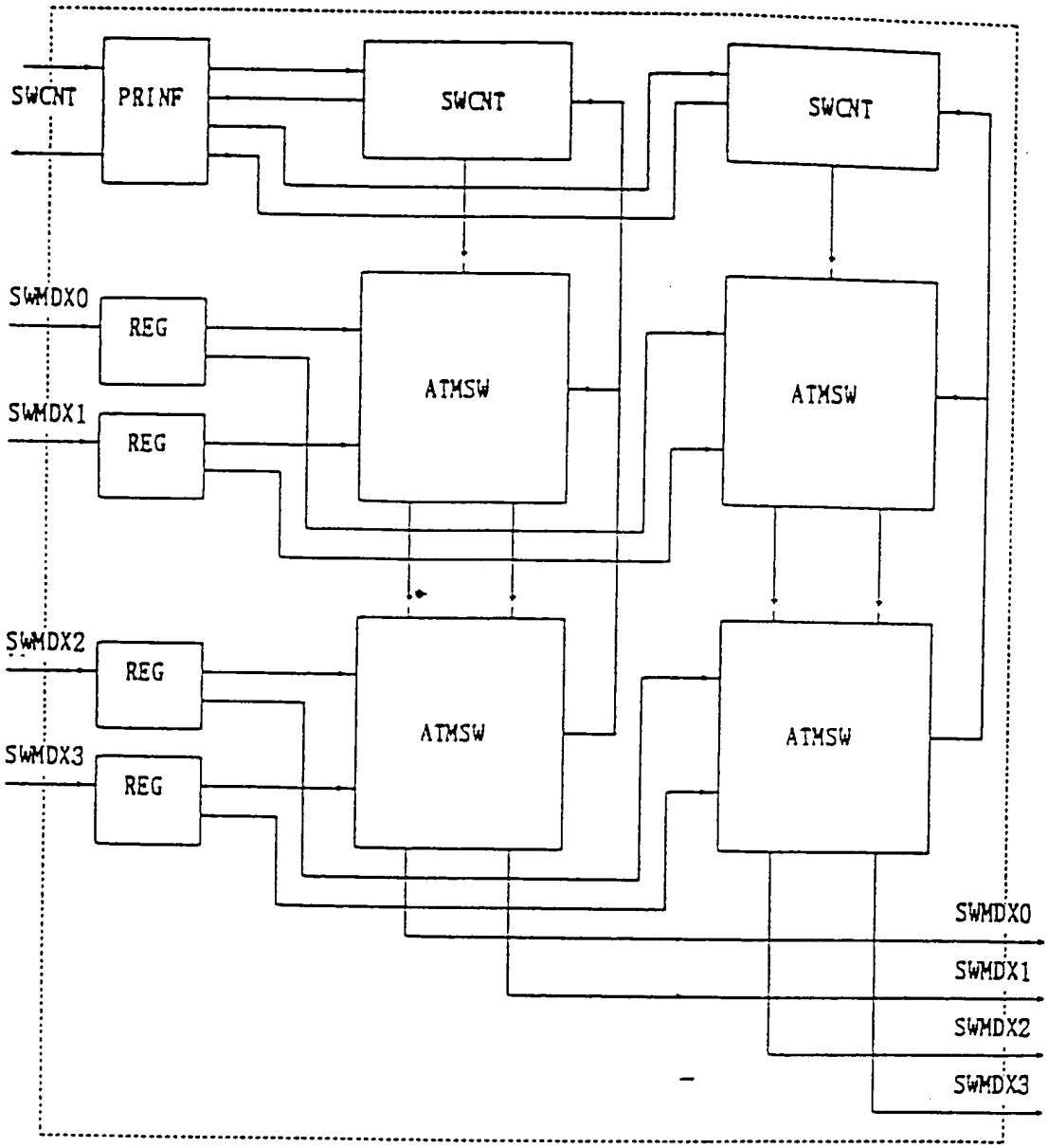


CSP : Cell Serial/Paralell Convertor
AMUX : ATM cell Multiplexer
ADMUX : ATM cell Demultiplexer
TRFM : Traffic Monitor

FIG. 182

BLOCK NAME	FUNCTION
CSP	・CONVERSION FROM 622 MBPS HIGHWAY 16 PARALLEL (TTL) TO 8 PARALLEL (ECL) ・CONVERSION FROM 622 MBPS HIGHWAY 8 PARALLEL (ECL) TO 16 PARALLEL (TTL) ・CHECKING PARITY IN INPUT HIGHWAY ・GENERATING PARITY IN OUTPUT HIGHWAY
AMUX	・FOUR 622 MBPS HIGHWAYS ARE CELL-MULTIPLEXED INTO 2.4 GBPS HIGHWAYS ・CHECKING PARITY IN INPUT HIGHWAY ・GENERATING PARITY IN OUTPUT HIGHWAY ・GENERATING AND CHECKING PARITY OF INTERNAL BUFFER
ADMUX	・2.4 GBPS HIGHWAY IS DEMULTIPLEXED INTO FOUR 622 MBPS HIHGWAYS ACCORDING TO TAG INFORMATION IN CELL ・CHECKING PARITY IN INPUT HIGHWAY (CELL IS DISCARDED, IF HEADER PARITY ERROR OCCURS) ・GENERATING PARITY IN OUTPUT HIGHWAY ・GENERATING AND CHECKING PARITY OF INTERNAL BUFFER ・OUTPUTTING CELL DISCARD NOTIFICATION, VALID CELL PASSING NITOFICATION, AND TRAFFIC MEASUREMENT HEADER INFORMATION ・SERVICE CLASS IS CONTROLLED BY P BIT WHEN DMUX BUFFER USE EXCEEDS THRESHOLD. (REFER TO TRAFFIC CONTROL FOR DETAILS)
TRFM	・SETTING AND READING PARAMETER FROM PROCESSOR (COUNTING NUMBER OF CELLS ARRIVING AND DISCARDED AT EACH OUTPUT LINE ACCORDING TO TRAFFIC INFORMATION FROM ADMUX)

FIG. 183

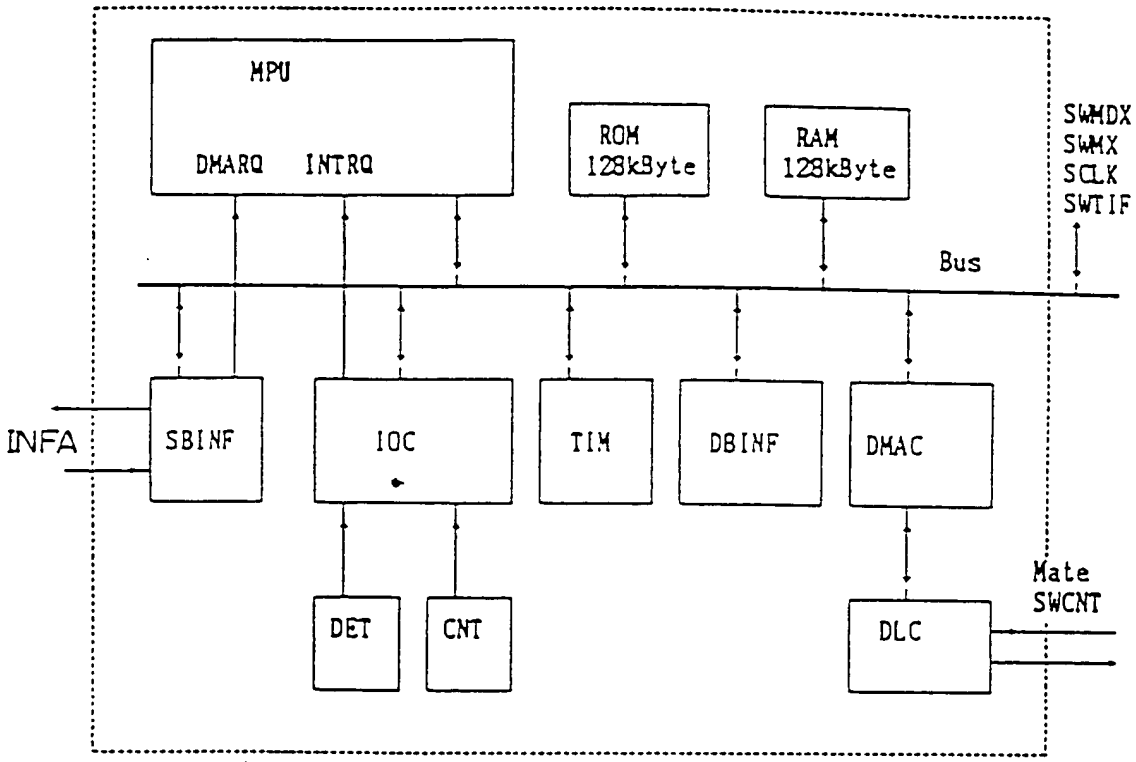


SWCNT : Switch Controller
ATMSW : ATM Switch
REG : Register
PRINF : Processor Interface

FIG. 184

BLOCK NAME	FUNCTION
SWCNT	・CELL READ FROM ATMSW IS CONTROLLED. ・ATMSW USE OF BUFFER IS MONITORED. ・SERVICE CLASS IS CONTROLLED BY P BIT WHEN BUFFER USE EXCEEDS THRESHOLD.
ATMSW	2×2 SELF-ROUTING SWITCH OF 2.4 GBPS HIGHWAY
REG	RETIMING INPUT HIGHWAY FROM SWMDX AND DISTRIBUTING IT TO ATMSWM
PRINF	SETTING AND READING PARAMETER FROM PROCESOR

FIG. 185

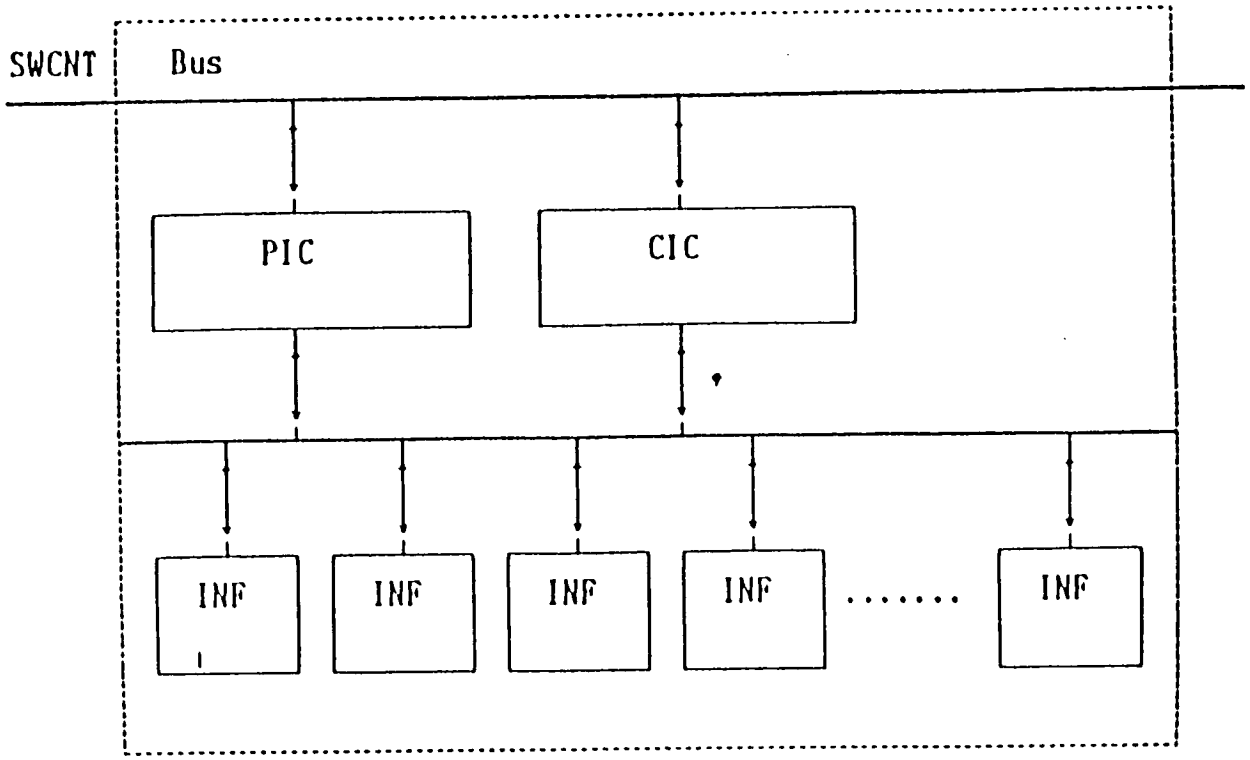


MPU : Micro-processor
IOC : I/O Controller
TIM : TIMER
ROM : Read Only Memory
RAM : Random Access Memory
SBINF : Switch Bus Interfacer
DLC : Data Link Controller
DMAC : DMA controller
DBINF : Debug Interfacer
DET : Fault Detecter
CNT : Interupt Controller

FIG. 186

BLOCK NAME	FUNCTION
MPU	SW UNIT CONTROL PROCESSOR
IOC	RECEIVING INTERRUPT REQUEST FROM I/O DEVICE AND CONTROLLING INTERRUPTION PROCESS
TIM	GENERATING FIRMWARE MONITOR TIMER AND DBINF COMMUNICATIONS CLOCK
ROM	STORING SW UNIT CONTROL PROGRAM
RAM	USED AS CONTROL PROCESSOR WORK AREA
SBINF	INTERFACING BETWEEN PIFA-SW BUS AND CONTROL PROCESSOR BUS. PERFORMING CC ACCESS PROCESS, DMA ACCESS PROCESS, AND MSCN PROCESS.
DLC	SERIAL COMMUNICATIONS CONTROLLER TO ESTABLISH COMMUNICATIONS WITH MATE SYSTEM
DMAC	DMA CONTROLLER FOR CONTROLLING DLC 4 CHANNEL
DBINF	DEBUGGING RS232C INTERFACE
DET	CONNECTING FAULT INFORMATION
CNT	CONTROLS VARIOUS INTERRUPTION INFORMATION

FIG. 187



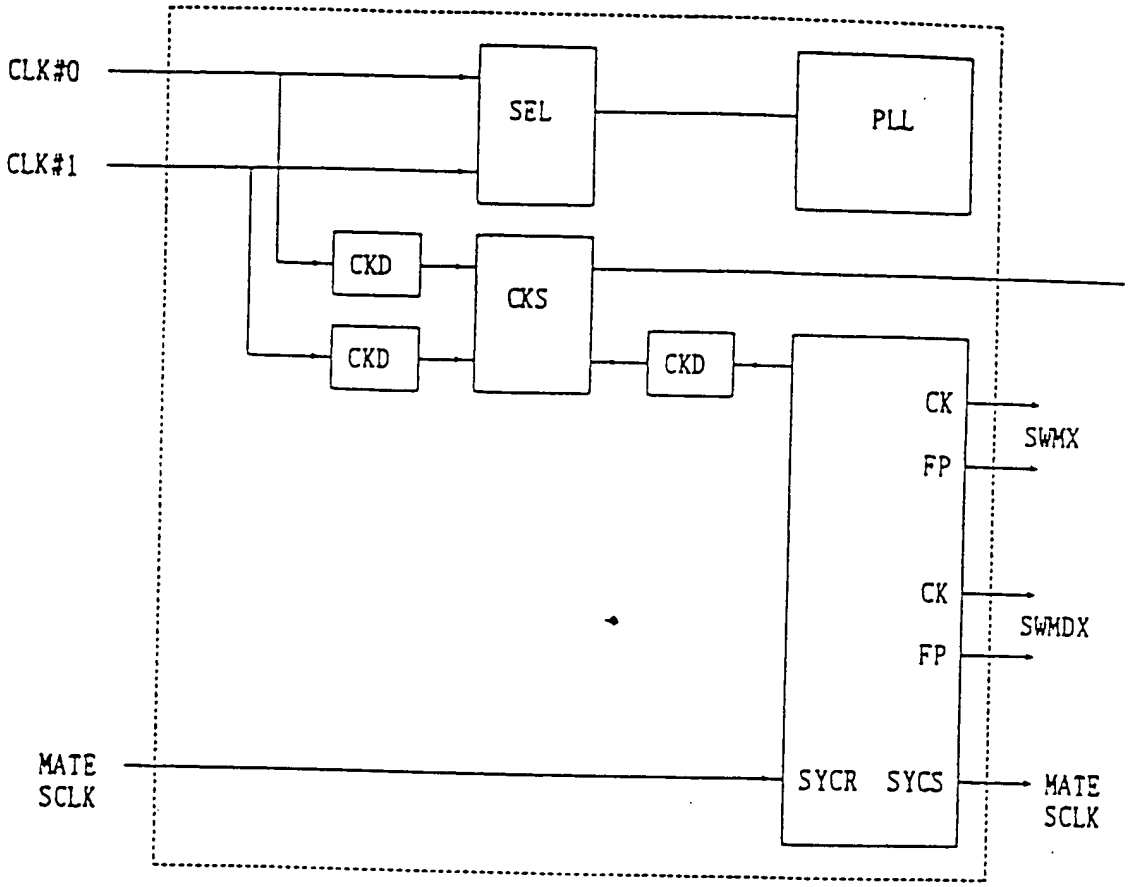
PIC : Processor Interface Controller
CIC : Communication Interface Controller
INF : Lower Unit Interfacer

FIG. 188

BLOCK NAME	FUNCTION
PIC	CONTROLLING INTERFACE WITH SW UNIT CONTROL PROCESSOR (i80C186) SELECTING LINE, REPORTING INTERRUPTION OCCURRENCE, ETC.
CIC	CONTROLLING INTERFACE WITH SWCNT DLC
INF	DETECTING COMMUNICATIONS CONTROL SIGNAL TO SW EXTENSION (NOT EXISTING) MONITORING PROCESSOR FAULT IN SW EXTENSION (NOT EXISTING)

FIG. 189

0927213.032609



CKD : Clock Down Detector
CKS : Clock Select Controller
SEL : Clock Selectore
PLL : Phase Lock Loop
TIM : Timing Generator

FIG. 190

BLOCK NAME	FUNCTION
CKD	DETECTING DISCONNECTION OF SYSTEM CLOCK FROM CLOCKS 0 AND 1 SYSTEMS DETECTING DISCONNECTION FROM OUTPUT CLOCK FROM PLL
CKS	SELECTING SYSTEM OF SYSTEM CLOCK (AUTONOMOUS SWITCH ACCORDING TO INFORMATION FROM CLKD) NOTIFYING SWCNT OF CLOCK FAULT AND SYSTEM SELECTION STATE
SEL	SELECTING AND OUTPUTTING CLOCK TO BE USED IN SRSW ACCORDING TO CONTROL SIGNAL OF CKS
PLL	GENERATING 155.5 MHZ FROM REFERENCE CLOCK 10.368 MHZ
TIM	GENERATING CLOCK/READ FRAME PULSE TO BE SUPPLIED TO SWMX AND SWMDX SYNCHRONIZING READ FRAME PULSE ACCORDING TO SYNCHRONIZATION SIGNAL FROM MATE SYSTEM AT INITIALIZATION

FIG. 191

SERVICE (CELL DISCARD CLASS)	CLP	P
Assured service (High priority)	0	0
Assured service (Low priority)	1	0
Non-assured service	1	1

FIG. 192

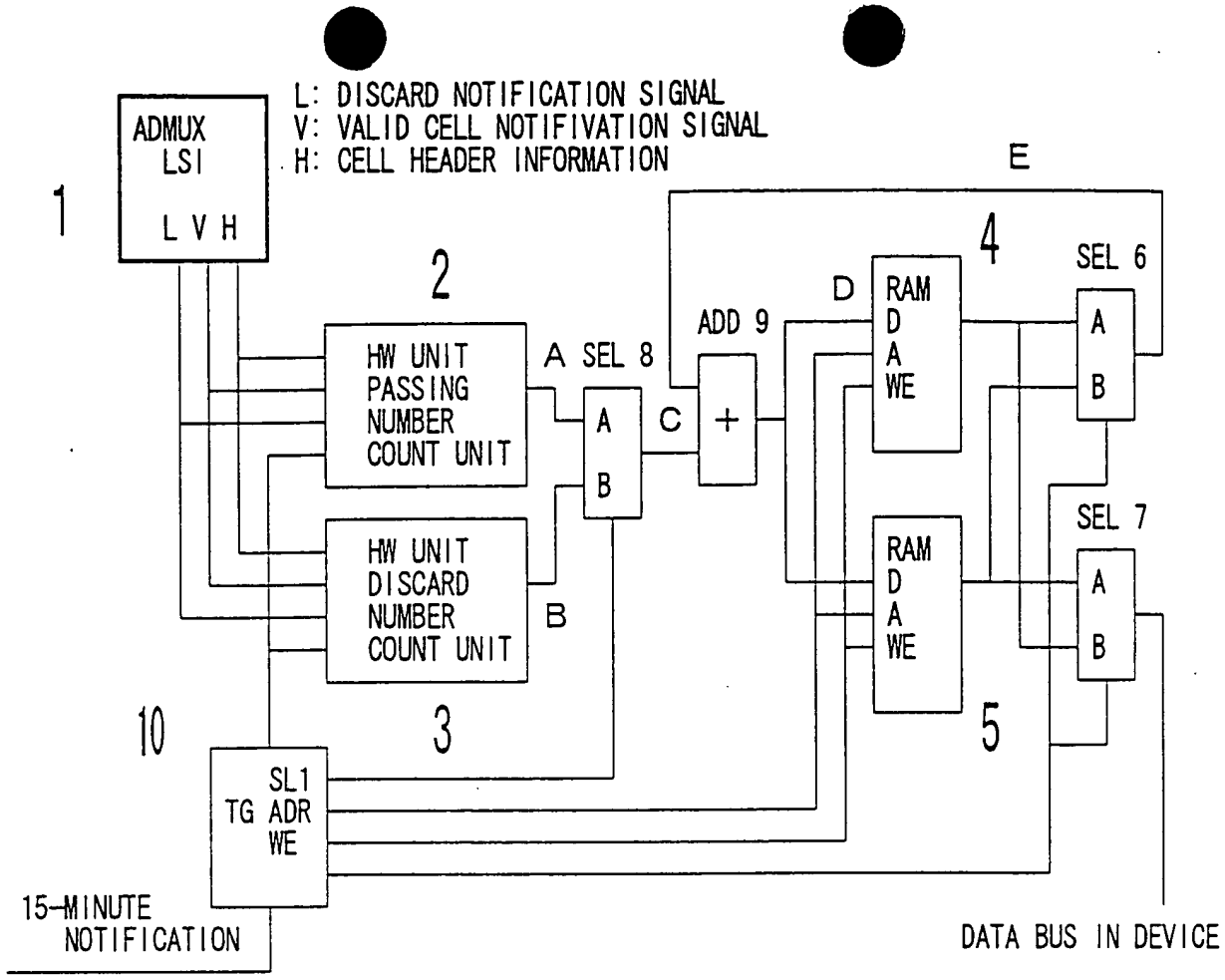

L: DISCARD NOTIFICATION SIGNAL
V: VALID CELL NOTIFIVATION SIGNAL
H: CELL HEADER INFORMATION
ADMUX LSI
L V H
1
2
HW UNIT PASSING NUMBER COUNT UNIT
HW UNIT DISCARD NUMBER COUNT UNIT
A SEL 8
A
B
C
+
ADD 9
D
E
4
RAM
D
A
WE
SEL 6
SEL 7
A
B
B
10
3
5
SL1
TG ADR
WE
15-MINUTE NOTIFICATION
DATA BUS IN DEVICE

FIG. 193

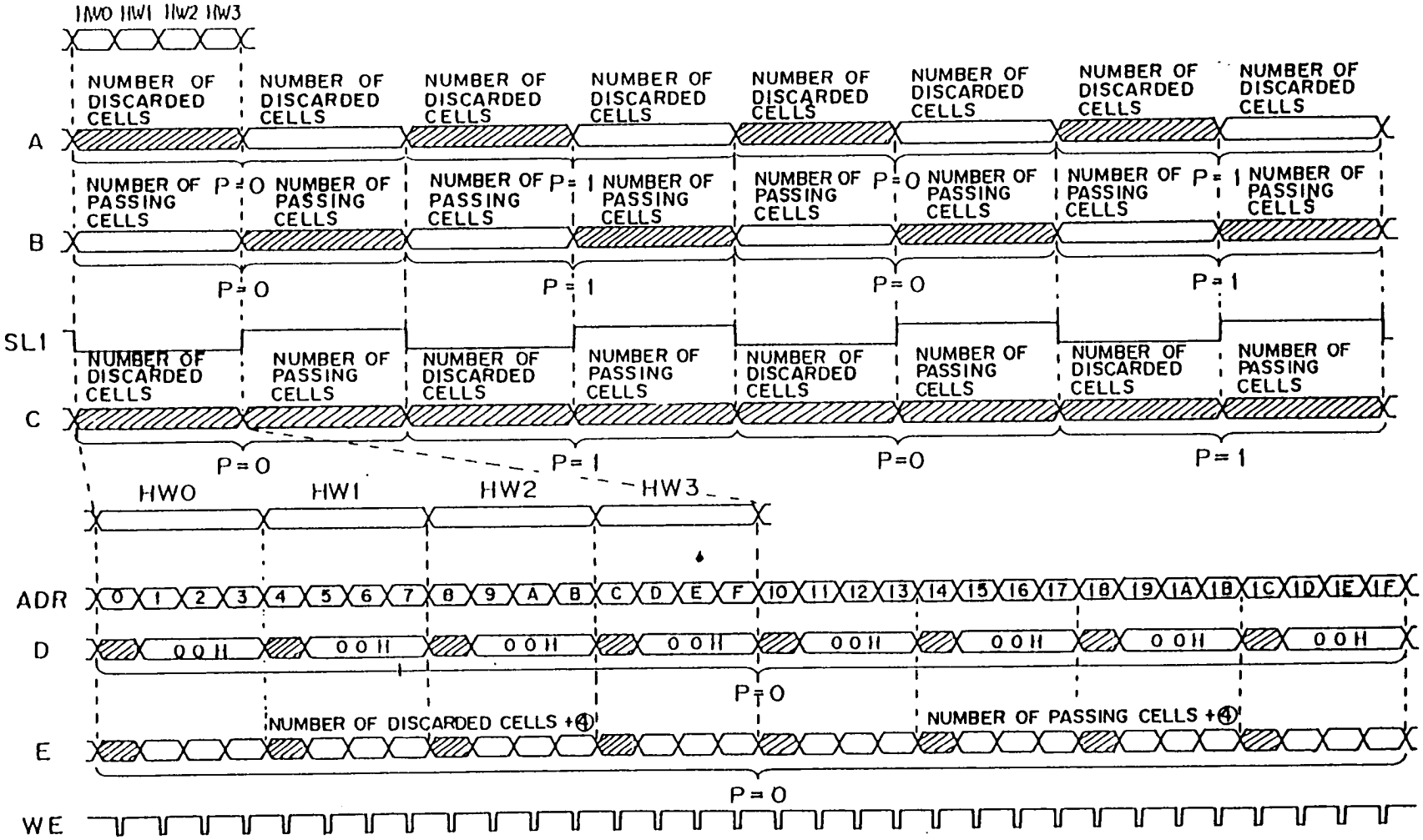
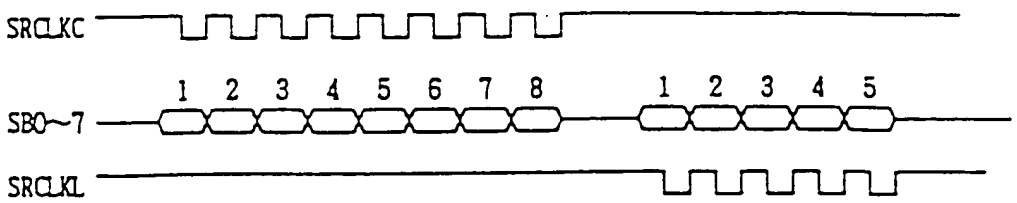

IHW0 IHW1 IHW2 IHW3
A
NUMBER OF DISCARDED CELLS
B
NUMBER OF PASSING CELLS
P=0
P=1
SL1
C
HW0
HW1
HW2
HW3
ADR
0 1 2 3 4 5 6 7 8 9 A B C D E F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F
D
00H
E
NUMBER OF DISCARDED CELLS +④
NUMBER OF PASSING CELLS +④
WE

FIG. 194

(a)



(b)

	1	2	3	4	5	6	7	8
SB0	(1)							
1								
2	D.	ADDRESS 16 ~ 23	ADDRESS 08 ~ 15	ADDRESS 00 ~ 07	D.	D.	D.	D.
3	C.				C.	C.	C.	C.
4								
5								
6								
SB7	(2)							
PTY	P	P	P	P	P	P	P	P

ADDRESS

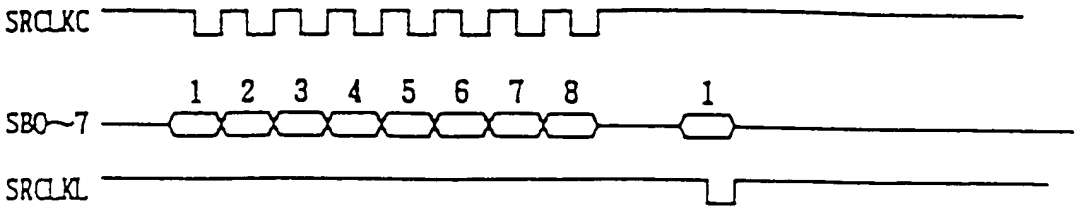
	1	2	3	4	5
	(1)				
	D.	Data 24 \ 31	Data 16 \ 23	Data 08 \ 15	Data 00 \ 07
	C.				
	(2)				
	P	P	P	P	P

DATA

(1)READ/WRITE READ:1 WRITE:0
(2)ORDER/ANSWER ORDER:1 ANSWER:0

FIG. 195

(a)



(b)

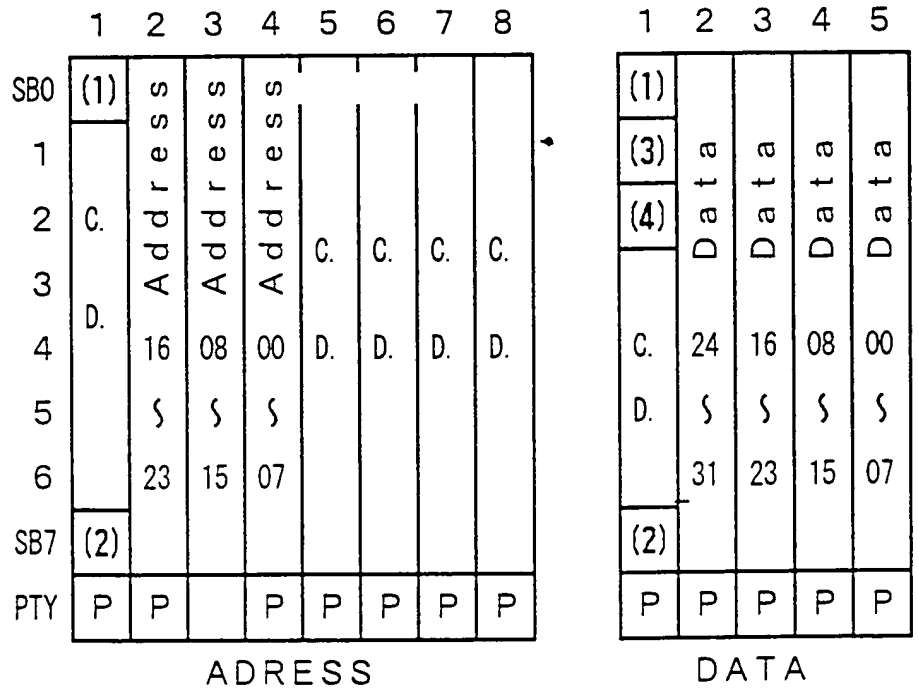
	1	2	3	4	5	6	7	8	1
SB0	(1)	ADDRESS 16 ~ 23	ADDRESS 08 ~ 15	ADDRESS 00 ~ 07	D. C.	D. C.	D. C.	D. C.	(1) D. C.
1									
2									
3									
4									
5									
6									
SB7	(2)								(2)
PTY	P	P	P	P	P	P	P	P	P
	ADDRESS								DATA

(1)READ/WRITE READ:1 WRITE:0
(2)ORDER/ANSWER ORDER:1 ANSWER:0

FIG. 196

(a)

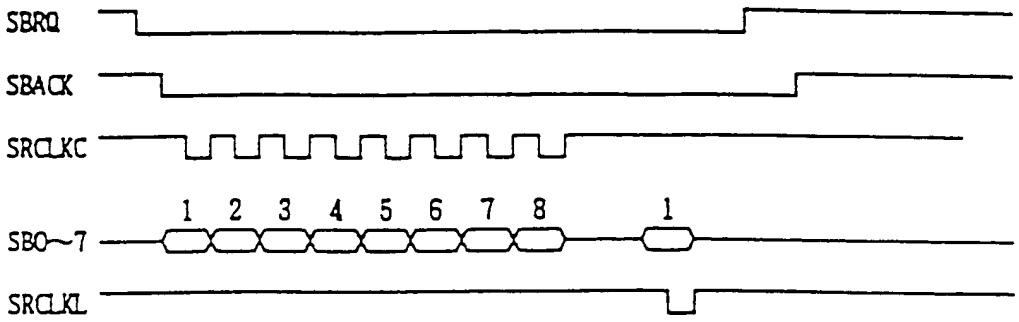
(b)



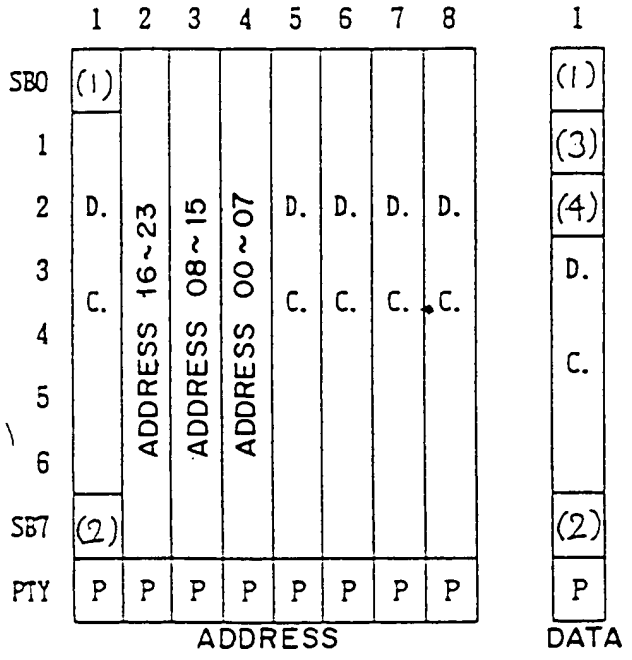
(1) READ/WRITE READ : 1 WRITE : 0
(2) ORDER/ANSWER ORDER : 1 ANSWER : 0
(3) ERROR1 ERROR EXISTING : 1 ERROR NOT EXSITING : 0
(4) ERROR2 ERROR EXISTING : 1 ERROR NOT EXSITING : 0

FIG. 197

(a)



(b)



(1) READ/WRITE READ:1 WRITE:0
(2) ORDER/ANSWER ORDER:1 ANSWER:0
(3) ERROR1 ERROR EXISTING : 1 NOT EXISTING : 0
(4) ERROR2 ERROR EXISTING : 1 NOT EXISTING : 0

FIG. 198

ORDER TYPE	IN/OUT	ORDER		MSB CONTENTS OF COMMANDS LSB																											
				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COMMAND ACTIVATION	OUT	0010	A	1	D. C.						(1)	D. C.			O	D. C.														ORDER			
			D	DC	NUMBER OF COMMANDS							COMMAND ADDRESS																					
RETRY INSTRUC-TION	OUT	0100	A	1	D. C.						(1)	D. C.			O	D. C.														ORDER			
			D	D. C.																													
MSCN READ	IN	1000	A	1	D. C.						(1)	D. C.			O	D. C.														ORDER			
			D	MSCN READ DATA																													
WRITIN TEST LOOP-BACK DATA	OUT	0001	A	1	D. C.						(1)	D. C.			O	D. C.														ORDER			
			D	LOOPBACK DATA																													
READING TEST LOOP-BACK DATA	IN	1001	A	1	D. C.						(1)	D. C.			O	D. C.														ORDER			
			D	LOOPBACK DATA																													

FIG. 199

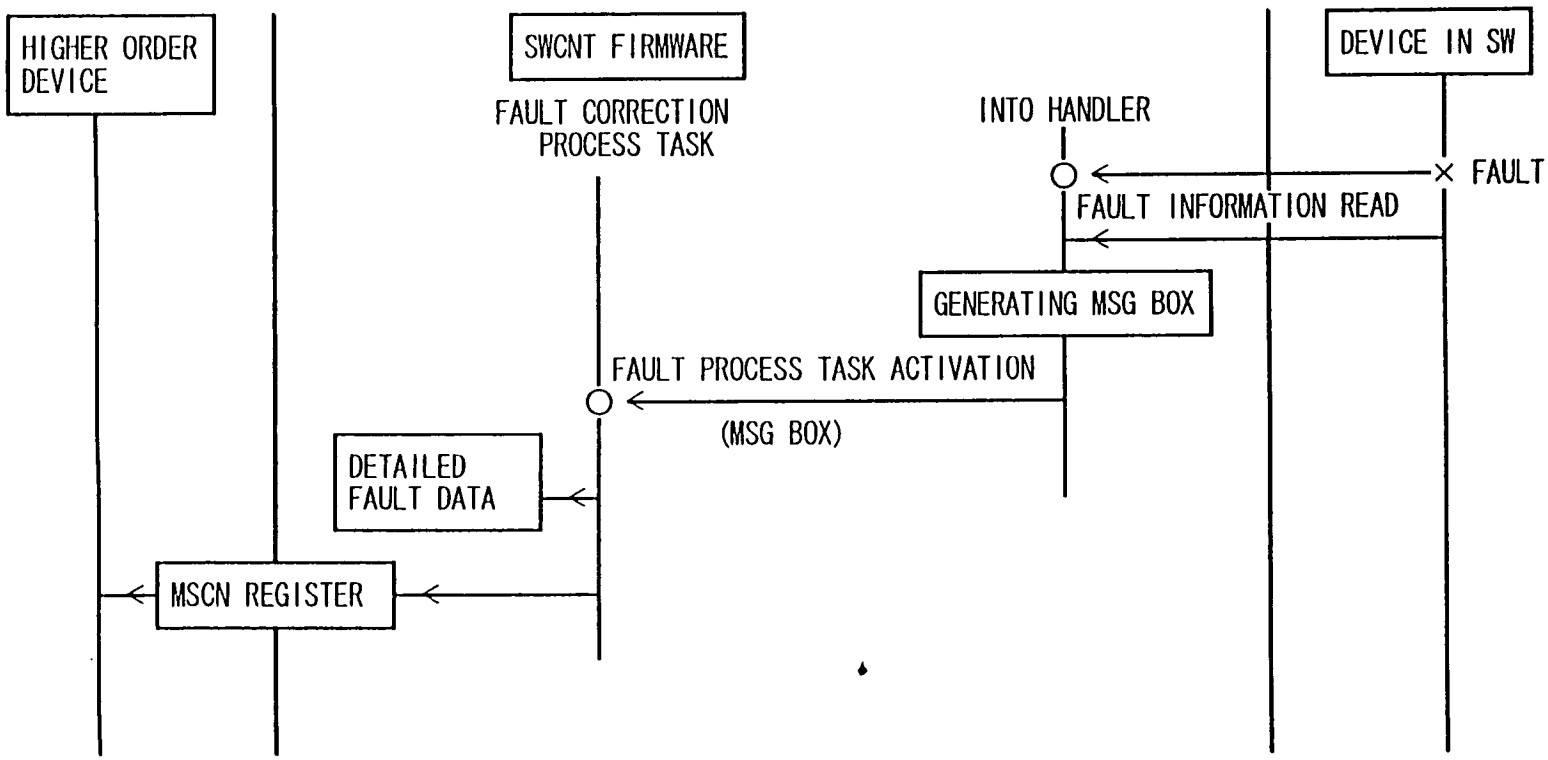

HIGHER ORDER DEVICE
SWCNT FIRMWARE
FAULT CORRECTION PROCESS TASK
INTO HANDLER
DEVICE IN SW
FAULT
FAULT INFORMATION READ
GENERATING MSG BOX
FAULT PROCESS TASK ACTIVATION
(MSG BOX)
DETAILED FAULT DATA
MSCN REGISTER

FIG. 200

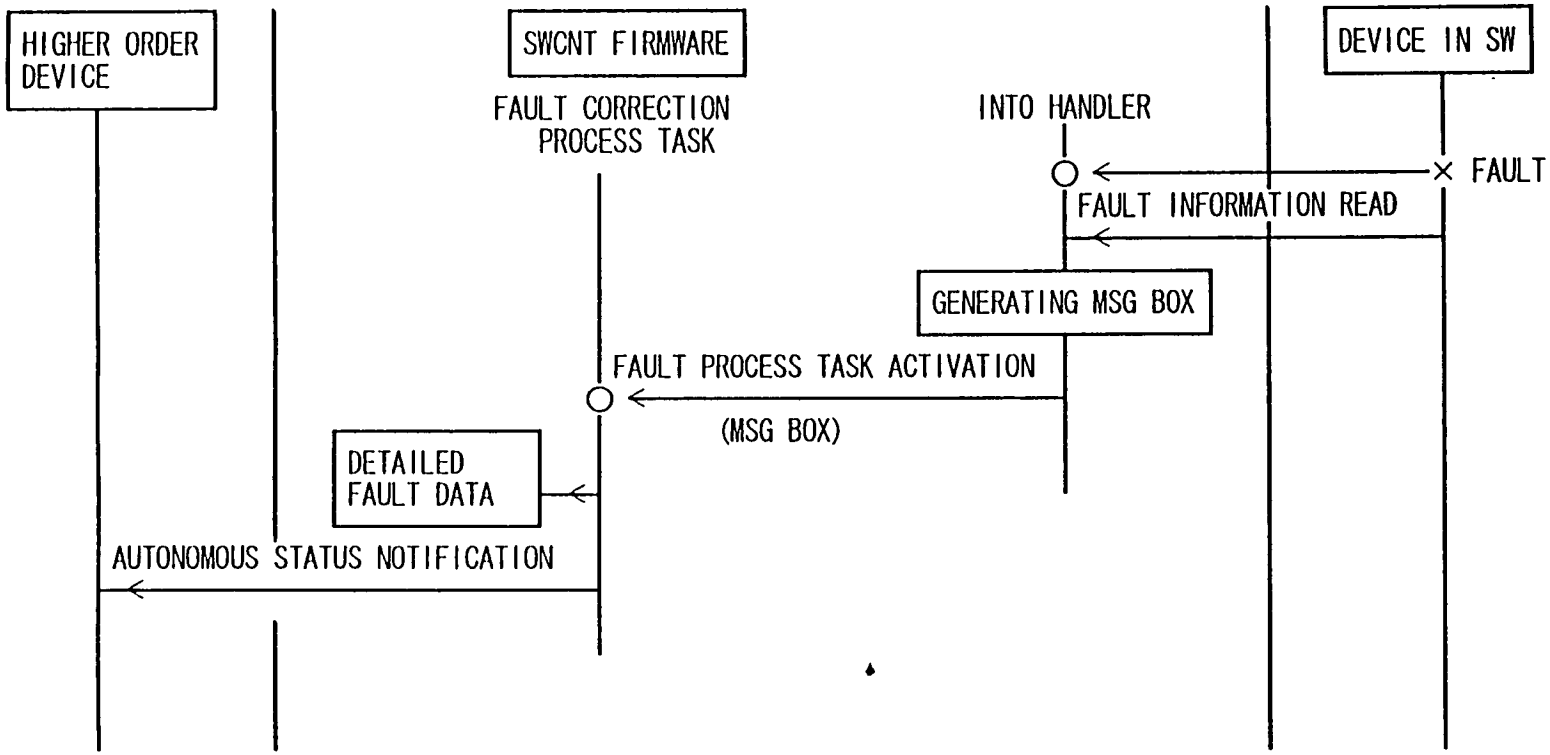

HIGHER ORDER DEVICE
SWCNT FIRMWARE
FAULT CORRECTION PROCESS TASK
INTO HANDLER
DEVICE IN SW
FAULT
FAULT INFORMATION READ
GENERATING MSG BOX
FAULT PROCESS TASK ACTIVATION
(MSG BOX)
DETAILED FAULT DATA
AUTONOMOUS STATUS NOTIFICATION

FIG. 201

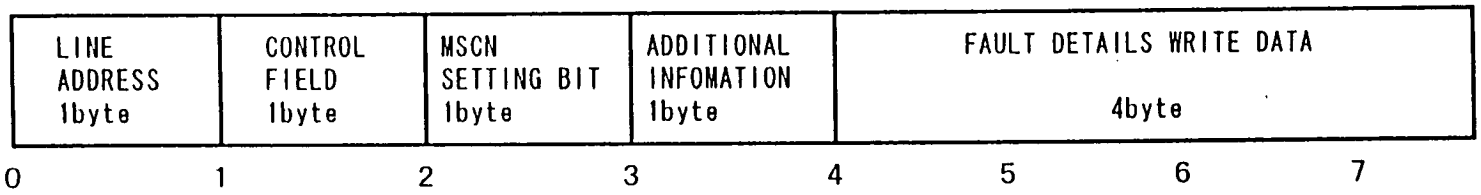

LINE ADDRESS 1byte
CONTROL FIELD 1byte
MSCN SETTING BIT 1byte
ADDITIONAL INFOMATION 1byte
FAULT DETAILS WRITE DATA 4byte
0
1
2
3
4
5
6
7

FIG. 202

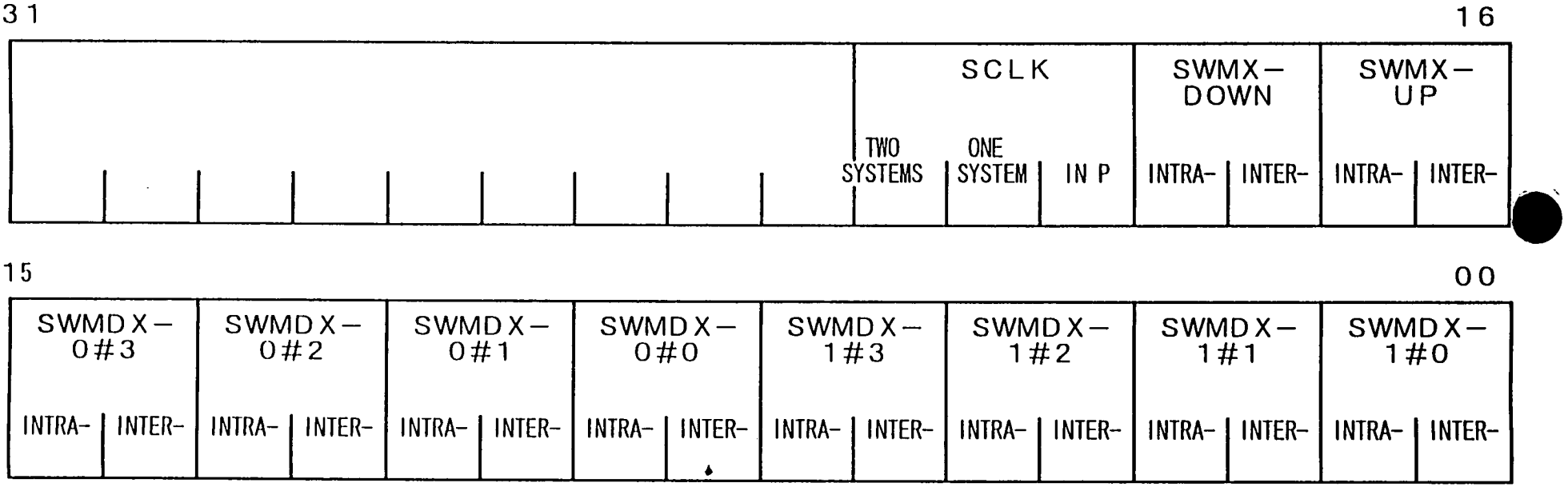

31
16
SCLK
SWMX-DOWN
SWMX-UP
TWO SYSTEMS
ONE SYSTEM
IN P
INTRA-
INTER-
INTRA-
INTER-
INTRA-
INTER-
15
00
SWMDX-0#3
SWMDX-0#2
SWMDX-0#1
SWMDX-0#0
SWMDX-1#3
SWMDX-1#2
SWMDX-1#1
SWMDX-1#0
INTRA-
INTER-

FIG. 203

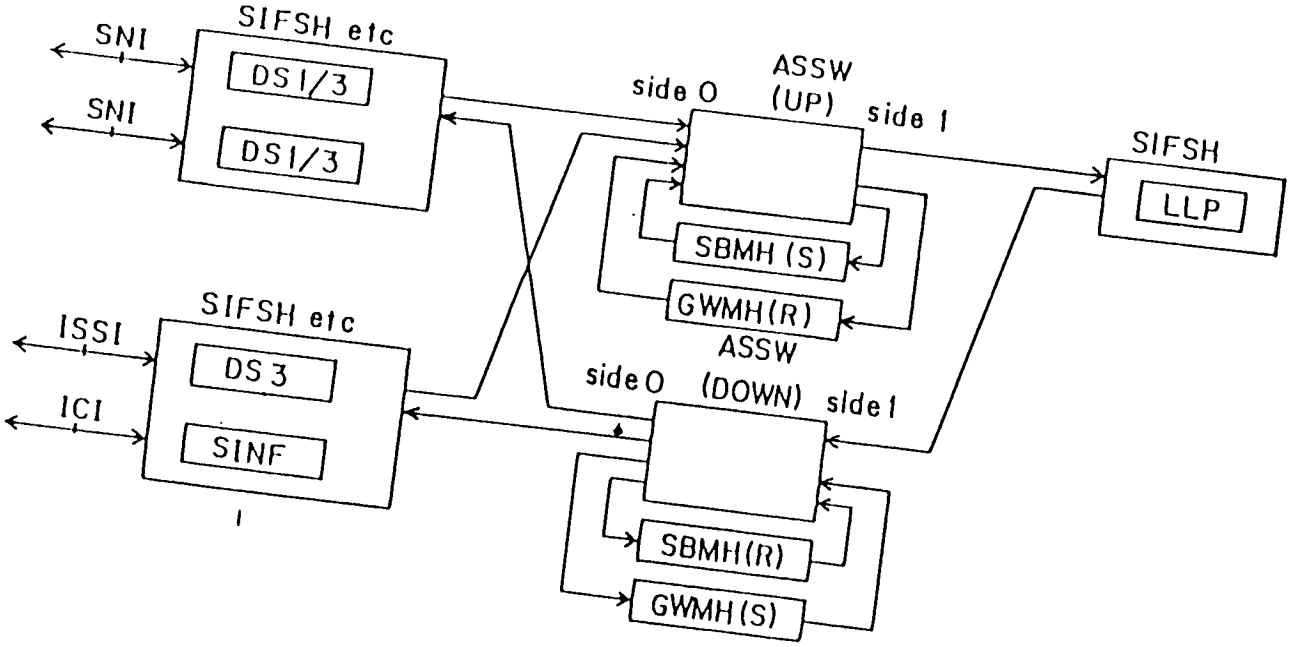

SNI
SNI
SIFSH etc
DS1/3
DS1/3
side 0
ASSW
(UP)
side 1
SIFSH
LLP
SBMH (S)
GWMH(R)
ISSI
ICI
SIFSH etc
DS3
SINF
ASSW
side 0
(DOWN)
side 1
SBMH(R)
GWMH(S)

FIG. 204

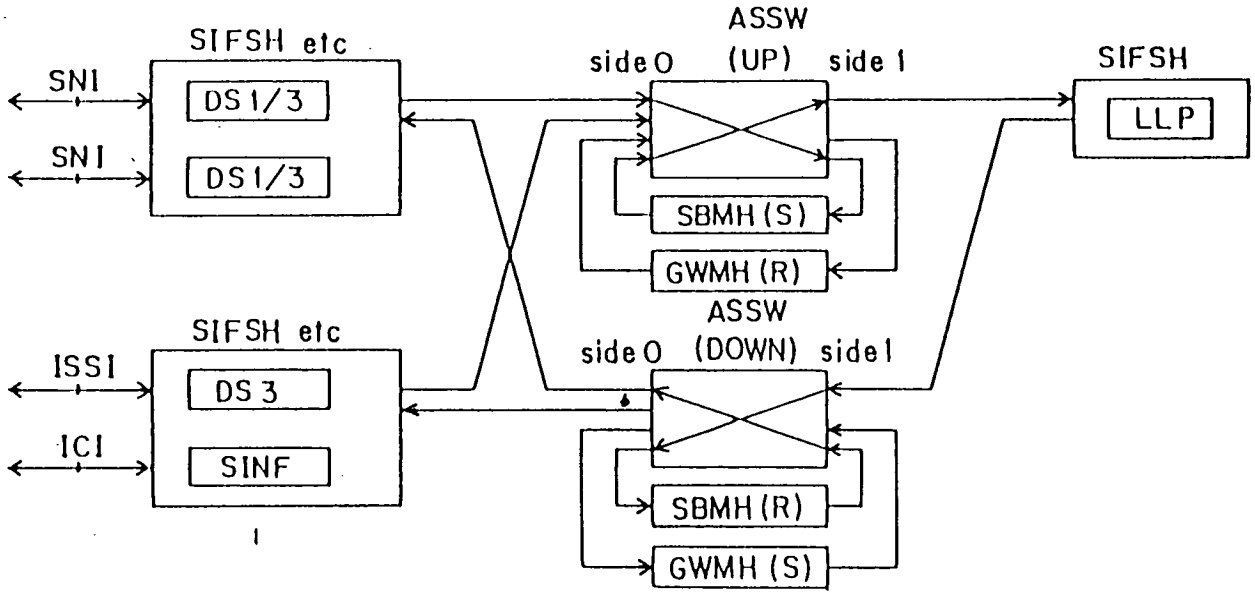

SIFSH etc
SNI
SNI
DS1/3
DS1/3
ASSW
side 0
(UP)
side 1
SIFSH
LLP
SBMH (S)
GWMH (R)
SIFSH etc
ISSI
ICI
DS 3
SINF
ASSW
side 0
(DOWN)
side 1
SBMH (R)
GWMH (S)

FIG. 205

6,958,269 EP 2,272,268

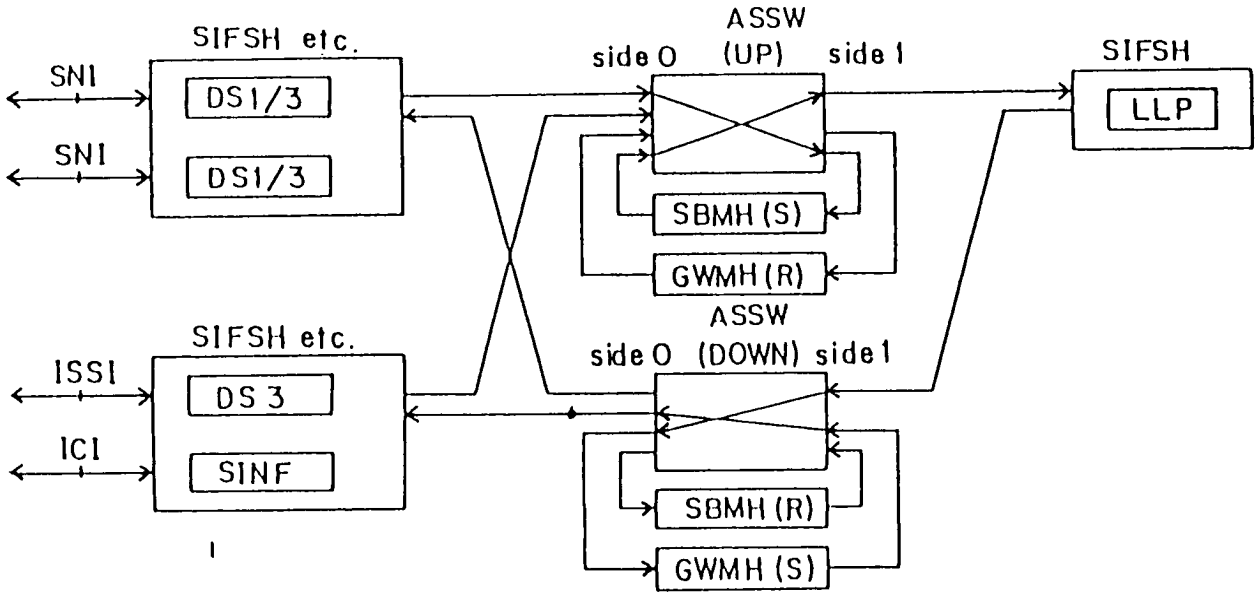


FIG. 206

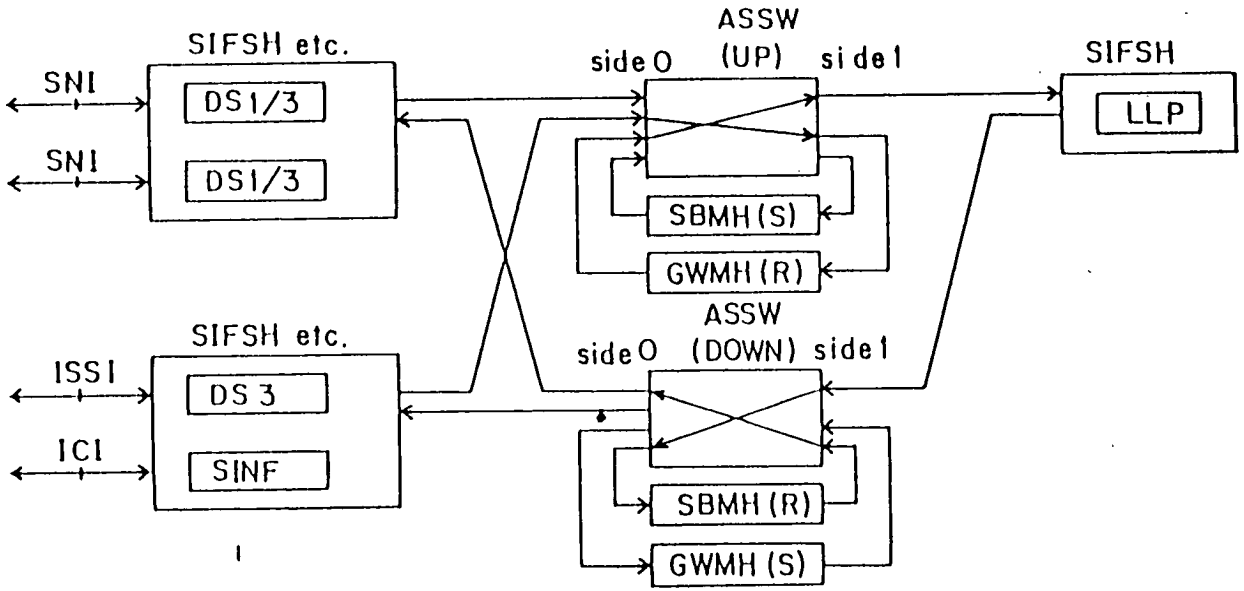

SIFSH etc.
SNI
SNI
DS1/3
DS1/3
ASSW
(UP)
side 0
side 1
SBMH (S)
GWMH (R)
SIFSH
LLP
SIFSH etc.
ISSI
ICI
DS 3
SINF
ASSW
(DOWN)
side 0
side 1
SBMH (R)
GWMH (S)

FIG. 207

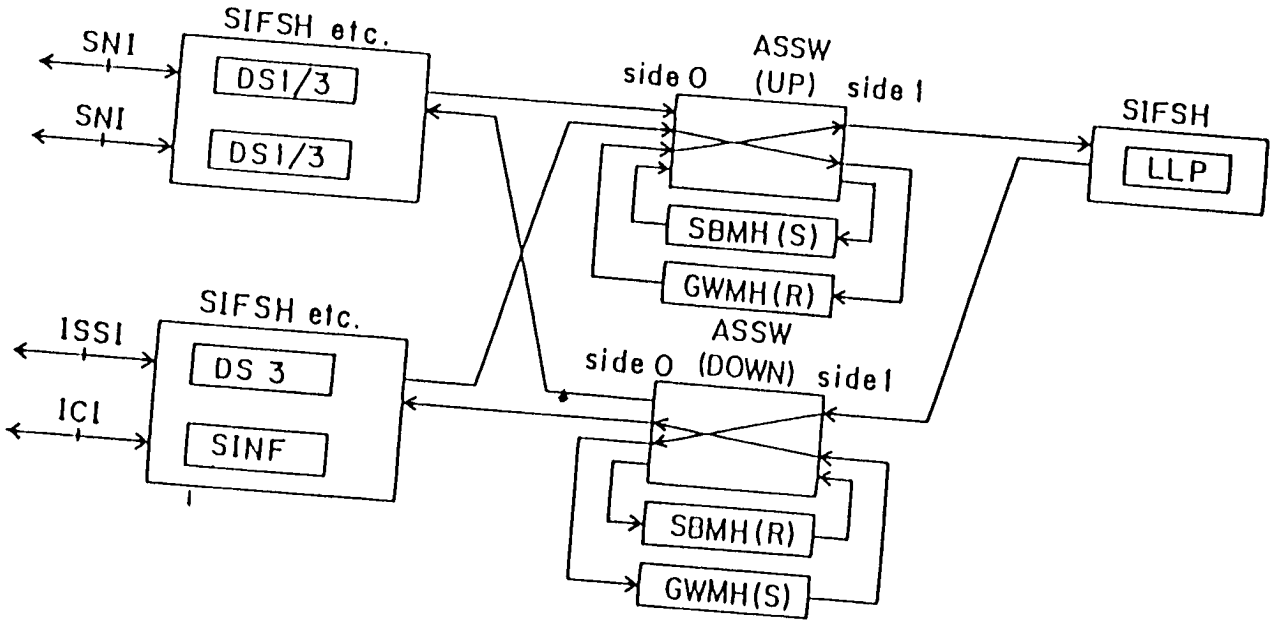

SNI
SNI
SIFSH etc.
DS1/3
DS1/3
ASSW
side 0
(UP)
side 1
SIFSH
LLP
SBMH(S)
GWMH(R)
ISSI
ICI
SIFSH etc.
DS 3
SINF
ASSW
side 0
(DOWN)
side 1
SBMH(R)
GWMH(S)

FIG. 208

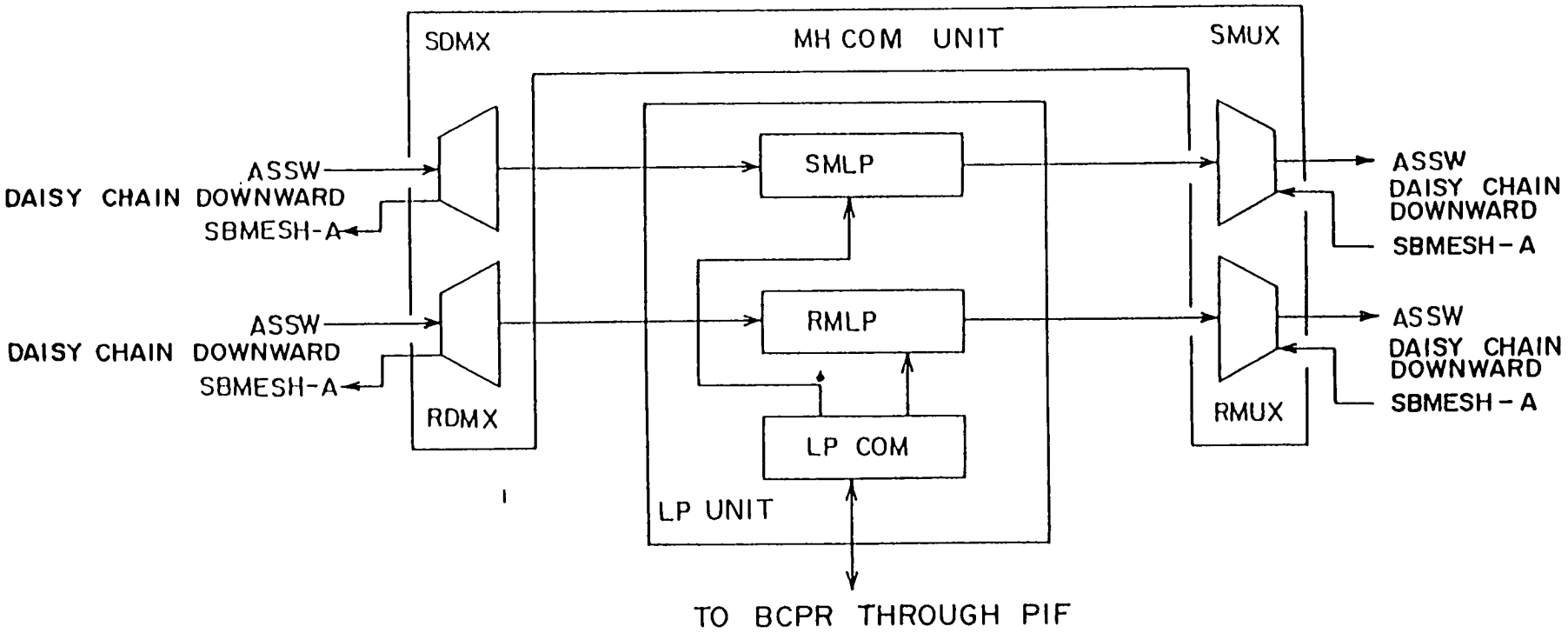

SDMX
MH COM UNIT
SMUX
ASSW
DAISY CHAIN DOWNWARD
SBMESH-A
ASSW
DAISY CHAIN DOWNWARD
SBMESH-A
SMLP
RMLP
LP COM
LP UNIT
RDMX
RMUX
ASSW
DAISY CHAIN DOWNWARD
SBMESH-A
ASSW
DAISY CHAIN DOWNWARD
SBMESH-A
TO BCPR THROUGH PIF

FIG. 209

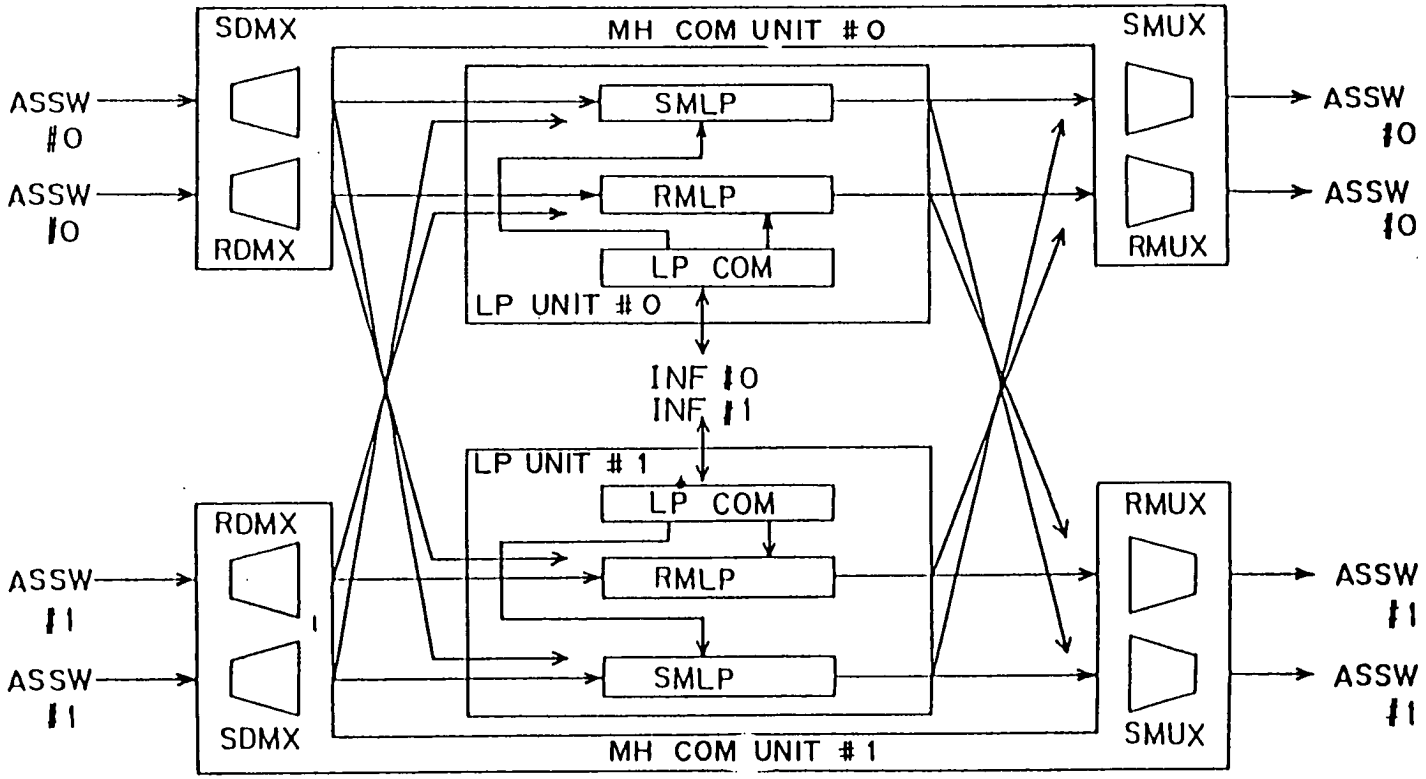

SDMX
MH COM UNIT #0
SMUX
ASSW #0
ASSW #0
SMLP
RMLP
LP COM
RDMX
LP UNIT #0
RMUX
ASSW #0
ASSW #0
INF #0
INF #1
LP UNIT #1
LP COM
RDMX
RMUX
ASSW #1
ASSW #1
RMLP
SMLP
SDMX
SMUX
MH COM UNIT #1
ASSW #1
ASSW #1

FIG. 210

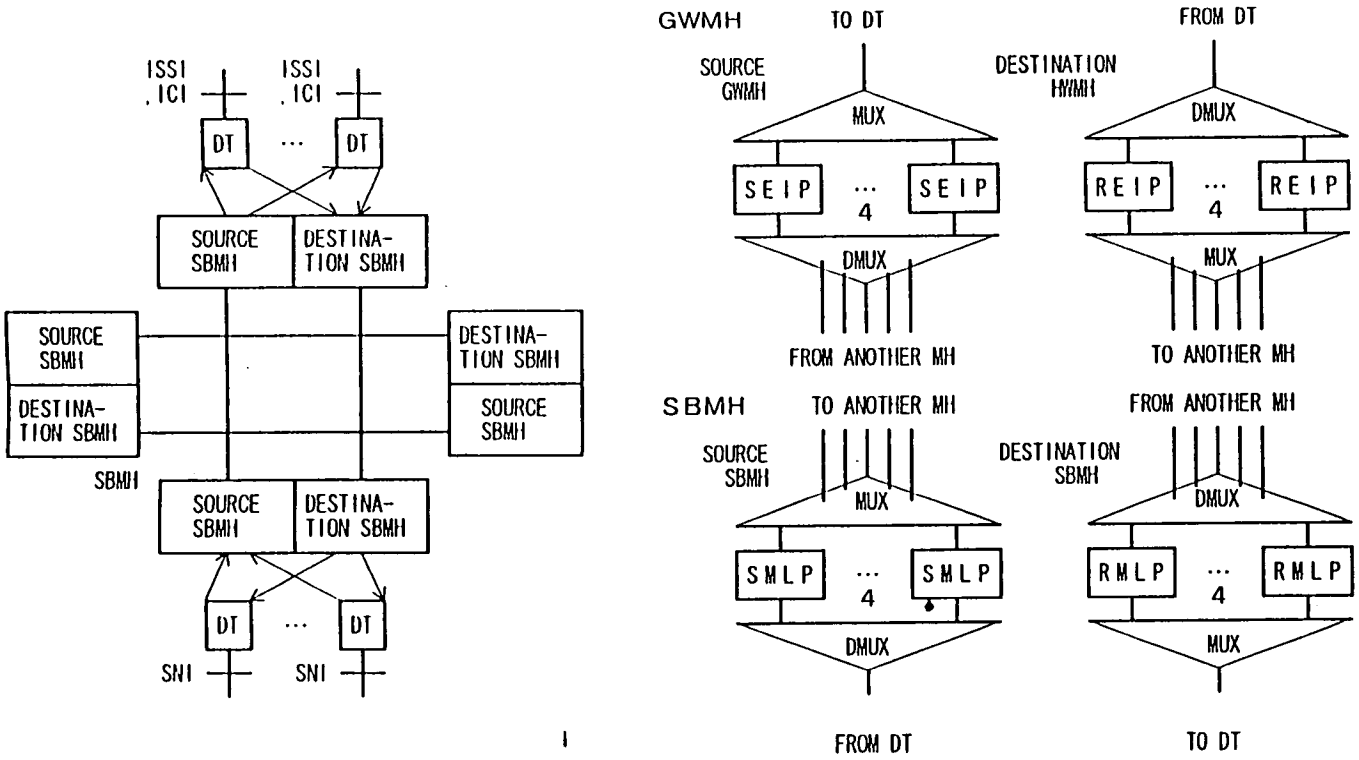
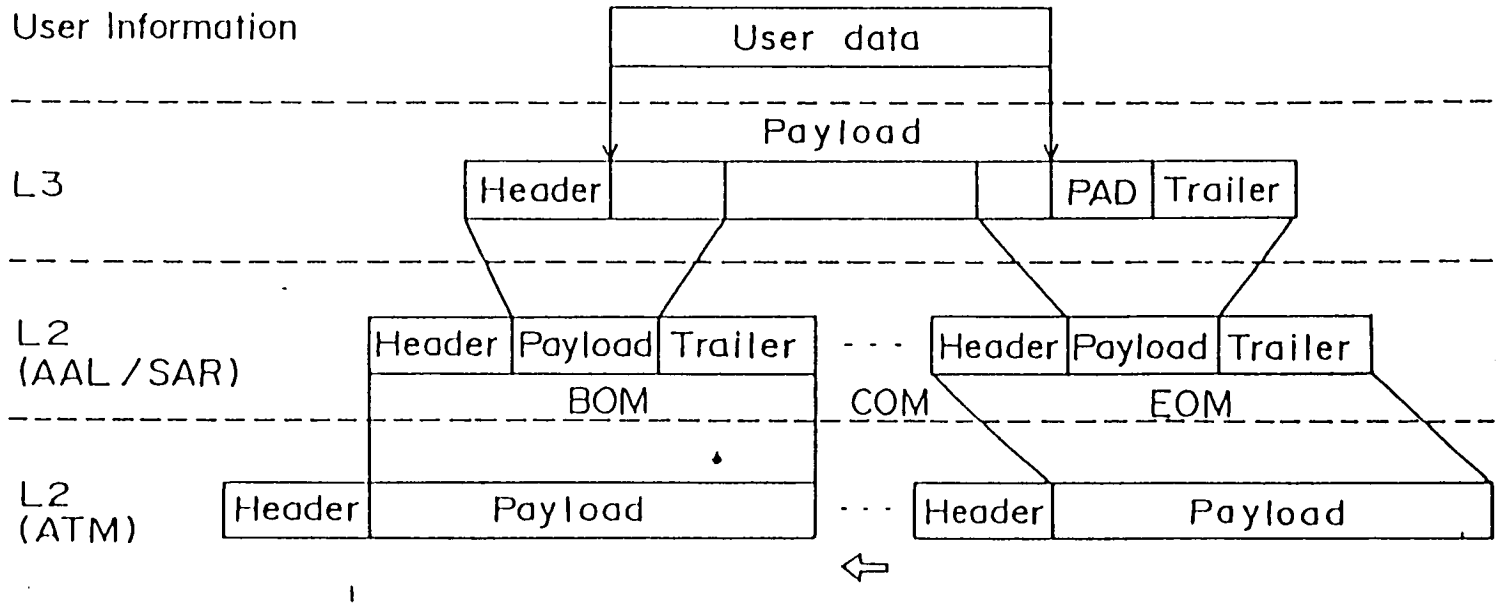

ISSI .ICI
ISSI .ICI
DT
DT
SOURCE SBMH
DESTINA-TION SBMH
SOURCE SBMH
DESTINA-TION SBMH
DESTINA-TION SBMH
SOURCE SBMH
SBMH
SOURCE SBMH
DESTINA-TION SBMH
DT
DT
SNI
SNI
GWMH
TO DT
FROM DT
SOURCE GWMH
DESTINATION HWMH
MUX
DMUX
SEIP
SEIP
4
REIP
REIP
4
DMUX
MUX
FROM ANOTHER MH
TO ANOTHER MH
SBMH
TO ANOTHER MH
FROM ANOTHER MH
SOURCE SBMH
DESTINATION SBMH
MUX
DMUX
SMLP
SMLP
4
RMLP
RMLP
4
DMUX
MUX
FROM DT
TO DT

FIG. 211



BOM : Beginning of Message
COM : Continuation of Message
EOM : End of Message
SAR : Segmention and Re-assembly

FIG. 212

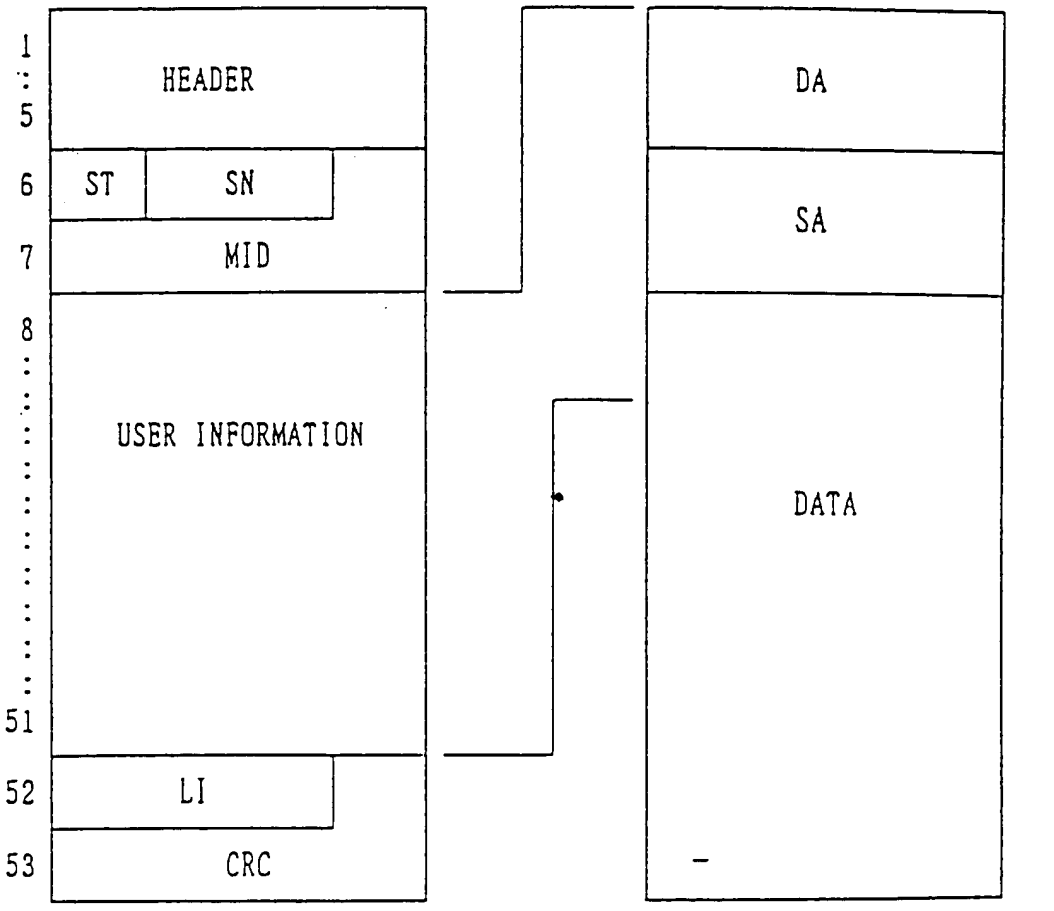

1
:
5
HEADER
6
ST
SN
7
MID
8
:
51
USER INFORMATION
52
LI
53
CRC
DA
SA
DATA
L2 PROTOCOL DATA UNIT
L3 PROTOCOL DATA UNIT
ST :Segment Type(BOM, SSM, COM, EOM)
SN :Sequence Number
MID:Message IDentifier
DA:Destination Address
SA:Source Address

FIG. 213

VCI/MID ALLOCATING SYSTEM BY CELL TYPE

	OUTPUT VCI DETERMINING SYSTEM	OUTPUT MID DETERMINING SYSTEM
SSM	DETERMINED BY DA FULL ANALYSIS	ASSIGNING NON-USED MID
BOM		
COM	RETRIEVING ROUTING MEMORY BY INPUT VCI/MID	
EOM		

FIG. 214

		SOURCE SNI	SOURCE SBMH		DESTINATION SBMH	
			DMUX	SMLP	RMLP	RMLP
ROUTING FUNCTION		VCI ALLOCATION MID ALLOCATION	LP DISTRIBUTION	VCI CONVERSION MID CONVERSION	LP DISTRIBUTION	VCI CONVERSION MID CONVERSION
USAGE INFORMATION	BOM, SSM	NONE	TAG	DA	DA	DA
	COM, EOM			VCI , MID	VCI , MID	VCI , MID

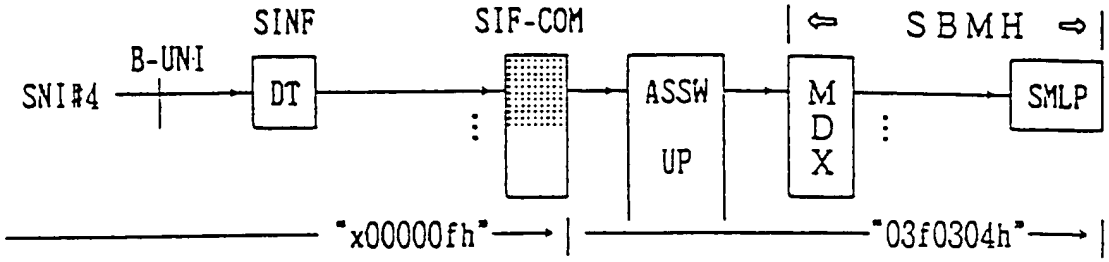
FIG. 215

6698E0 ET2726O

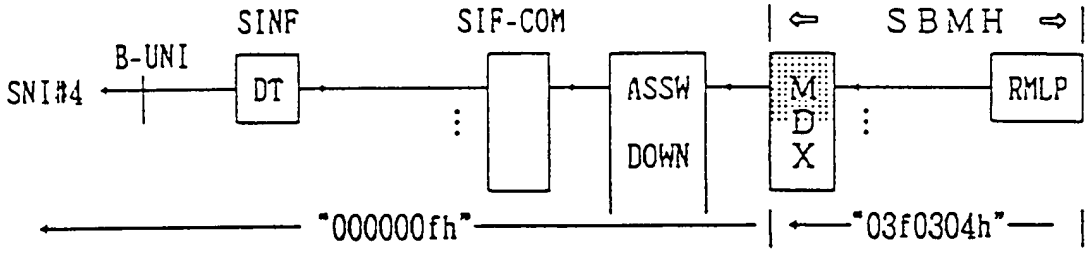
SNI No	VPI (hex)	VCI (hex)
SNI# 0	03f	0300
SNI# 1	03f	0301
⋮	⋮	⋮
SNI#31	03f	031f

FIG. 216

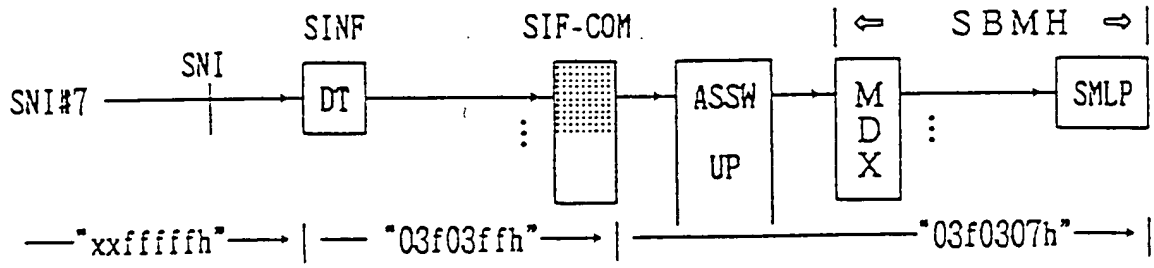
· FROM B-UNI TO SMLP (UPWARD)



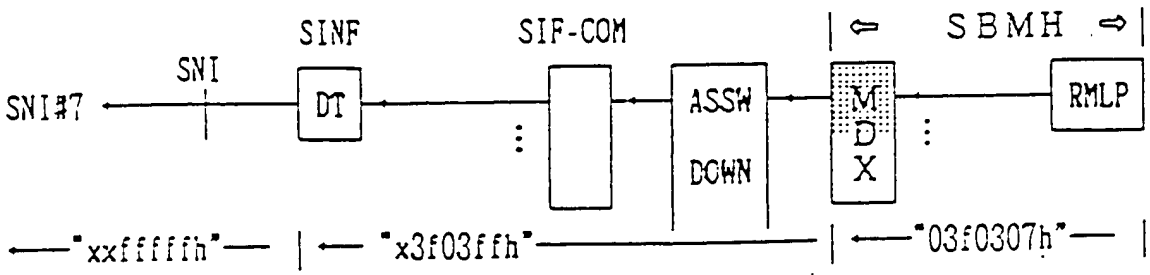
· FROM RMLP TO B-UNI (DOWNWARD)



· FROM SNI TO SMLP (UPWARD)



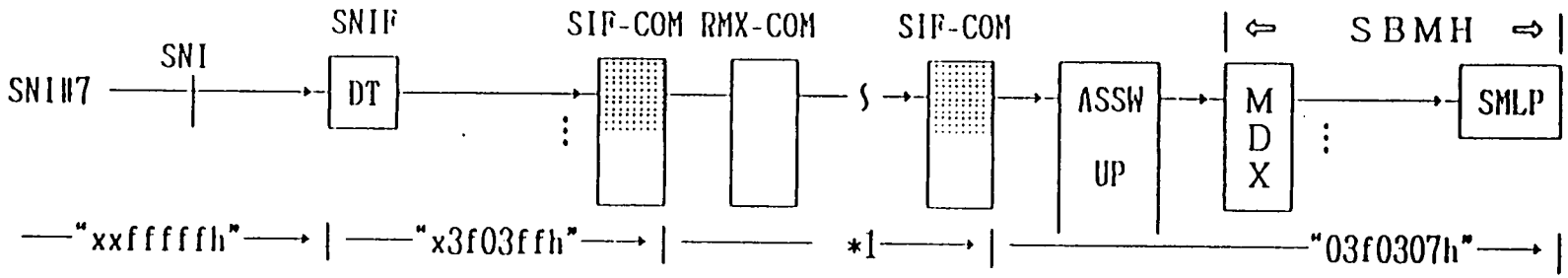
· FROM RMLP TO SNI (DOWNWARD)



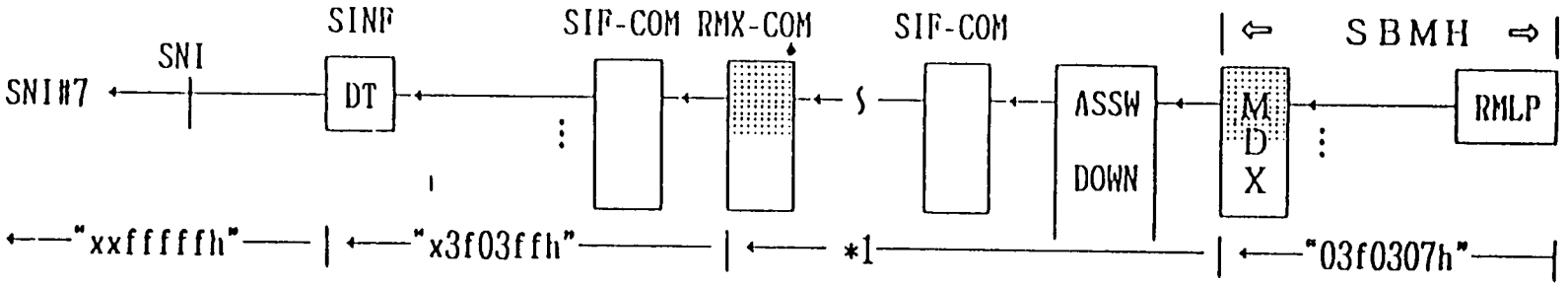
INDICATES POSITION OF VCC

FIG. 217

· FROM SNI (IN BRLC) TO SMLP (UPWARD)



· FROM RMLP TO SNI(IN BRLC) (DOWNWARD)



INDICATES POSITION OF VCC

FIG. 218

DESTINATION MH	VPI (hex)	VCI (hex)
SBMH# 0 : SBMH#31	03f : 03f	0300 : 031f
GWMH# 0 : GWMH#31	03f : 03f	0340 : 035f

NOTE : VCI INDICATES NUMBER OF RECEIVING MH BETWEEN SENDING MH AND ASSW. AND NUMBER OF SENDING MH BETWEEN ASSW AND RECEIVMG MH.

FIG. 219

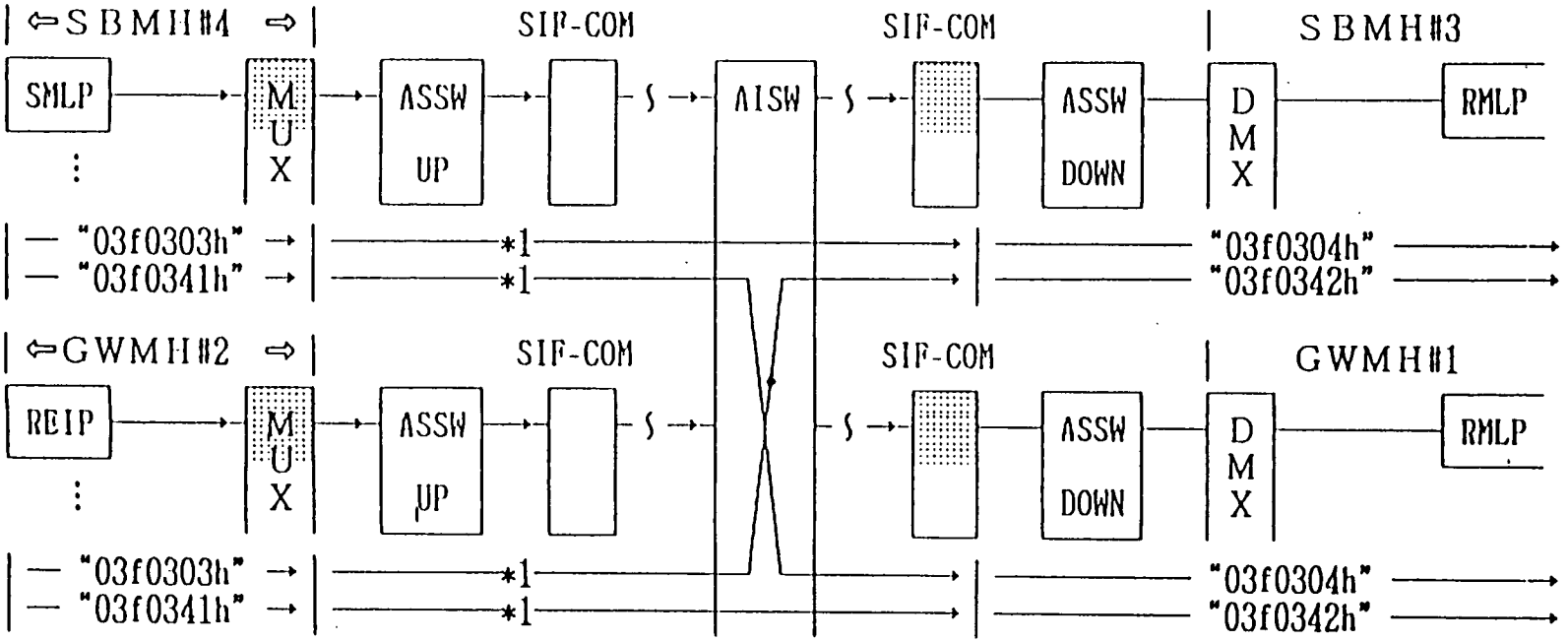
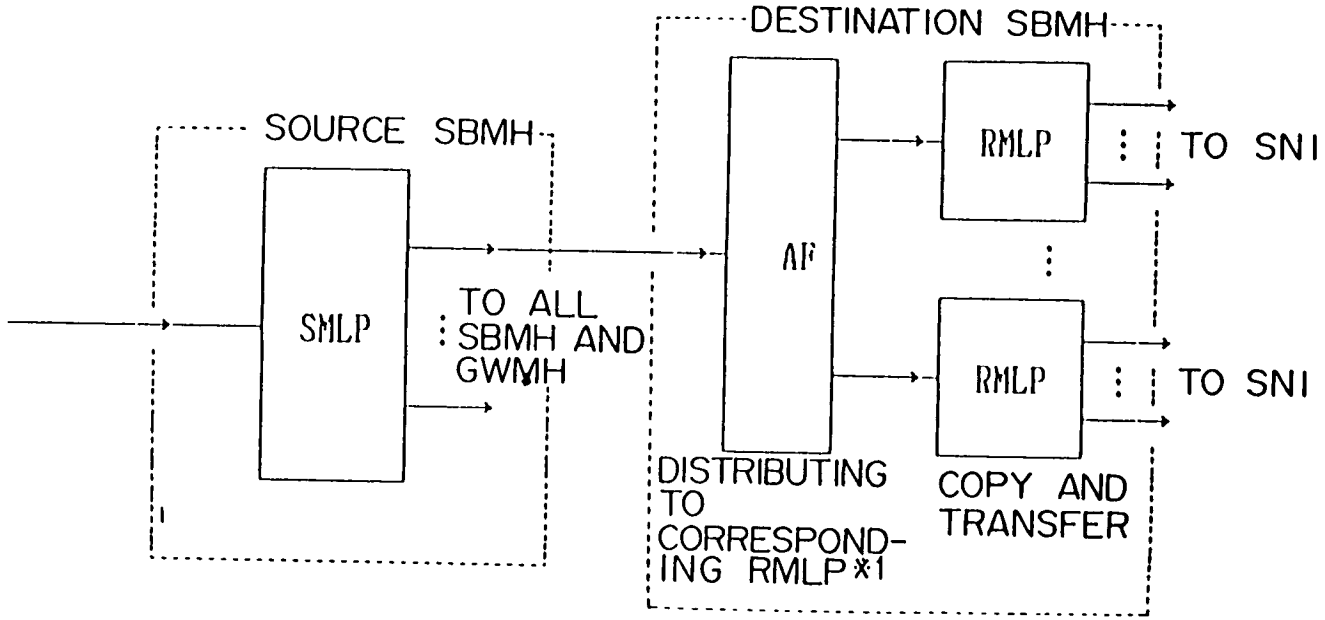

⇦SBMH#4 ⇨
SIF-COM
SIF-COM
SBMH#3
SMLP
MUX
ASSW UP
AISW
ASSW DOWN
DMX
RMLP
"03f0303h"
"03f0341h"
*1
*1
"03f0304h"
"03f0342h"
⇦GWMH#2 ⇨
SIF-COM
SIF-COM
GWMH#1
REIP
MUX
ASSW UP
ASSW DOWN
DMX
RMLP
"03f0303h"
"03f0341h"
*1
*1
"03f0304h"
"03f0342h"

FIG. 220

SMLP	RANGE OF MID (hex)
SMLP#0	000 ~ 0ff
SMLP#1	100 ~ 1ff
SMLP#2	200 ~ 2ff
SMLP#3	300 ~ 3ff

FIG. 221



*1: DISCARDED IF THERE IS NO SNI TO ACCOMMODATE CORRESPONDING GA IN DESTINATION SBMH

FIG. 222

	DETERMIN-ATION	DETERMIN-ATION AREA	PROCESS EXAMPLES
SMLP	SOURCE SNI	INPUT VCI	Screening, Traffic Measure, Etc.
	L3 PDU	INPUT VCI/MID	SN Check, Routing, Etc.
RMLP	DESTINA-TION SNI	OUTPUT VCI	Screening, Traffic Measure, Etc.
	L3 PDU	OUTPUT VCI/MID	Routing Egress Restriction, Etc.

FIG. 223

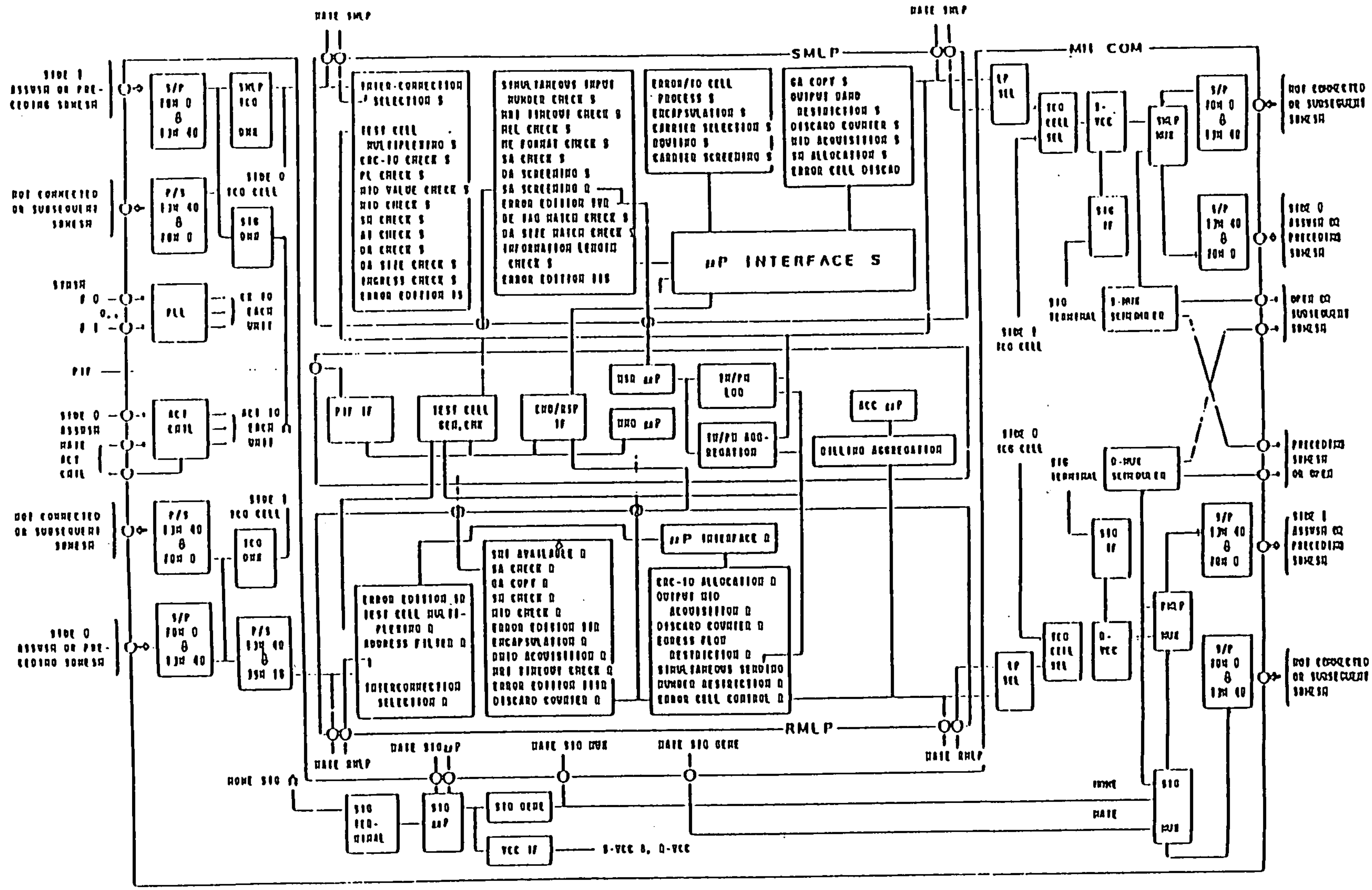

SMLP
RMLP
MII COM
μP INTERFACE S
μP INTERFACE Q
BILLING AGGREGATION

FIG. 224

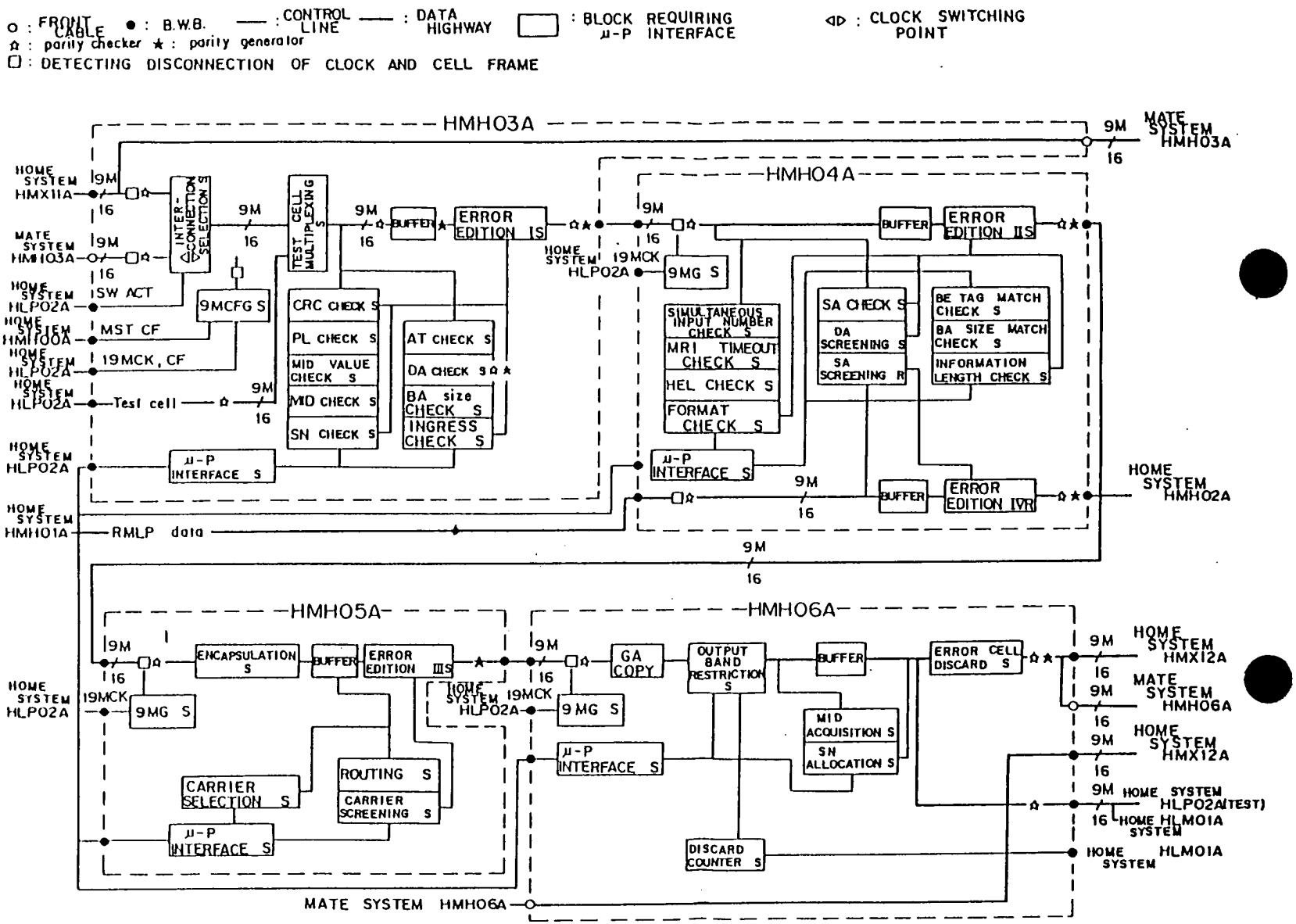

○ : FRONT CABLE
● : B.W.B.
—— : CONTROL LINE
—— : DATA HIGHWAY
: BLOCK REQUIRING μ-P INTERFACE
◁▷ : CLOCK SWITCHING POINT
☆ : parity checker ★ : parity generator
□ : DETECTING DISCONNECTION OF CLOCK AND CELL FRAME
HMH03A
HMH04A
HMH05A
HMH06A
HOME SYSTEM HMX11A
MATE SYSTEM HMH03A
HOME SYSTEM HLP02A
HOME SYSTEM HMH00A
HOME SYSTEM HMH01A
9M
16
INTER-CONNECTION SELECTION S
TEST CELL MULTIPLEXING S
BUFFER
ERROR EDITION IS
ERROR EDITION IIS
ERROR EDITION IVR
ERROR EDITION IIIS
SW ACT
MST CF
19MCK, CF
Test cell
9MCFG S
CRC CHECK S
PL CHECK S
MID VALUE CHECK S
MID CHECK S
SN CHECK S
AT CHECK S
DA CHECK S
BA size CHECK S
INGRESS CHECK S
μ-P INTERFACE S
19MCK
9MG S
SIMULTANEOUS INPUT NUMBER CHECK S
MRI TIMEOUT CHECK S
HEL CHECK S
FORMAT CHECK S
SA CHECK S
DA SCREENING S
SA SCREENING R
BE TAG MATCH CHECK S
BA SIZE MATCH CHECK S
INFORMATION LENGTH CHECK S
RMLP data
ENCAPSULATION S
CARRIER SELECTION S
ROUTING S
CARRIER SCREENING S
GA COPY
OUTPUT BAND RESTRICTION S
MID ACQUISITION S
SN ALLOCATION S
DISCARD COUNTER S
ERROR CELL DISCARD S
HOME SYSTEM HMX12A
MATE SYSTEM HMH06A
HOME SYSTEM HLP02A(TEST)
HOME SYSTEM HLM01A
MATE SYSTEM HMH06A

FIG. 225

ITEM	BLOCK NAME	CONTENTS	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	ME	CC	MS	
01	INTER-CONNECTIOM SELECTION S	SELECTING MDX ACT SYSTEM DATA ACCORDING TO SWITCH SYSTEM IMFORMATION. LOSING TCG CELL.	○	—	—	—	HMH 03A
02	TEST CELL MULTIPLEXING	MULTIPLEXING TEST CELL WHEN LINE IS IDLE. PRIORITIZING TEST CELL DURING DIAGNOSTICS.	○	○	—	—	
03	CRC-10 CHECK S	CRC DIVING CELL PAYLOAD CHECKING FOR ERRORS.	○	×	—	—	
04	PL LENGTH CHECK S	CHECKING WHETHER OR NOT PAYLOAD LENGTH INDICATES PREDEYERMINED VALUE.	○	×	○	—	
05	MID VALUE CHECK S	CHECKING WHETHER OR NOT MID VALUEE IS PREDEYERMINED VALUE.	○	×	○	—	
06	MID CHECK S	CHECKING WHETHER VCI/MID IS NOT ACTIVE AT BOM, AND WHETHER VCI/MID IS ACTIVE AT COM AND EOM.	○	×	△	—	
07	SN CHECK S	INITIALIZING SN AT BOM AND SSM. AND CHECKING ORDER OF SN AT COM AND EOM	○	×	△	—	
08	AT CHECK S	CHECKING WHETHER OR NOT ADDRESS TYPE INDICATES PREDETERMINED VALUE.	○	×	○	—	
09	DA CHECK S	CHECKING WHETHER DA IS NOT IA ENTERED IN INPUT SNI.	○	×	○	—	
10	BAsize CHECK S	CHECKING WHETHER OR NOT BA SIZE INDICATES PREDETERMINED VALUE.	○	×	○	—	
11	INGRESS FLOW CHECK S	CHECKING WHETHER OF NOT SNI OF DS3 MEETS ACCESS CLASS OF CLASSES 1-4.	○	×	×	—	
12	ERROR EDITION I	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG.	○	×	○	—	
13	SIMULTANEOUS INPUT NUMBER CHECK S	LIMITING NUMBER OF MID SIMULTANEOUSLY INPUT FROM 1 SNI TO 1 OR 16.	○	×	○	○	HMH 04A
14	MRI TIMEOUT CHECK S	CHECKING TIME FROM BOM TO EOM IN 1 L3 PDU UNITS.	○	×	○	○	
15	HEL CHECK S	CHECKING WHETHER OR NOT HEADER EXTENSION LENGTH INDICATES PREDETERMINED VALUE.	○	×	—	×	
16	HE FORMAT CHECK S	CHECKING FORMAT OF HEADER EXTENSION.	○	×	—	×	

SUB : SNI LOOPBACK TEST CELL ME : INTER-MH PVC TEST CELL CC : CRC-10-ERROR CELL MS : MASTER ERROR CELL
○ : APPLIED FOR PROCESS OBJECT OR DURING PROCESS × : NOT OBJECT OF PROCESS
— : NO CELL PASSES OR NO RELATED CELLS △ : CHECKING BUT NO WRITING TO MEMORY.

FIG. 226

ITEM	BLOCK NAME	CONTENTS	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	ME	CC	MS	
17	SA CHECK S	CHECKING WHETHER SA IS AN IA ENTERED IN INPUT SNI.	○	×	—	○	HMH 04A
18	DA SCREENING	RECEPTION IS LIMITED AT DA IN INPUT SNI UNITS. SHARED WITH TABLE OF RMLP SA SCREENING R.	○	×	—	○	
19	BE tag MATCH CHECK S	CHECKING WHETHER OR NOT BE TAG OF SIP L3 HEADER MATCHES BE TAG OF TRAILER.	○	×	—	○	
20	BA size MATCH CHECK S	CHECKING WHETHER OR NOT BA SIZE OF SIP L3 HEADER MATCHES BE LENGTH OF TRAILER.	○	×	—	○	
21	INFORMATION LENGTH CHECK S	CHECKING WHETHER OR NOT ACTUAL LENGTH OF L3 PDU MATCHES LENGTH OF SIP L3 TRAILER.	○	×	—	○	
22	ERROR EDITION II	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG.	○	×	—	○	
23	ENCAPSULATION S	CHANGING SIP INTO FORMAT OF INTER-MH INF. PDU: ADDING ISSI-L3 DTPDU HEADER AND CGV HEADER TO NEW BOM.	○	○	—	○	HMH 05A
24	CARRIER SELECTION S	SETTING SIP L3 HEADER CARRIER OR CARRIER ENTERED IN SNI UNITS IN CARRIER AREA IN ISSI L3 DTPDU HEADER.	○	○	—	○	
25	ROUTING S	SPECIFYING, FROM DA, MH(SBMH/GWMH) ACCOMMODATING DESTINATION SNI.	○	○	—	○	
26	CARRIER SCREENING S	LIMITING SENDING OF CARRIER.	○	○	—	○	
27	GA COPY S	OUTPUT CELL INPUT AT GA TO EACH SUBSCRIBER.	○	○	—	○	HMH 06A
28	OUTPUT BAND RESTRICTION S	LIMITING OUTPUT BAND(PEAK RATE) FOR EACH OUTPUT MH.	○	○	—	○	
29	DISCARD COUNT S	COUNTING NUMBER OF L2 AND L3 MESSAGES DISCARDED BY OUTPUT BAND RESTRICTION AND REPORTING IT TO PM OF LP-COM.	○	○	—	○	
30	MID ACQUISITION S	ASSIGNING OUTPUT MID TO OUTPUT MH UNIT.	○	○	—	×	
31	SN ALLOCATION S	ASSIGNING SEQUENCE NUMBER (SN).	○	○	—	○	
32	ERROR CELL DISCARD S	MASTER ERROR(MS) OF ERROR FLAG DISCARDS NG CELLS.	○	○	—	○	

SUB : SNI LOOPBACK TEST CELL ME : INTER-MH PVC TEST CELL CC : CRC-10 ERROR CELL MS : MASTER ERROR CELL
○ : APPLIED FOR PROCESS OBJECT OR DURING PROCESS × : NOT OBJECT OF PROCESS
— : NO CELL PASSES OR NO RELATED CELLS

FIG. 227

ITEM	BLOCK NAME	CONTENTS	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	ME	CC	MS	
33	μ-P INTERFACE S	INTERFACING WITH MNG μ-P OF HLP01A	—	—	—	—	COMMON TO PWCB
34	9MG S	GENERATING CLOCK BASED ON 19M CLOCK RECEIVED FROM HLP02A AND CELL FRAME	—	—	—	—	
35	9MCFG S	GENERATING 9M CLOCK BASED ON 19M CLOCK RECEIVED FROM HLP02A AND CELL FRAME, AND REFERENCE CELL FRAME BASED ON SMLP.	—	—	—	—	HMH 03A

SUB : LOOPBACK TEST CELL ME : INTER-MH PVC TEST CELL CC : ERROR CELL MS : MASTER ERROR CELL
O : APPLIED FOR PROCESS OBJECT OR DURING PROCESS × : NOT OBJECT OF PEOCESS — : NO CELL PASSES OR NO RELATED CELLS

FIG. 228

EF / MESSAGE	E1 MS	E1 RM	E2 PL	E2 IM	E1 IM	E2 MA	E1 MA	E2 SN	E2 DT	E2 ST	E2 DA	E2 BA	E2 AC	E2 EM	E2 MT	E2 HE	E2 VE	E2 CS	E2 SA	E2 DA	E2 BE	E2 LE	E2 IL	E2 EB	PV C
CRC-10 CHECK S	ON	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
PL LENGTH CHECK S	ON	ON	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
MID VALUE CHECK S (S/B)	ON	ON	—	ON		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
MID CHECK S (B)		O	—	—	—	ON		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
MID CHECK S (E)	ON	O	—	—	—	ON		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
MID CHECK S (C)	ON	O	—	—	—		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
SN CHECK S	ON	O	—	—	—	O	O	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
ADDRESS FORMAT CHECK S (DA)	ON	—	—	—	—	—	—	—	ON		—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
ADDRESS FORMAT CHECK S (SA)	ON	—	—	—	—	⊥	—	—		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M

'ON' : EF WHICH IS SET ON WHEN CHECK RESULT INDICATES NG. '—' : CHECK IS MADE REGARDLESS OF OK/NG OF EF WITH THIS MARK.
'O' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK. 'M' : NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 229

BLOCK NAME \ EF	E1 MS	E1 RM	E2 PL	E2 IM	E1 IM	E2 MA	E1 MA	E2 SM	E2 DT	E2 ST	E2 DA	E2 BA	E2 AC	E2 EM	E2 MT	E2 HE	E2 VE	E2 CS	E2 SA	E2 DA	E2 BE	E2 LE	E2 IL	E2 EB	PV C
DA CHECK S (B/S)	ON	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	M
BA SIZE CHECK S (B/S)	ON	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	—	—	—	M
INGRESS FLOW CHECK S (B/S)	ON	O	—	—	—	—	—	—	—	—	—	O	ON	—	—	—	—	—	—	—	—	—	—	—	M
SIMULTANEOUS INPUT NUMBER CHECK S (E)	ON O	O	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	—	M
SIMULTANEOUS INPUT NUMBER CHECK S (C)	ON O	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
MRI TIME OUT S (E)	ON O	O	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	M
HEL CHECK S (B/S)	ON O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	M
HE FORMAT CHECK S - 1ST (B/S)	ON O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	♦ —	ON	—	—	—	—	—	—	—	M
HE FORMAT CHECK S - 2ND (B/S)	ON O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON —	—	—	—	—	—	—	M
SA CHECK A (B/S)	ON —	—	—	—	—	—	—	↓ —	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	

'ON' : EF WHICH IS SET ON WHEN CHECK RESULT INDICATES NG. '—' : CHECK IS MADE REGARDLESS OF OK/NG OF EF WITH THIS MARK.
'O' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK. 'M' : NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 230

EF / BLOCK NAME	E1 MS	E1 RM	E2 PL	E2 IM	E1 IM	E2 MA	E1 MA	E2 SN	E2 DT	E2 ST	E2 DA	E2 BA	E2 AC	E2 EM	E2 MT	E2 HE	E2 VE	E2 CS	E2 SA	E2 DA	E2 BE	E2 LE	E2 IL	E2 EB	PVC
DA SCREENING S (B/S)	ON —	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	M
BE TAG MATCH S (E)	ON —	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	O	—	M
BA SIZE MATCH CHECK S (E)	ON —	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	O	ON	O	—	M
INFORMATION LENGTH CHECK S (S/C/E)	ON —	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	M
ENCAPSULATION S (C/E)	ON *1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
	*1 WHEN L2-PDU WHOSE 'EIMS' IS ON IS RECEIVED AT BOM AND COM HAVING SAME RMID VALUE, SUBSEQUENTLY RECEIVED COM AND EOM HAVE 'EIMS' SET 'ON'.																								
CARRIER SELECTION S (ISSIB)	ON O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	M
ROUTING S	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
CARRIER SCREENING (ISSIB)	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
GA COPY S (C/E)	*2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
	*2 BOM WHOSE 'EFMS' INDICATES NG (ON) IS NOT COPIED, BUT ORIGINAL CELL IS SET MHID AND TRANSMITTED IF COM AND EOM ARE FIRST NG CELL, THEY ARE COPIED.																								

'ON' : EF WHICH IS SET ON WHEN CHECK RESULT INDICATES NG. '—' : CHECK IS MADE REGARDLESS OF OK/NG OF EF WITH THIS MARK.
'O' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK. 'M' : NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 231

EF / BLOCK NAME	E1 MS	E1 RM	E2 PL	E2 IM	E1 IN	E2 MA	E1 MA	E2 SN	E2 DT	E2 ST	E2 DA	E2 BA	E2 AC	E2 EM	E2 MT	E2 HE	E2 VE	E2 CS	E2 SA	E2 DA	E2 BE	E2 LE	E2 IL	E2 EB	E2 C
OUTPUT BAND CONTROL S	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
NID ACQUISITION S	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SN ASSIGNMENT S	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ERROR CELL DISCARD S	×	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

'ON' : EF WHICH IS SET ON WHEN CGECK RESULT INDICATES NG.
'O' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK.
'×' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES NG.
'—' : CHECK IS MADE REGARDLESS OF OK/NG OF EF WITH THIS MARK.
'M' : NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 232

DATA INTERFACE OF SMLP AND LPCOM

SENDING PROCESS UNIT⇨PM UNIT, TM UNIT, TEST CELL RECEIVING UNIT INTERFACE (TRANSMITTED FROM SAME INTERFACE)

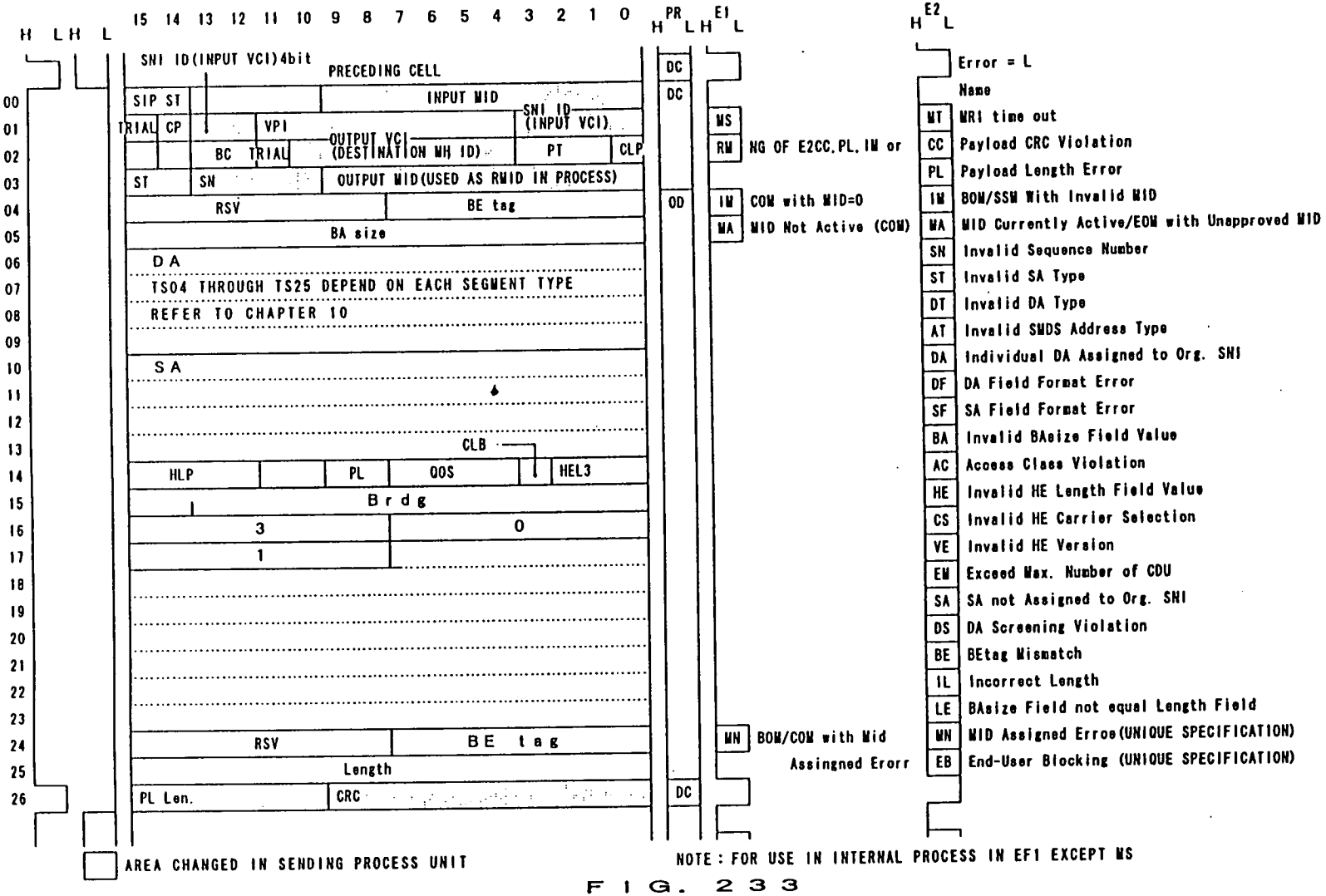
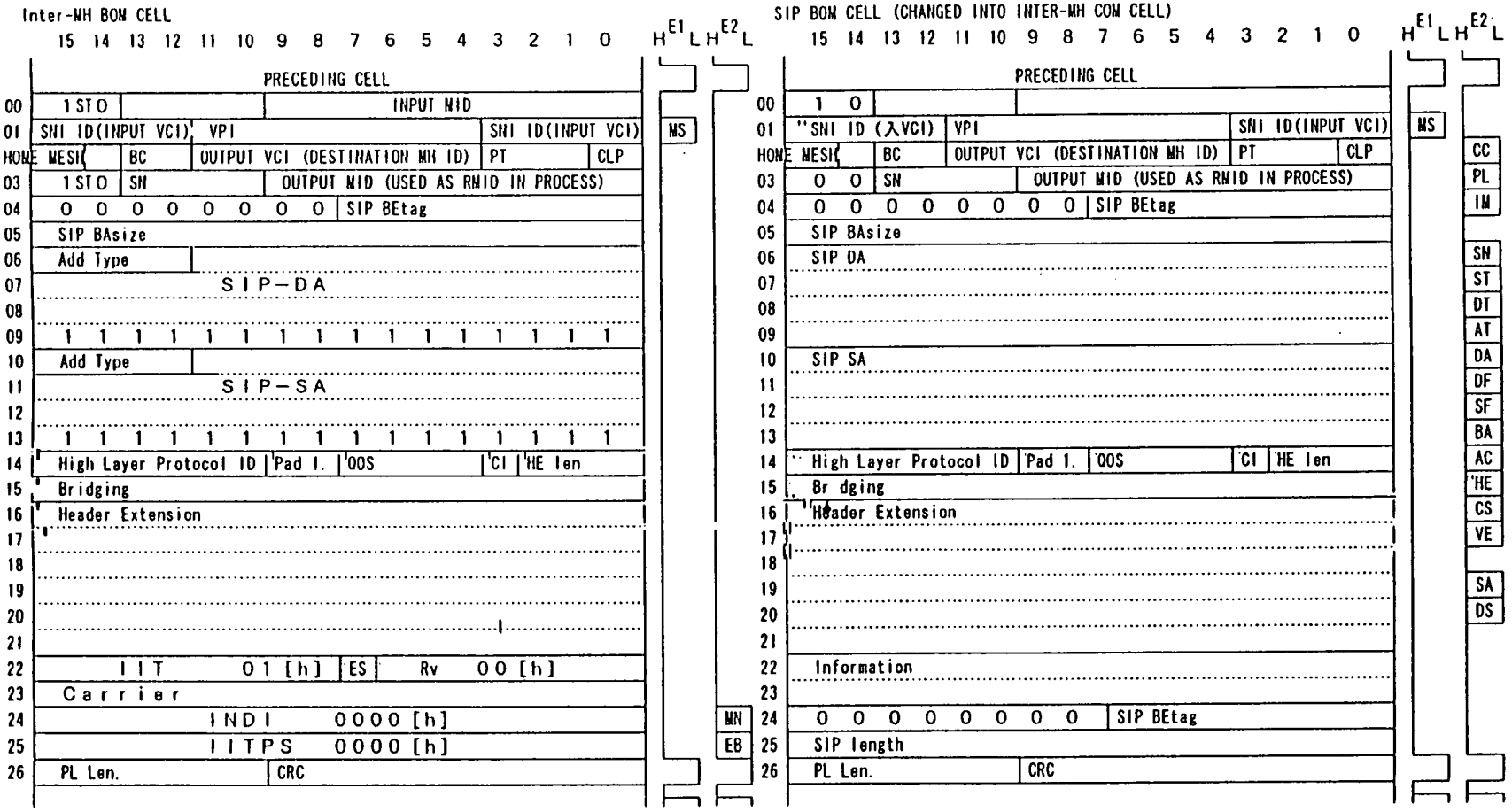


FIG. 233

SIP ST :	ST OF SIP FORMAT IS ENTERED. (ASSIGNED IN ERROR EDITION I).
BC :	INDICATES WHERE TO BROADCAST TO. (ASSIGNED IN ROOUTING PROCESS UNIT).
DESTINATION MH ID :	INDICATES OUTPUT VCI (DESTINATION MH ID).
TRIAL :	INDICATES WHETHER OR NOT IT IS PVC TEST CELL (INTERMESH/SNI LOOPBACK). TEST CELL IS 1. (ASSIGNED BEFORE CRC-10 CHECK PROCESS UNIT BETWEEN MESHS. ASSIGNED AT ROUTING PROCESS UNIT AT SNI LOOPBACK)
SNI ID :	8-BIT LSB OF VCI INPUT FROM MDX. INDICATES SOURCE SNI ID. 15-12 IS 4-BIT MSB (1-BIT MSB IS TEST BIT), AND 3-0 IS 4-BIT LSB (MOVED IN ERROR EDITION I).
HOME MESH :	INDICATES WHETHER OR NOT IT IS LOOPBACK CELL TO HOME MESH (ASSIGNED IN DA CHECK PROCESS UNIT. LOOPBACK CELL TO HOME MESH DOES NOT REQUIRE RETRIEVAL OF ROUTE INFORMATION IN ROUTING PROCESS UNIT).
OUTPUT VCI :	DESTINATION MH ID. 1-BIT MSB OF TEST CELL IS 1.
PT :	PAYLOAD TYPE (NOT CHANGED IN PROCESS UNIT).
CLP :	CELL LOSS PRIORITY (NOT CHANGED IN PROCESS UNIT).
ST :	SEGMENT TYPE OF INTER-MH (REASSIGNMENT FROM SIP IN ENCAPSULATION PROCESS UNIT).
SN :	SEQUENCE NUMBER (REASSIGNMENT IN SN ASSIGNING UNIT).
MID :	MESSAGE IDENTIFIER 1. RMID FROM VCI AND MID IS ENTERED IN SIMULTANEOUS INPUT NUMBER CHECK UNIT. 2. OUTPUT MID IS ENTERED IN MID ACQUIRING UNIT.
SAR PL :	SAR PAYLOAD,
PL :	PL OF SIP IS INPUT.
CRC :	REASSIGNED IN CRC-10 ASSIGNING UNIT.
CP :	0 FOR ORIGINAL CELL, AND 1 FOR COPIED CELL.

FIG. 234



SINCE ERROR CELL IS NOT ENCAPSULATED, NO ERROR FLAG OTHER THAN E2MN AND E2EB IS SET.

FIG. 235

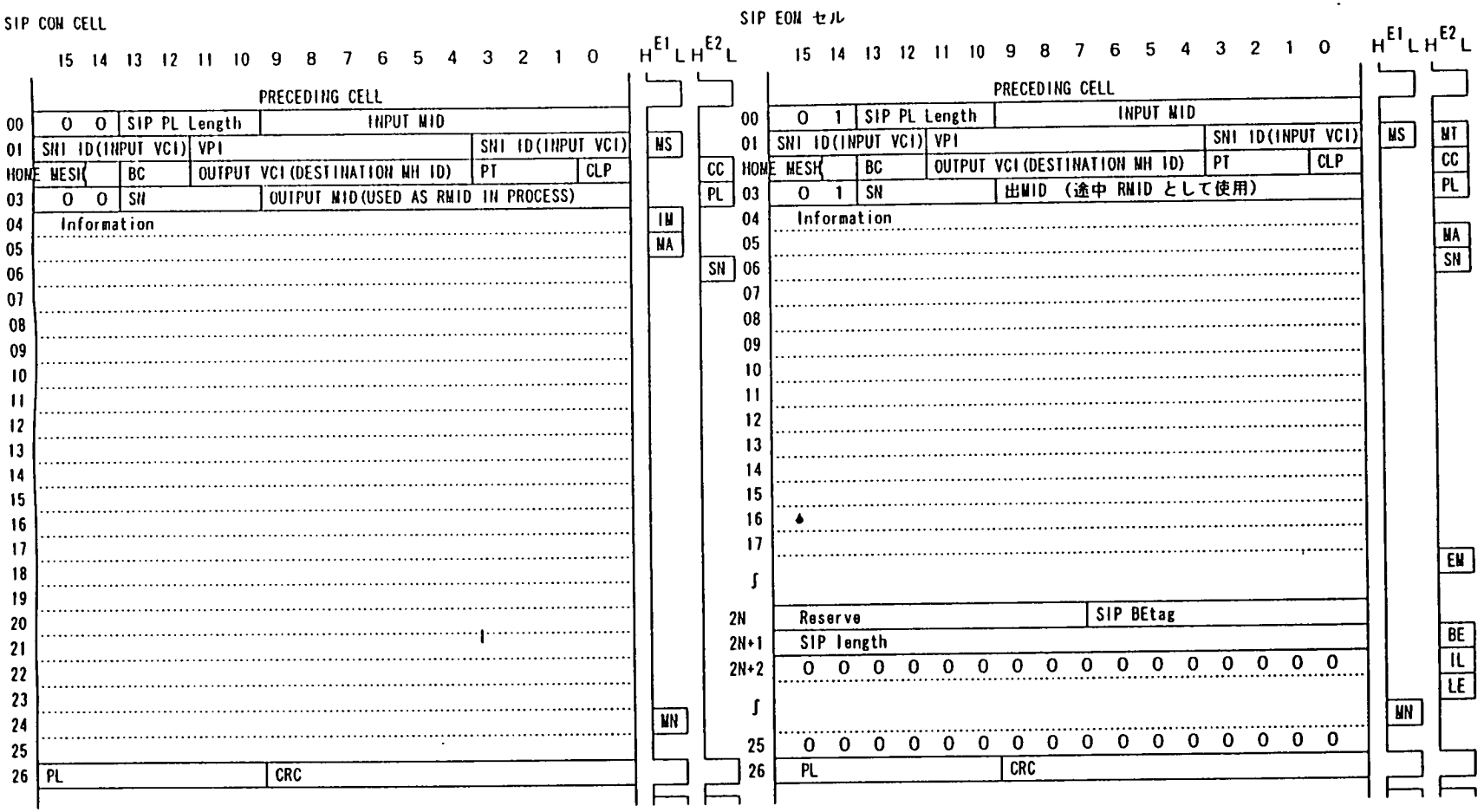

SIP CON CELL
SIP EOM セル
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
H EI L H E2 L
PRECEDING CELL
00 0 0 SIP PL Length INPUT MID
01 SNI ID(INPUT VCI) VPI SNI ID(INPUT VCI)
HOME MESH BC OUTPUT VCI(DESTINATION NH ID) PT CLP
03 0 0 SN OUTPUT MID(USED AS RNID IN PROCESS)
04 Information
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26 PL CRC
MS
CC
PL
IM
MA
SN
MN
0 1 SIP PL Length INPUT MID
SNI ID(INPUT VCI) VPI SNI ID(INPUT VCI)
HOME MESH BC OUTPUT VCI(DESTINATION NH ID) PT CLP
0 1 SN 出MID (途中 RNID として使用)
Information
2N Reserve SIP BEtag
2N+1 SIP length
2N+2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
25 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
26 PL CRC
MS
MN
MT
CC
PL
MA
SN
EM
BE
IL
LE

FIG. 236

SIP SSM セル (CHANGED INTO INTER-MH BOM CELL)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	H E1 L	H E2 L
	PRECEDING CELL																	
00	1	1	SIP PL Length						INPUT MID									
01	SNI ID(INPUT VCI)				VPI								SNI ID(INPUT VCI)				MS	
HOME MESH			BC		OUTPUT VCI(DESTINATION ID)								PT			CLCLP		CC
03	0	1	SN		OUTPUT MID(USED AS RNID IN PROCESS)													PL
04	0	0	0	0	0	0	0	0	SIP BEtag									IM
05	SIP P BAsize																	
06	SIP P DA																	SN
07																		ST
08																		DT
09																		AT
10	SIP P SA																	DA
11																		DF
12																		SF
13																		BA
14	Highgh Layer Protocol ID				Pad 1.		QOS				CI		HE len					AC
15	Bridiдging																	HE
16	Headader Extension																	CS
17																		VE
18																		
19																		SA
20																		DS
21																		BE
22	Infoformation																	IL
23																		LE
24	0	0	0	0	0	0	0	0	SIP BEtag									
25	SIP length																	
26	PL Len.						CRC											

FIG. 237

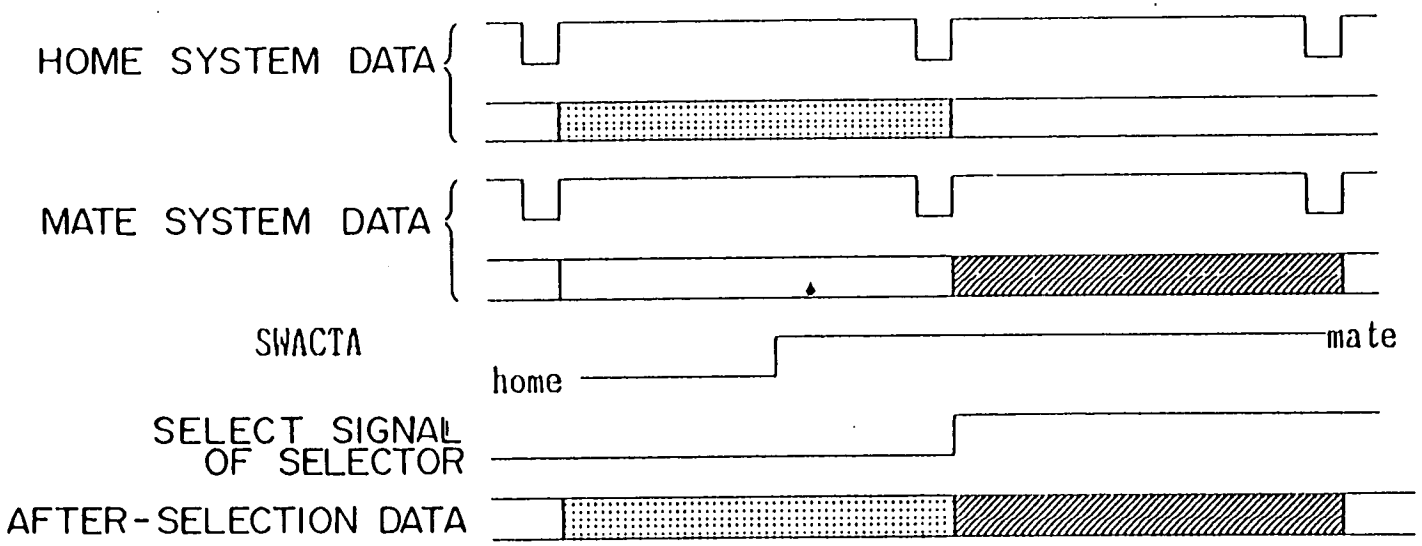

HOME SYSTEM DATA
MATE SYSTEM DATA
SWACTA
home
mate
SELECT SIGNAL OF SELECTOR
AFTER-SELECTION DATA

FIG. 238

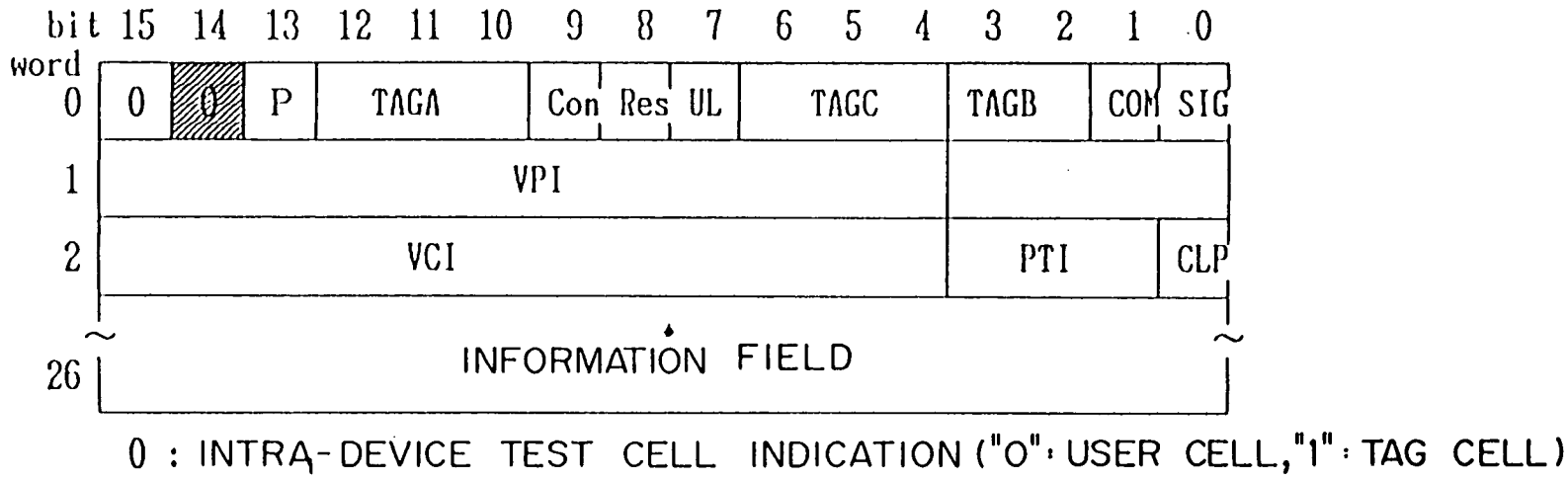

bit 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
word
0
0
0
P
TAGA
Con
Res
UL
TAGC
TAGB
COM
SIG
1
VPI
2
VCI
PTI
CLP
26
INFORMATION FIELD
0 : INTRA-DEVICE TEST CELL INDICATION ("0": USER CELL, "1": TAG CELL)

FIG. 239

6698260 "ET82260

INPUT			OUTPUT		
LP UNIT STATUS	LINE CELL ENB	TEST CELL ENB	CELL ENB	CELL	TEST CELL FETCH TSOK
IN NORMAL OPERATION	ENB	DSB	ENB	LINE CELL	NG
	ENB	ENB	ENB	LINE CELL	NG
	DSB	ENB	ENB	TEST CELL	OK
	DSB	DSB	DSB	LINE CELL	NG
IN DIAGNOSTICS	DSB BY COMPULSORY MASK	ENB	ENB	TEST CELL	OK
		DSB	DSB	TEST CELL	NG

ENB : ENABLE (ENABLE CELL)
DSB : DISABLE (DISABLE CELL)

FIG. 240

INPUT	OUTPUT
RESIDUAL CELL PAYLOAD	EFCC
0	OFF
OTHER THAN 0	ON

FIG. 241

ST	ERROR CONDITION		
BOM	PL ≠ 44 OCTET	———	PL IS NOT MULTIPLE OF 4 OCTETS.
COM	PL ≠ 44 OCTET	———	PL IS NOT MULTIPLE OF 4 OCTETS.
EOM	4 OCTET > PL	4 OCTET < PL	PL IS NOT MULTIPLE OF 4 OCTETS.
SSM	28 OCTET > PL	44 OCTET < PL	PL IS NOT MULTIPLE OF 4 OCTETS.

FIG. 242

5,052,042

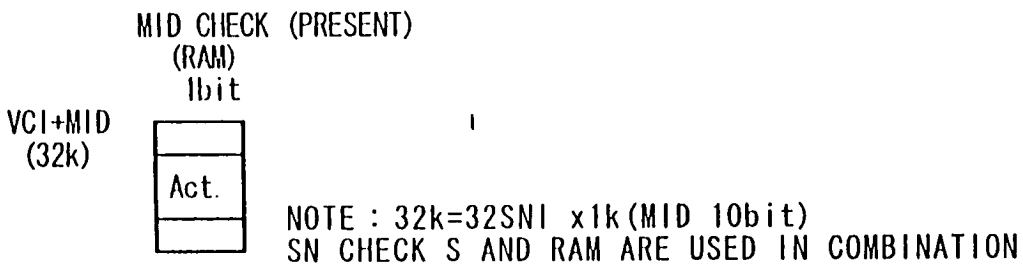
ST	ERROR CONDITION	E1 EFIM	E2 EFIM
BOM	MID = 0	OFF	ON
COM	MID = 0	ON	OFF
EOM	MID = 0	OFF	ON
SSM	MID≠ 0	ON	ON

FIG. 243

5,535,205

INPUT		OUTPUT		
		EF1	EF2	
ST	MID CHECK	MA	MA	MID CHECK
BOM	not ACT	OFF	OFF	ACT
BOM	ACT	OFF	ON	ACT
COM	ACT	OFF	OFF	ACT
COM	not ACT	ON	OFF	not ACT
EOM	ACT	OFF	OFF	not ACT
EOM	not ACT	OFF	ON	not ACT

*1 : ERROR FLAG(EF2MA) IS SET,
BUT MASTER ERROR FLAG(EF1MS) IS NOT SET.



NOTE : 32k=32SNI x1k(MID 10bit)
SN CHECK S AND RAM ARE USED IN COMBINATION

FIG. 244

I INPUT			OUTPUT	
ST	CELL SN	SN CHECK	EFSN	SN CHECK
BOM, SSM	SN	D. C.	OFF	SN+1
COM, EOM	SN	SN	OFF	SN+1
COM, EOM	SN	≠SN	ON	SN+1

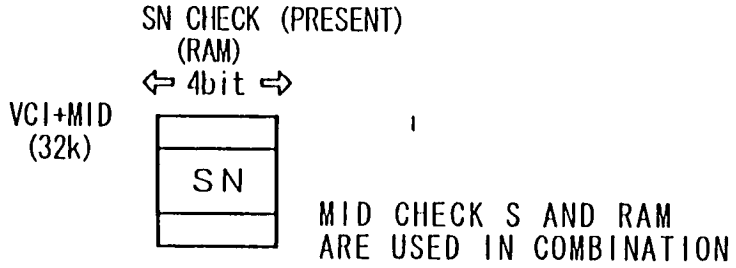


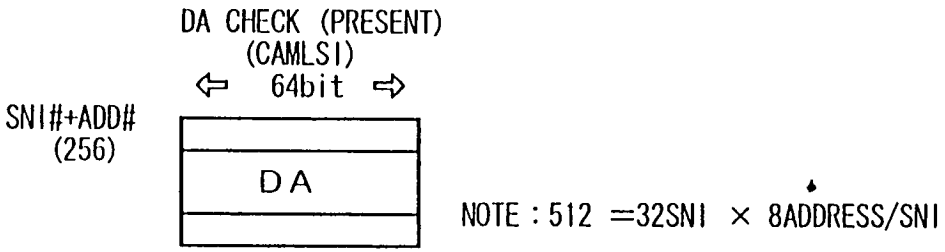
FIG. 245

ST		ERROR CONDITION(ADDRESS TYPE 4BIT)	EFDT	EFST
BOM SSM	DA	VALUE OTHER THAN 1100 OR 1110	ON	OFF
	SA	VALUE OTHER THAN 1100	OFF	ON

FIG. 246

INPUT			OUTPUT
		*1	
ST	DA CHECK	MATCHING ADDRESS	EFSA
BOM, SSM	No Match	D.C.	*2
BOM, SSM	Match	≠SNI#	*3
BOM, SSM	Match	=SNI#	
COM, EOM	D.C.	D.C.	ACT

*1 : MATCHING ADDRESS MSB 4bit
*2 : ROUTE RETRIEVAL IS REQUIRED IN ROUTING UNIT
*3 : ROUTE RETRIEVAL IS REQUIRED IN ROUTING UNIT



NOTE : 512 =32SNI × 8ADDRESS/SNI

FIG. 247

ST	ERROR CONDITION
BOM, SSM	BASIZE<320CTETS, BASIZE >92224CTETS

FIG. 248

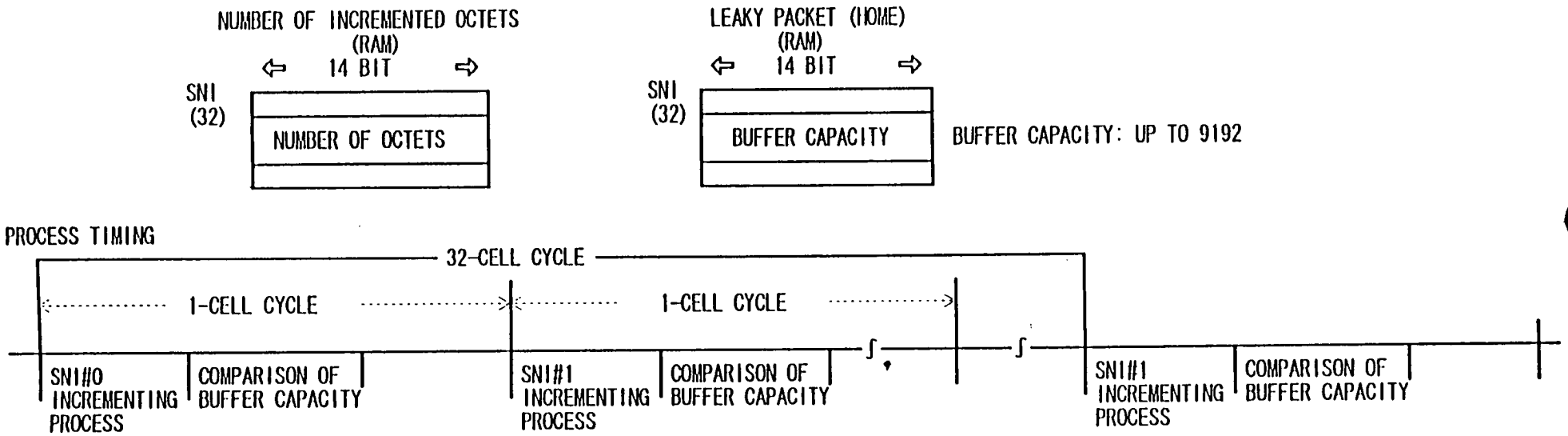

NUMBER OF INCREMENTED OCTETS
(RAM)
14 BIT
SNI
(32)
NUMBER OF OCTETS
LEAKY PACKET (HOME)
(RAM)
14 BIT
SNI
(32)
BUFFER CAPACITY
BUFFER CAPACITY: UP TO 9192
PROCESS TIMING
32-CELL CYCLE
1-CELL CYCLE
1-CELL CYCLE
SNI#0 INCREMENTING PROCESS
COMPARISON OF BUFFER CAPACITY
SNI#1 INCREMENTING PROCESS
COMPARISON OF BUFFER CAPACITY
SNI#1 INCREMENTING PROCESS
COMPARISON OF BUFFER CAPACITY

FIG. 249

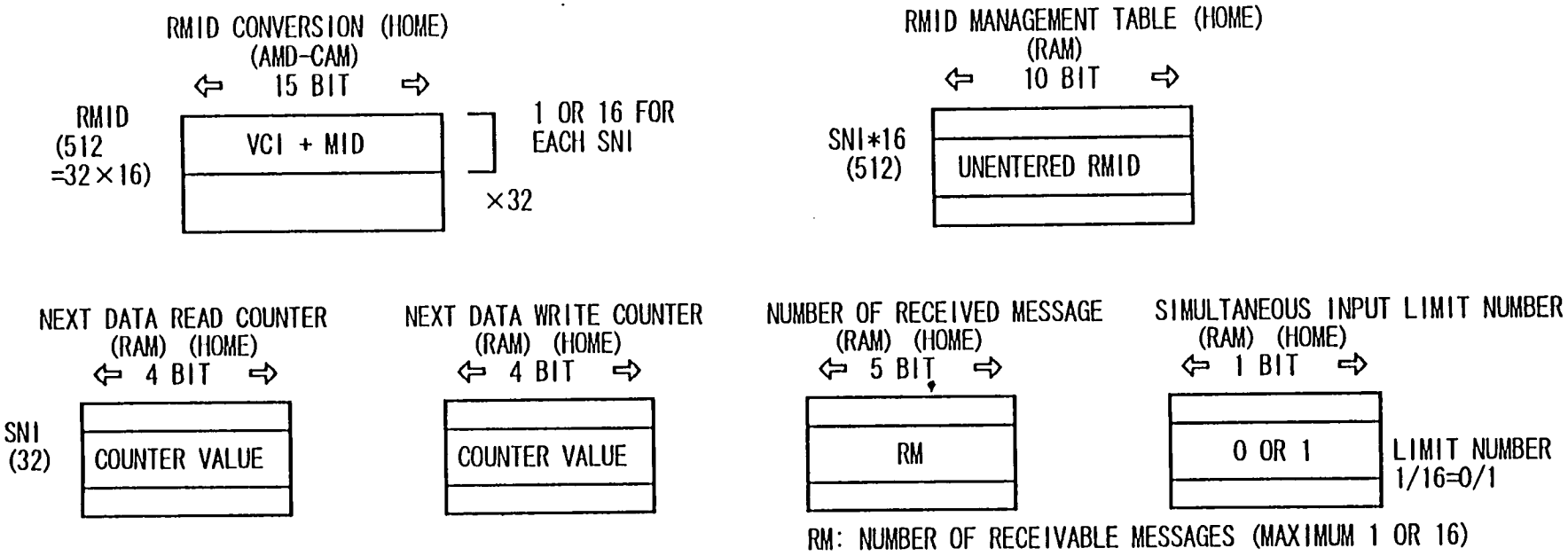

RMID CONVERSION (HOME)
(AMD-CAM)
15 BIT
RMID
(512
=32×16)
VCI + MID
1 OR 16 FOR
EACH SNI
×32
RMID MANAGEMENT TABLE (HOME)
(RAM)
10 BIT
SNI*16
(512)
UNENTERED RMID
NEXT DATA READ COUNTER
(RAM) (HOME)
4 BIT
SNI
(32)
COUNTER VALUE
NEXT DATA WRITE COUNTER
(RAM) (HOME)
4 BIT
COUNTER VALUE
NUMBER OF RECEIVED MESSAGE
(RAM) (HOME)
5 BIT
RM
SIMULTANEOUS INPUT LIMIT NUMBER
(RAM) (HOME)
1 BIT
0 OR 1
LIMIT NUMBER
1/16=0/1
RM: NUMBER OF RECEIVABLE MESSAGES (MAXIMUM 1 OR 16)

FIG. 250

6693260 "EP2772860

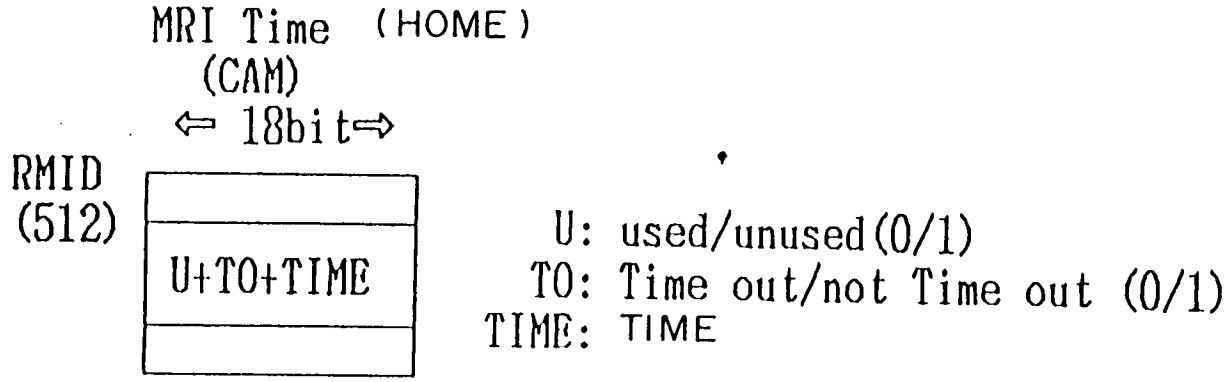


FIG. 251

READ AND WRITE DATA TO RMID CONVERSION CAM AND MRI CAM

INPUT \ CAM	RMID CONVERSION		MRMR I		OUTPUT	RMID CONVERSION	MR I
TYPE	MATCHING DATA	RESULT	MATCHING DATA	RESULT	ERROR FLAG	WRITE DATA	WRITE DATA
FOR EACH CELL FRAME (FOR IDLE CELL)	——		0+1+PRESENT TIME	MATCHING	EFMT*1	ALL 1	ALL 1
FOR EACH CELL FRAME (FOR BOM, COM, EOM, AND SSM)	——		0+1+PRESENT TIME	MATCHING	——	——	0+1+TO TIME
FOR EACH CELL FRAME (FOR ALL CELLS)	——		0+1+PRESENT TIME	NON-MATCHING	——	——	——
IDLE CELL (WHEN MRI MATCHING FOR CELL FRAME)	——		NO MATCHING OPERATION		REFER TO ABOVE LISTED "FOR CELL FRAME (FOR IDLE CELL)"		
IDLE CELL (WHEN MRI NON-MATCHING FOR CELL FRAME)	——		1+0+ ALL 1	MATCHING	EFMT*1	ALL 1	ALL 1
IDLE CELL (WHEN MRI NON-MATCHING FOR CELL FRAME)	——		1+0+ ALL 1	NON-MATCHING	——	——	——
FOR EACH CELL FRAME +) BOM	——		——		——	VCI+MID	0+1+TO TIME
FOR EACH CELL FRAME +) COM	VCI+MID	MATCHING	——		——	——	——
FOR EACH CELL FRAME +) COM	VCI+MID	NON-MATCHING	——		E1RM	——	——
FOR EACH CELL FRAME +) EOM	VCI+MID	MATCHING	——		——	ALL 1	ALL 1
FOR EACH CELL FRAME +) EOM	VCI+MID	NON-MATCHING	——		E1RM	——	——
SSM	D.C.						

*1 : EOM (TIME OUT) CELL GENERATION

FIG. 252

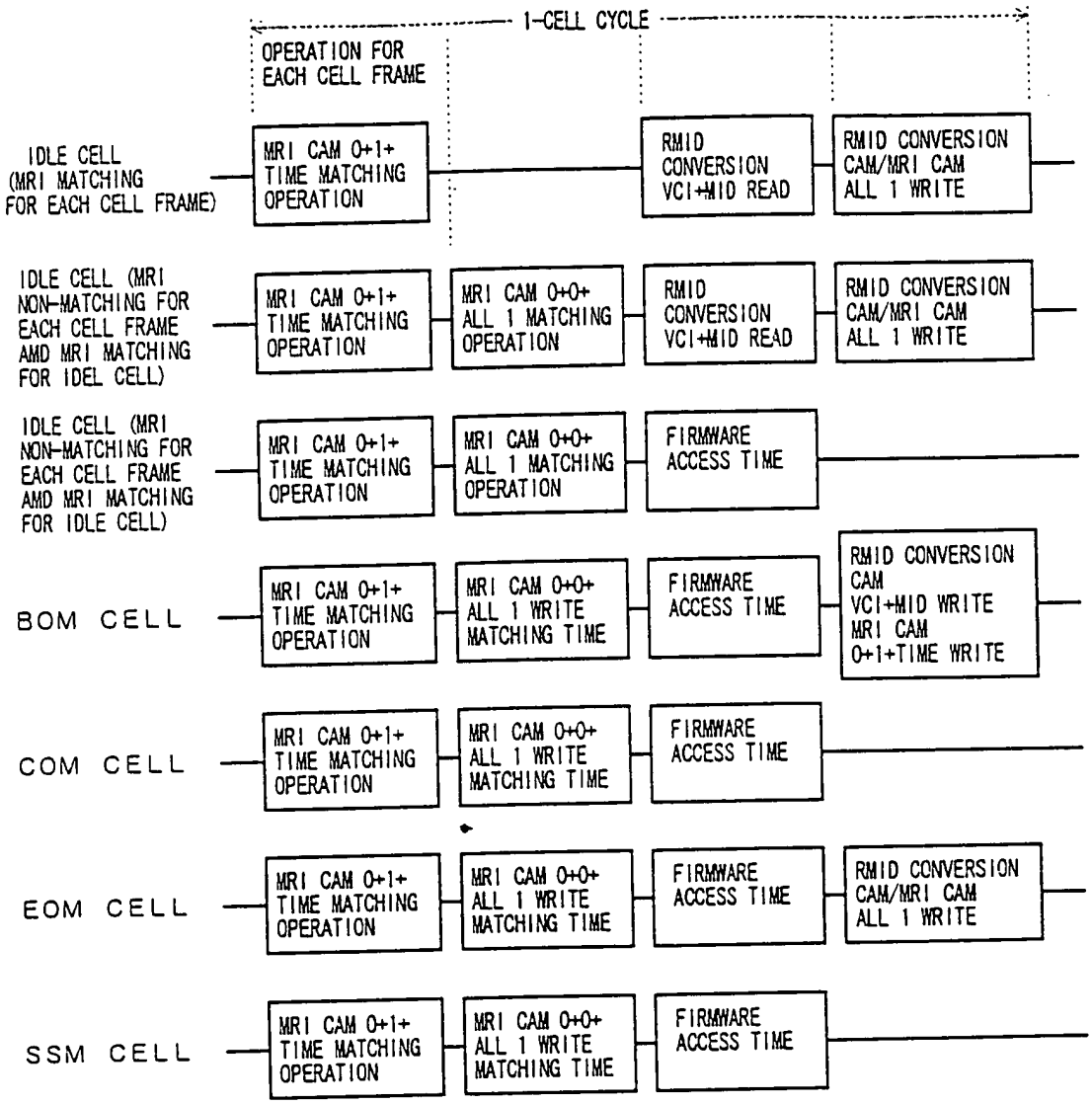

1-CELL CYCLE
OPERATION FOR EACH CELL FRAME
IDLE CELL (MRI MATCHING FOR EACH CELL FRAME)
MRI CAM 0+1+ TIME MATCHING OPERATION
RMID CONVERSION VCI+MID READ
RMID CONVERSION CAM/MRI CAM ALL 1 WRITE
IDLE CELL (MRI NON-MATCHING FOR EACH CELL FRAME AMD MRI MATCHING FOR IDEL CELL)
MRI CAM 0+1+ TIME MATCHING OPERATION
MRI CAM 0+0+ ALL 1 MATCHING OPERATION
RMID CONVERSION VCI+MID READ
RMID CONVERSION CAM/MRI CAM ALL 1 WRITE
IDLE CELL (MRI NON-MATCHING FOR EACH CELL FRAME AMD MRI MATCHING FOR IDLE CELL)
MRI CAM 0+1+ TIME MATCHING OPERATION
MRI CAM 0+0+ ALL 1 MATCHING OPERATION
FIRMWARE ACCESS TIME
BOM CELL
MRI CAM 0+1+ TIME MATCHING OPERATION
MRI CAM 0+0+ ALL 1 WRITE MATCHING TIME
FIRMWARE ACCESS TIME
RMID CONVERSION CAM VCI+MID WRITE MRI CAM 0+1+TIME WRITE
COM CELL
MRI CAM 0+1+ TIME MATCHING OPERATION
MRI CAM 0+0+ ALL 1 WRITE MATCHING TIME
FIRMWARE ACCESS TIME
EOM CELL
MRI CAM 0+1+ TIME MATCHING OPERATION
MRI CAM 0+0+ ALL 1 WRITE MATCHING TIME
FIRMWARE ACCESS TIME
RMID CONVERSION CAM/MRI CAM ALL 1 WRITE
SSM CELL
MRI CAM 0+1+ TIME MATCHING OPERATION
MRI CAM 0+0+ ALL 1 WRITE MATCHING TIME
FIRMWARE ACCESS TIME

FIG. 253

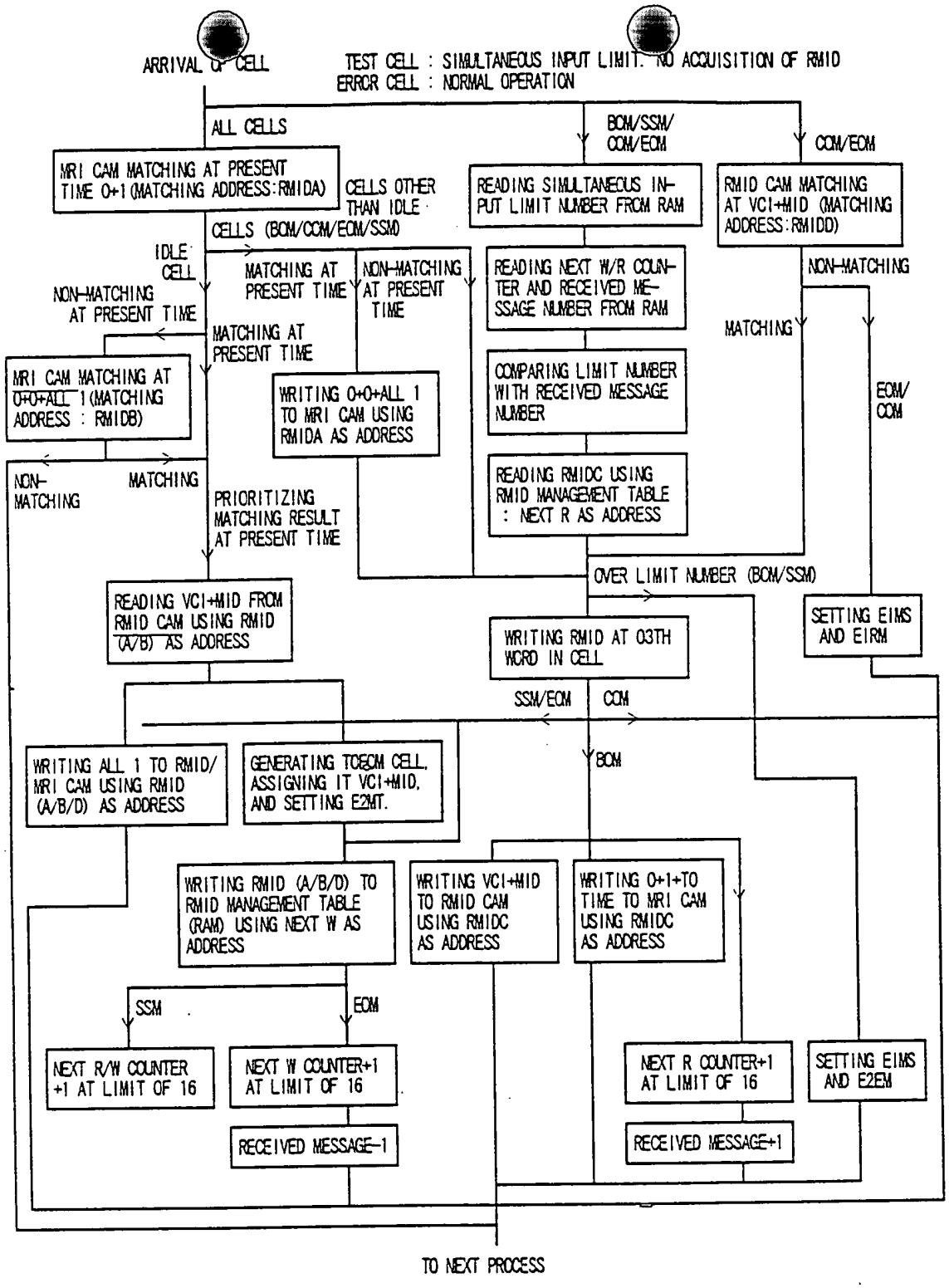

ARRIVAL OF CELL
TEST CELL : SIMULTANEOUS INPUT LIMIT: NO ACQUISITION OF RMID
ERROR CELL : NORMAL OPERATION
ALL CELLS
BOM/SSM/ COM/EOM
COM/EOM
MRI CAM MATCHING AT PRESENT TIME 0+1 (MATCHING ADDRESS:RMIDA)
CELLS OTHER THAN IDLE
READING SIMULTANEOUS INPUT LIMIT NUMBER FROM RAM
RMID CAM MATCHING AT VCI+MID (MATCHING ADDRESS:RMIDD)
CELLS (BOM/COM/EOM/SSM)
IDLE CELL
MATCHING AT PRESENT TIME
NON-MATCHING AT PRESENT TIME
READING NEXT W/R COUNTER AND RECEIVED MESSAGE NUMBER FROM RAM
NON-MATCHING
NON-MATCHING AT PRESENT TIME
MATCHING AT PRESENT TIME
MATCHING
MRI CAM MATCHING AT 0+0+ALL 1 (MATCHING ADDRESS : RMIDB)
WRITING 0+0+ALL 1 TO MRI CAM USING RMIDA AS ADDRESS
COMPARING LIMIT NUMBER WITH RECEIVED MESSAGE NUMBER
EOM/ COM
NON-MATCHING
MATCHING
READING RMIDC USING RMID MANAGEMENT TABLE : NEXT R AS ADDRESS
PRIORITIZING MATCHING RESULT AT PRESENT TIME
OVER LIMIT NUMBER (BOM/SSM)
READING VCI+MID FROM RMID CAM USING RMID (A/B) AS ADDRESS
WRITING RMID AT 03TH WORD IN CELL
SETTING EIMS AND EIRM
SSM/EOM
COM
WRITING ALL 1 TO RMID/ MRI CAM USING RMID (A/B/D) AS ADDRESS
GENERATING TOEOM CELL, ASSIGNING IT VCI+MID, AND SETTING E2MT.
BOM
WRITING RMID (A/B/D) TO RMID MANAGEMENT TABLE (RAM) USING NEXT W AS ADDRESS
WRITING VCI+MID TO RMID CAM USING RMIDC AS ADDRESS
WRITING 0+1+TO TIME TO MRI CAM USING RMIDC AS ADDRESS
SSM
EOM
NEXT R/W COUNTER +1 AT LIMIT OF 16
NEXT W COUNTER+1 AT LIMIT OF 16
NEXT R COUNTER+1 AT LIMIT OF 16
SETTING EIMS AND E2EM
RECEIVED MESSAGE-1
RECEIVED MESSAGE+1
TO NEXT PROCESS

FIG. 254

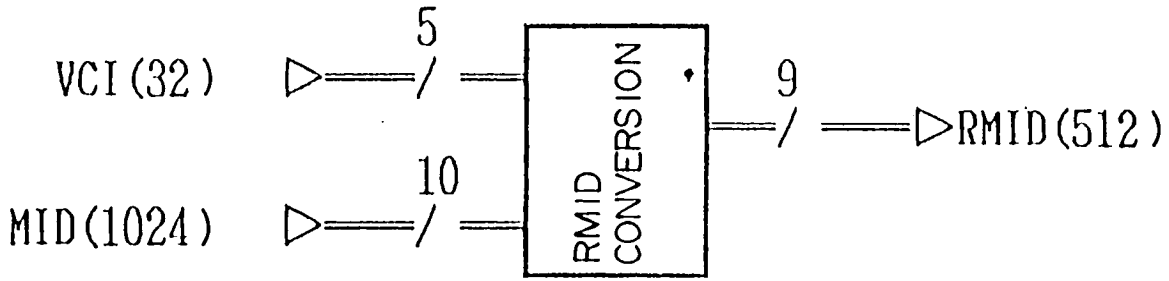


FIG. 255

TABLE RMID RMID ACQUISITION UNIT, SIMULTANEOUS INPUT LIMIT, MRI T.Q. SET/RELEASE PROCESS

INPUT			RMID ACQUISITION CHECK	SIMULTANEOUS INPUT LIMIT CHECK	OUTPUT			RMID	MRI T.Q.	RECEIVED CELL NUMBER	READ POINTER	WRITE POINTER	REMARKS
CELL	MS	RM			MS	RM	EM						
SSM	×	×	ACQUIRED	——	×	×	×	IMPOSSIBLE	——	——	——	——	RELEASING RMID
			NOT-ACQUIRED	OK	×	×	×	NEW RMID	——	——	+1	+1	
				NG	○	○	○	ALL 1	——	——	——	——	
	○	×	ACQUIRED	——	○	×	×	IMPOSSIBLE	——	——	——	——	
			NOT-ACQUIRED	——		○	×	ALL 1	——	——	——	——	
	○	○	——	——	○	○	×	ALL 1	——	——	——	——	
BOM	×	×	ACQUIRED	——	×	×	×	ACQUIRED RMID	RESETTING	——	——	——	
			NOT-ACQUIRED	OK	×	×	×	NEW RMID	SETTING	+1	+1	——	
				NG	○	○	○	ALL 1	——	——	——	——	
	○	×	ACQUIRED	——	○	×	×	ACQUIRED RMID	CLEAR	−1	——	+1	RELEASING RMID
			NOT-ACQUIRED	——		○	×	ALL 1	——	——	——	——	
	○	○	——	——	○	○	×	ALL 1	——	——	——	——	
COM	×	×	ACQUIRED	——	×	×	×	ACQUIRED RMID	——	——	——	——	
			NOT-ACQUIRED	——	○	○	×	ALL 1	——	——	——	——	
	○	×	ACQUIRED	——	○	×	×	ACQUIRED RMID	CLEAR	−1	——	+1	RELEASING RMID
			NOT-ACQUIRED	——		○	×	ALL 1	——	——	——	——	
	○	○	——	——	○	○	×	ALL 1	——	——	——	——	
EOM	×	×	ACQUIRED	——	×	×	×	ACQUIRED RMID	CLEAR	−1	——	+1	RELEASING RMID
			NOT-ACQUIRED	——	○	○	×	ALL 1	——	——	——	——	
	○	×	ACQUIRED	——	○	×	×	ACQUIRED RMID	CLEAR	−1	——	+1	RELEASING RMID
			NOT-ACQUIRED	——		○	×	ALL 1	——	——	——	——	
	○	○	——	——	○	○	×	ALL 1	——	——	——	——	
T.Q.	—	—	ACQUIRED	——	○	×	×	ACQUIRED RMID	CLEAR	−1	——	+1	RELEASING RMID
PVC	—	—	——	——	×	×	×	INPUT MID	——	——	——	——	NO ACTION

○ : ERROR ON, × : ERROR OFF, —— : NO OBJECT OF PROCESS

FIG. 256

ST		NORMAL VALUE OF HEADER EXTENTION					
		FIRST ELEMENT			SECOND ELEMENT		
		FIRST OCTET	SECOND OCTET	THIRD OCTET	FOURTH OCTET	FIFTH OCTET	SIXTH OCTET
BOM SSM	CONDITION 1	3	0	1	4, 6, OR 8	1	D. C.
	CONDITION 2	3	0	1	D. C.	VALUE OTHER THAN 1	D. C.

FIG. 257

INPUT			OUTPUT
ST	SA CHECK	MATCHING ADDRESS *1	EFSA
BOM, SSM	No	D.C.	ON
COM, EOM	Match	≠SNI#	ON
COM, EOM	Match	=SNI#	OFF
COM, EOM	D.C.	D.C.	OFF

*1 : MATCHING ADDRESS MSB 4 bit

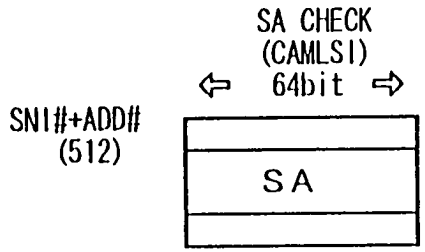


FIG. 258

SC ATTRIBUTE	MATCHING AT CAM	NON-MATCHING AT CAM
1	ERROR(NOT RECEIVABLE AT ENTERED ADDRESS)	SENDING EANBLED
0	SENDING ENABLED	ERROR(NOT RECEIVABLE AT ADDRESS OTHER THAN ENTERED ADDRESS)

- COM AND EOM ARE NOT OBJECT OF PROCESS.
- CELL WHOSE TEST BIT OF 02TH WORD INDICATES 1 (INTER-MESH PVC TEST CELL) IS NOT OBJECT OF PROCESS.

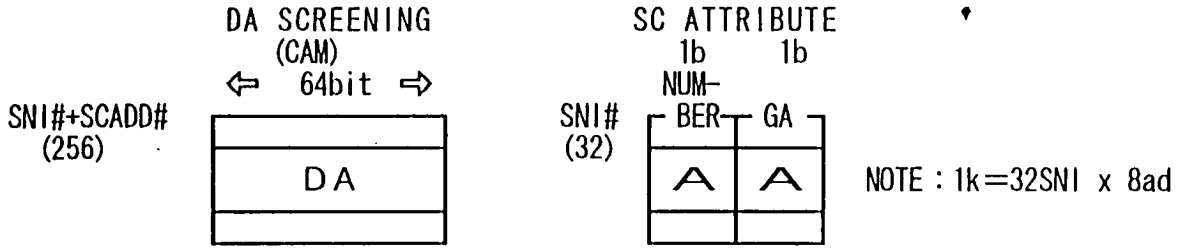


FIG. 259

INPUT				OUTPUT	
ST(SIP)	BEtag (H)	BEtag CHECK	BEtag (T)	EFBE	BEtag CHECK
BOM	BEtag H	D.C.	D.C.	OFF	BE tag H
COM	D.C.	D.C.	D.C.	OFF	———
EOM	D.C.	BEtag	= BEtag	OFF	D.C.
EOM	D.C.	BEtag	≠ BEtag	ON	D.C.
SSM	BEtag H	D.C.	= BEtagH	OFF	D.C.
SSM	BEtag H	D.C.	≠ BEtagH	ON	D.C.

H : Header
T : Trailer

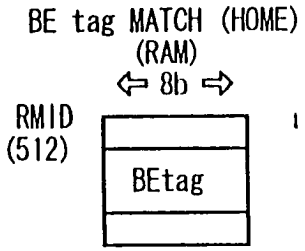


FIG. 260

INPUT				OUTPUT	
ST (SIP)	BASIZE	BASIZE CHECK	LENGTH	EFBE	BASIZE CHECK
BOM	BASIZE	D. C.	D. C.	OFF	BASIZE
COM	D. C.	D. C.	D. C.	OFF	———
EOM	D. C.	BASIZE	= LENGTH	OFF	D. C.
EOM	D. C.	BASIZE	≠ LENGTH	ON	D. C.
SSM	BASIZE	D. C.	= LENGTH	OFF	D. C.
SSM	BASIZE	D. C.	≠ LENGTH	ON	D. C.

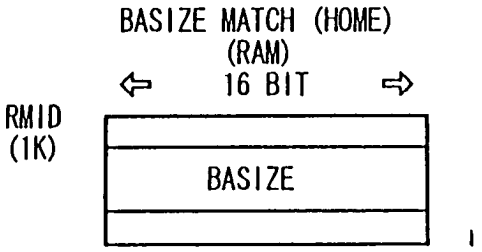


FIG. 261

INPUT						OUTPUT (2)		
ST	BASIZE	PAD LENGTH	CELL COUNT	PL LENGTH	INFORMATION LENGTH PL LENGTH OF EOM	CELL COUNT	EFIL	INFORMATION LENGTH
BOM	BASIZE	PAD	D.C.	D.C.	D.C.	INITIAL VALUE	OFF	PL LENGTH OF EOM
COM	D.C.	D.C.	≠0	D.C.	D.C.	DOWN	OFF	——
COM	D.C.	D.C.	=0	D.C.	D.C.	D.C.	ON	——
EOM	D.C.	D.C.	≠0	D.C.	D.C.	D.C.	ON	——
EOM	D.C.	D.C.	=0	PL	≠PL	D.C.	ON	D.C.
EOM	D.C.	D.C.	=0	PL	=PL	D.C.	OFF	D.C.
SSM	BASIZE	PAD	D.C.	PL	≠PL	D.C.	ON	D.C.
SSM	BASIZE	PAD	D.C.	PL	=PL	D.C.	OFF	D.C.

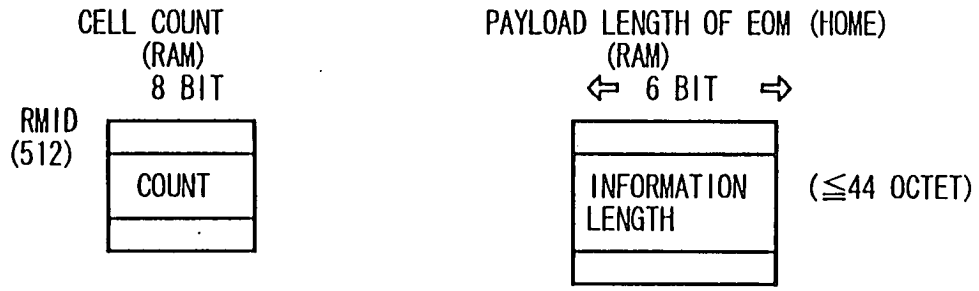


FIG. 262

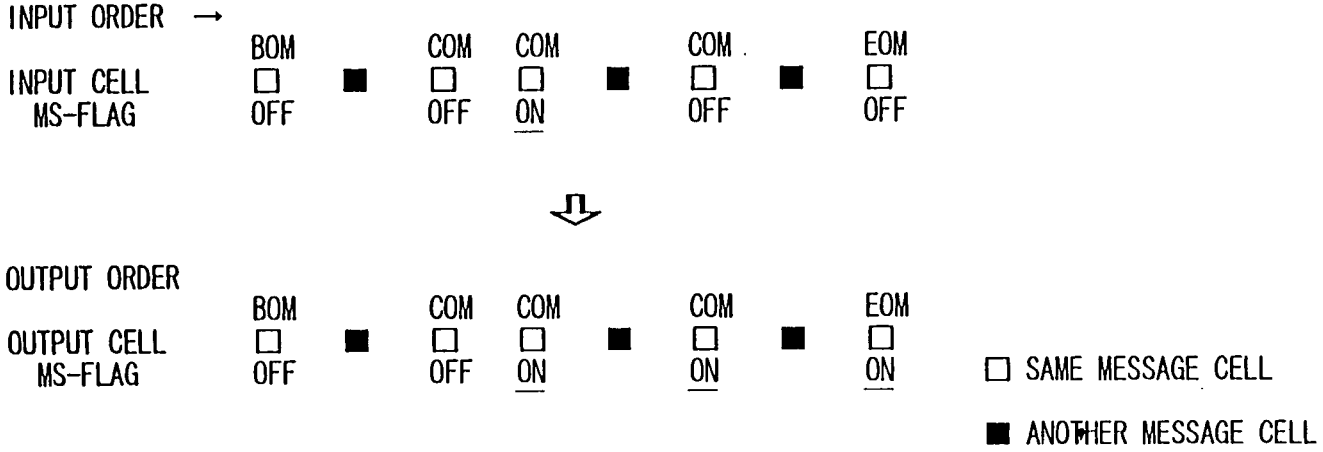

INPUT ORDER →
BOM
COM
COM
COM
EOM
INPUT CELL
MS-FLAG
OFF
OFF
ON
OFF
OFF
OUTPUT ORDER
BOM
COM
COM
COM
EOM
OUTPUT CELL
MS-FLAG
OFF
OFF
ON
ON
ON
SAME MESSAGE CELL
ANOTHER MESSAGE CELL

FIG. 263

- COM : MS-FLAG IS SET ON AND SUBSEQUENT CELLS ARE PROCESSED AS ERROR CELLS
- EOM : DISCARDED AS INVALID CELL. SIGNAL IS OUTPUT TO COUNT DISCARDED CELLS.

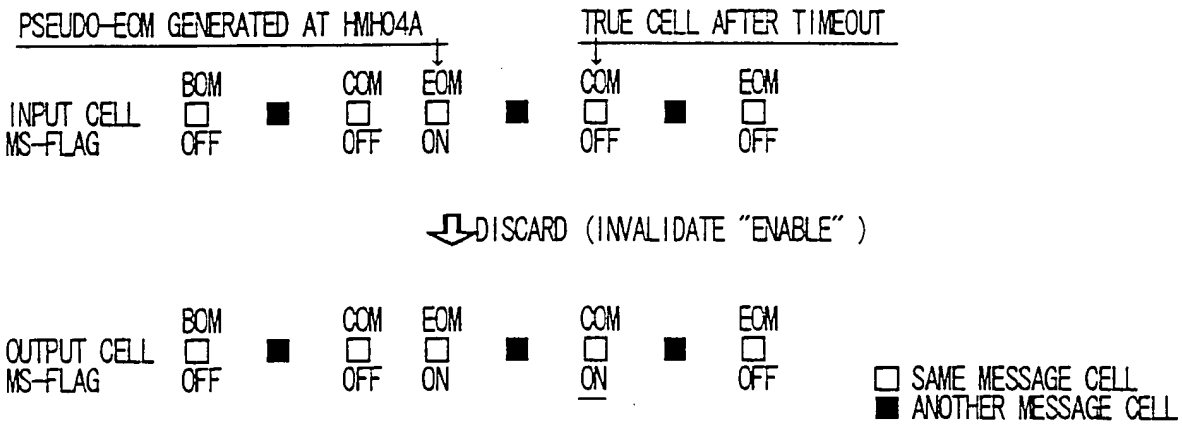
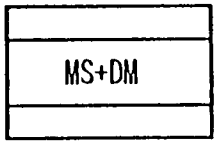


FIG. 264

○ PROCESS FOR ERRONEOUS MEMORY
ERROR (HOME)
2bit (RAM)

TRIAL BIT+VCI+MID
(32k)



MS(Mster) : 1 IF MASTER ERROR FLAG OF CELL IS SET

DM(Discard Message) : IDENTIFIER INDICATING WHETHER OR NOT EOM HAS ARRIVED (1 AT ARRIVA)

・ERROR MEMORY MATRIX

ITEM	INPUT CELL	read data		write data		OUTPUT CELL PROCESS
	ST	MS	DM	MS	DM	
①	BOM (NORMAL CELL)	D.C.	D.C.	0	0	NO (INPUT THROUGH)
②	BOM (ERROR CELL)	D.C.	D.C.	1	0	NO (INPUT THROUGH)
③	COM (NORMAL CELL)	0	0	0	0	NO (INPUT THROUGH)
④	COM (NORMAL CELL)	1	0	1	0	SETTING MASTER ERROR FLAG
⑤	COM (NORMAL CELL)	D.C.	1	1	1	SETTING MASTER ERROR FLAG
⑥	COM (ERROR CELL)	D.C.	0	1	0	NO (INPUT THROUGH)
⑦	COM (ERROR CELL)	D.C.	1	1	1	NO (INPUT THROUGH)
⑧	EOM	0	0	0	1	NO (INPUT THROUGH)
⑨	EOM	1	0	1	1	SETTING MASTER ERROR FLAG
⑩	EOM	D.C.	1	D.C.	11	INVALID CELL

FIG. 265

INPUT		ISSI ASSIGNING HEADER	OUTPUT(CELL DATA, ETC.)					
ST			IST	STC	SN	MID	PL	CRC
BOM	GENERATING BOM	ASSIGNING HEADER	——	BOM	COPY	COPY	COPY	COPY
	ARRIVAL OF BOM	D.C.	BOM	COM	——	——	——	——
COM		D.C.	COM	COM	——	——	——	——
EOM		D.C.	EON	EOM	——	——	——	——
SSM	GENERATING BOM	ASSIGNING HEADER	——	BOM	COPY	COPY	COPY	COPY
	ARRIVAL OF SSM	D.C.	SSM	EOM	——	——	——	——

FIG. 266

○ ISSI HEADER TO BE ASSIGNED TO INTER-MH INF BOM

NAME	INFORMATION LENGTH	LEVEL	ACTION	PROCESS POSITION
RV(RESERVE)	1 cot	L2	D.C (COPY ARRIVING BOM)	(22) ENCAPSULATION
BEtag	1 cot	L2	D.C (COPY ARRIVING BOM)	(22) ENCAPSULATION
BAsize	2 cot	L2	D.C (COPY ARRIVING BOM)	(22) ENCAPSULATION
DA(Destination Address)	8 cot	L3	D.C. (COPY ARRIVING BOM)	(22) ENCAPSULATION
SA(Source Address)	8 cot	L3	D.C. (COPY ARRIVING BOM)	(22) ENCAPSULATION
D.C	17 cot	L3	D.C. (COPY ARRIVING BOM)	(22) ENCAPSULATION
IIT	1 cot	L3	SETTING 01_H	(23) CARRIER SELECTION
ES(Explicit Selection)	1 cot	L3	SETTING 0 OR 1	(23) CARRIER SELECTION
Rv(reserve)	7 cot	L3	SETTING ALL 0	(23) CARRIER SELECTION
C(Carrier)	2 cot	L3	ASSIGNING CARRIER INFORMATION	(23) CARRIER SELECTION
INID	2 cot	L3	SETTING ALL 0	(23) CARRIER SELECTION
IITPS	2 cot	L3	SETTING ALL 0	(23) CARRIER SELECTION

FIG. 267

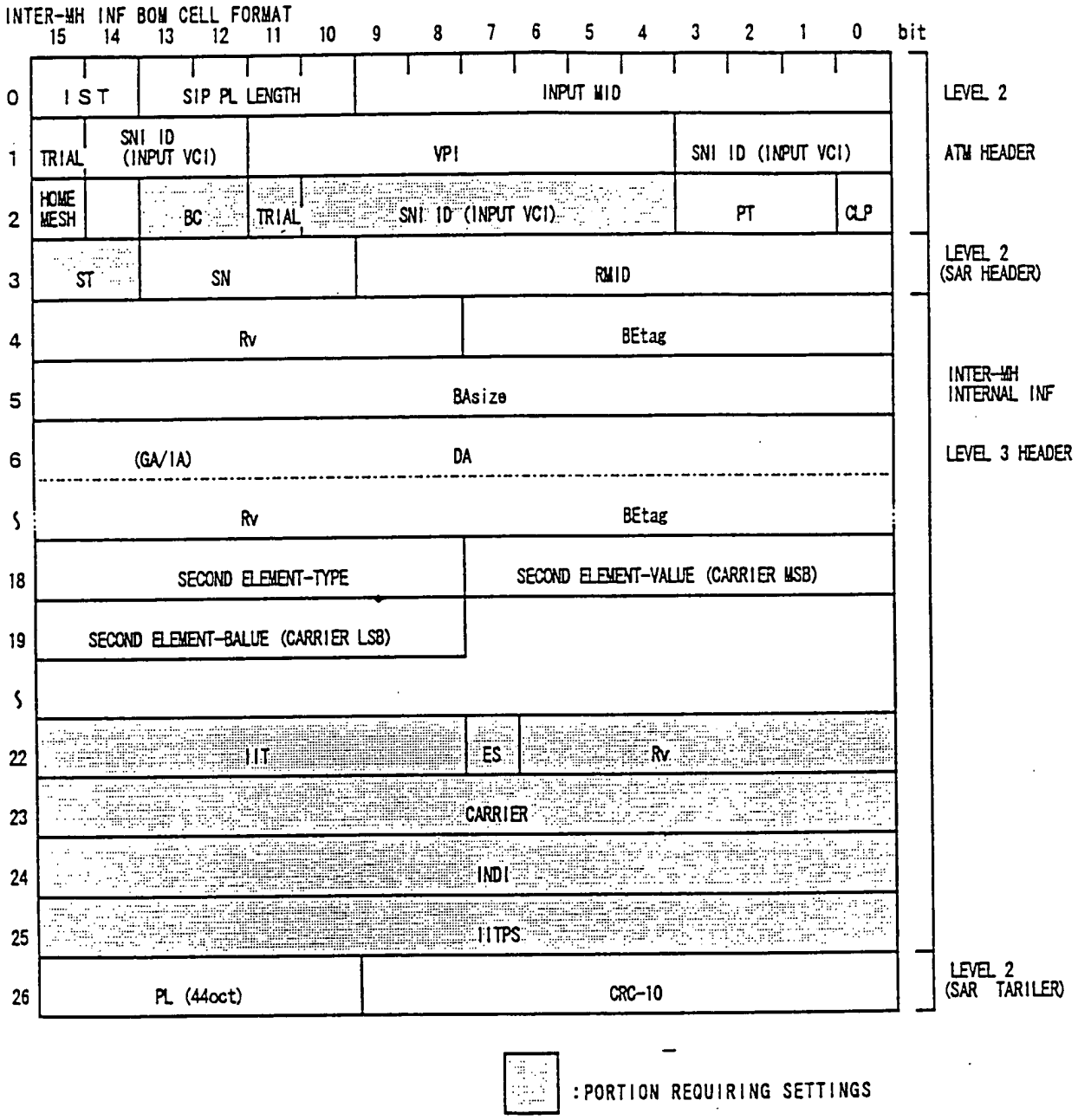

INTER-MH INF BOM CELL FORMAT
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 bit
0
1
2
3
4
5
6
S
18
19
S
22
23
24
25
26
I S T
SIP PL LENGTH
INPUT MID
TRIAL
SNI ID (INPUT VCI)
VPI
SNI ID (INPUT VCI)
HOME MESH
BC
TRIAL
SNI ID (INPUT VCI)
PT
CLP
ST
SN
RMID
Rv
BEtag
BAsize
(GA/IA)
DA
Rv
BEtag
SECOND ELEMENT-TYPE
SECOND ELEMENT-VALUE (CARRIER MSB)
SECOND ELEMENT-BALUE (CARRIER LSB)
IIT
ES
Rv
CARRIER
INDI
IITPS
PL (44oct)
CRC-10
LEVEL 2
ATM HEADER
LEVEL 2
(SAR HEADER)
INTER-MH
INTERNAL INF
LEVEL 3 HEADER
LEVEL 2
(SAR TARILER)
:PORTION REQUIRING SETTINGS

FIG. 268

6,068,539 5/2000 Haba

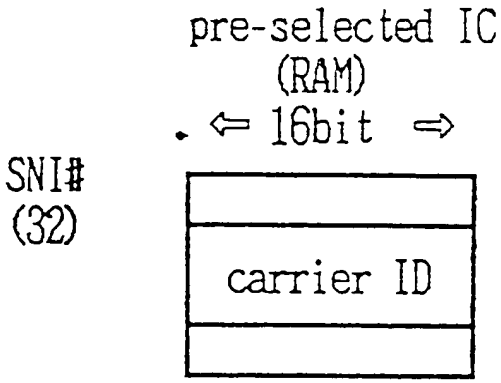


FIG. 269

AT INDICATES GA	CAM MATCHING			DETERMI-NATION	ACTION	BC (BROADCAST IDENTIFIER)		ISSI CARRIER AREA
	INTRA-STATION TABLE	INTRA-STATION NUMBER TABLE	EXTERNAL NUMBER TABLE			MSB	LSB	
○	D.C.	D.C.	D.C.	GA	BROADCAST TO ALL MH	1	1	ASSIGNING CARRIER
×	MATCHING	D.C.	D.C.	INTRA-STATION	ASSIGNING SBMH SPECIFIED VCI	0	0	CLEARING CARRIER
×	NON-MATCHING	MATCHING	NON-MATCHING	INTRA-STATION	BROADCAST TO ALL SBMH	0	1	CLEARING CARRIER
×	NON-MATCHING	NON-MATCHING	MATCHING	EXTERNAL	ASSIGNING GWMH SPECIFIED VCI	0	0	CLEARING CARRIER
×	NON-MATCHING	NON-MATCHING	NON-MATCHING	DETERMINATION IMPOSSIBLE	BROADCAST TO ALL GWMH	1	0	ASSIGNING CARRIER

FIG. 270

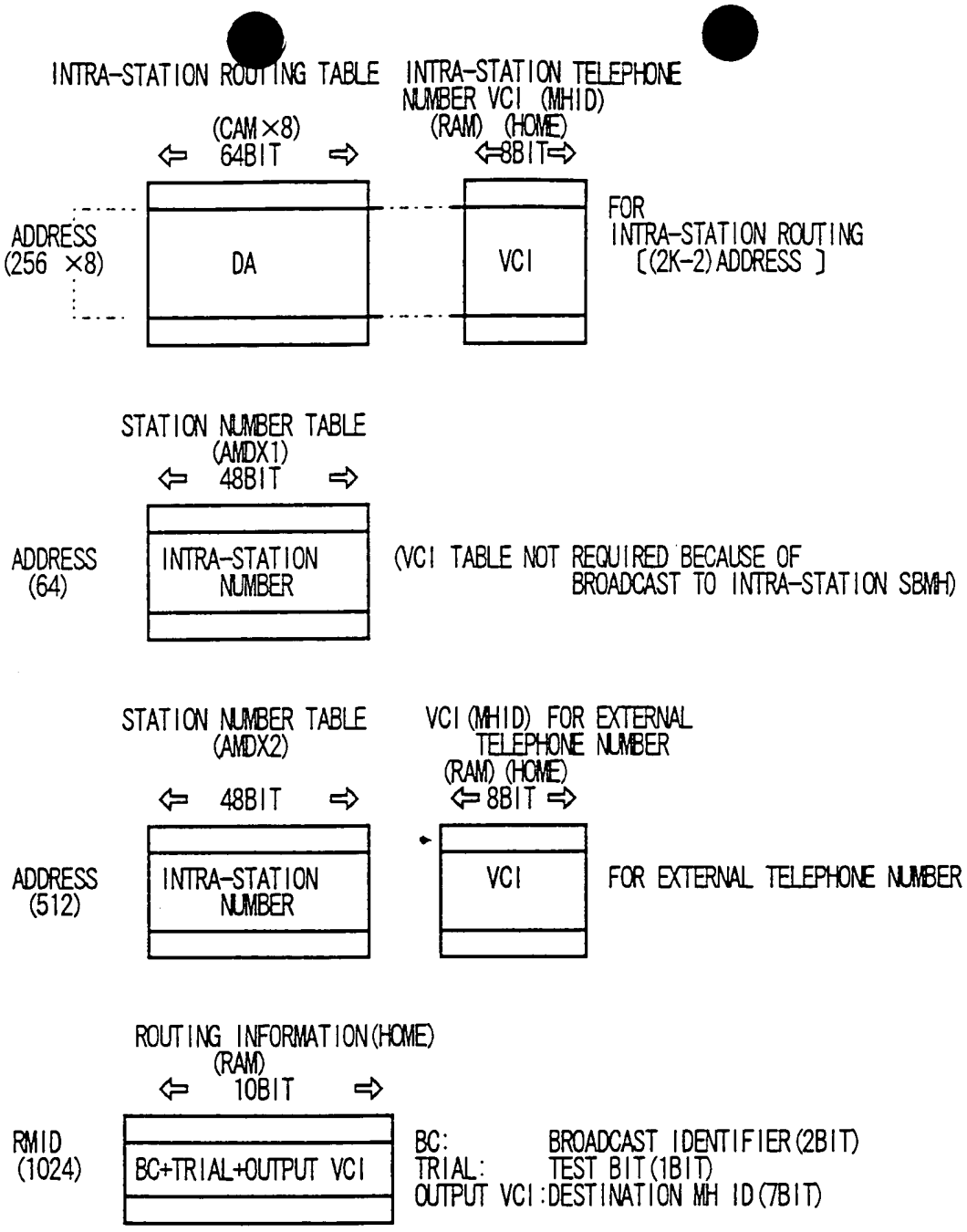
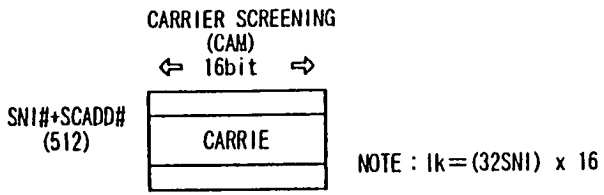


FIG. 271

5,526,362



NOTE : 1k=(32SNI) x 16

CARRIER AREA STATE

ROUTING METHOD	CARRIER AREA	REMARKS
BROADCAST TO ALL MH	ASSIGNING CARRIER	CELL NOT USING ICI REQUIRES MASKING IN GWMH
ASSIGNING SBMH SPECIFIED VCI	CLEARING CARRIER	MASKING CARRIER AREA WITH "INTRA-STATION" DETERMINED
BROADCAST TO ALL SBMH	CLEARING CARRIER	MASKING CARRIER AREA WITH "INTRA-STATION" DETERMINED
ASSIGNING GWMH SPECIFIED VCI	CLEARING CARRIER	MASKING CARRIER AREA WITH "LATA" DETERMINED
BROADCAST TO GWMH	ASSIGNING CARRIER	CELL NOT USING ICI REQUIRES MASKING IN GWMH

FIG. 272

SPECIFYING BROADCAST

BC(2BIT)	TRANSFERRED TO:
(11)	TRANSFER TO ALL MH (DETERMINED AS GA)
(00)	DETERMINING DESTINATION MH (BROADCAST NOT REQUIRED)
(01)	TRANSFER TO ALL SBMH (DESTINATION IN HOME STATION)
(10)	TRANSFER TO ALL GWMH (DESTINATION IN MATE STATION)

FIG. 273

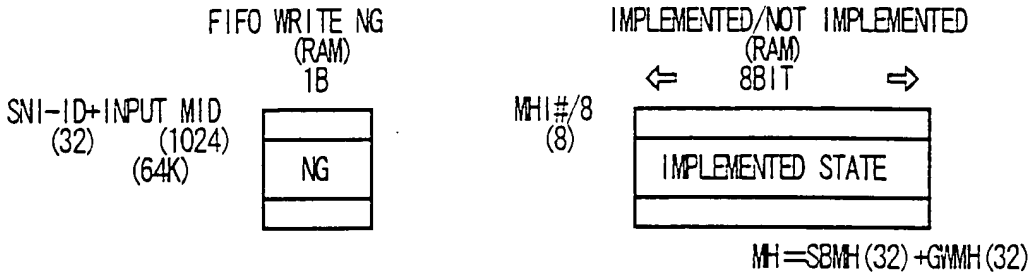


FIG. 274

6,839,348 Jan. 4, 2005

6692E0 EP2726A1

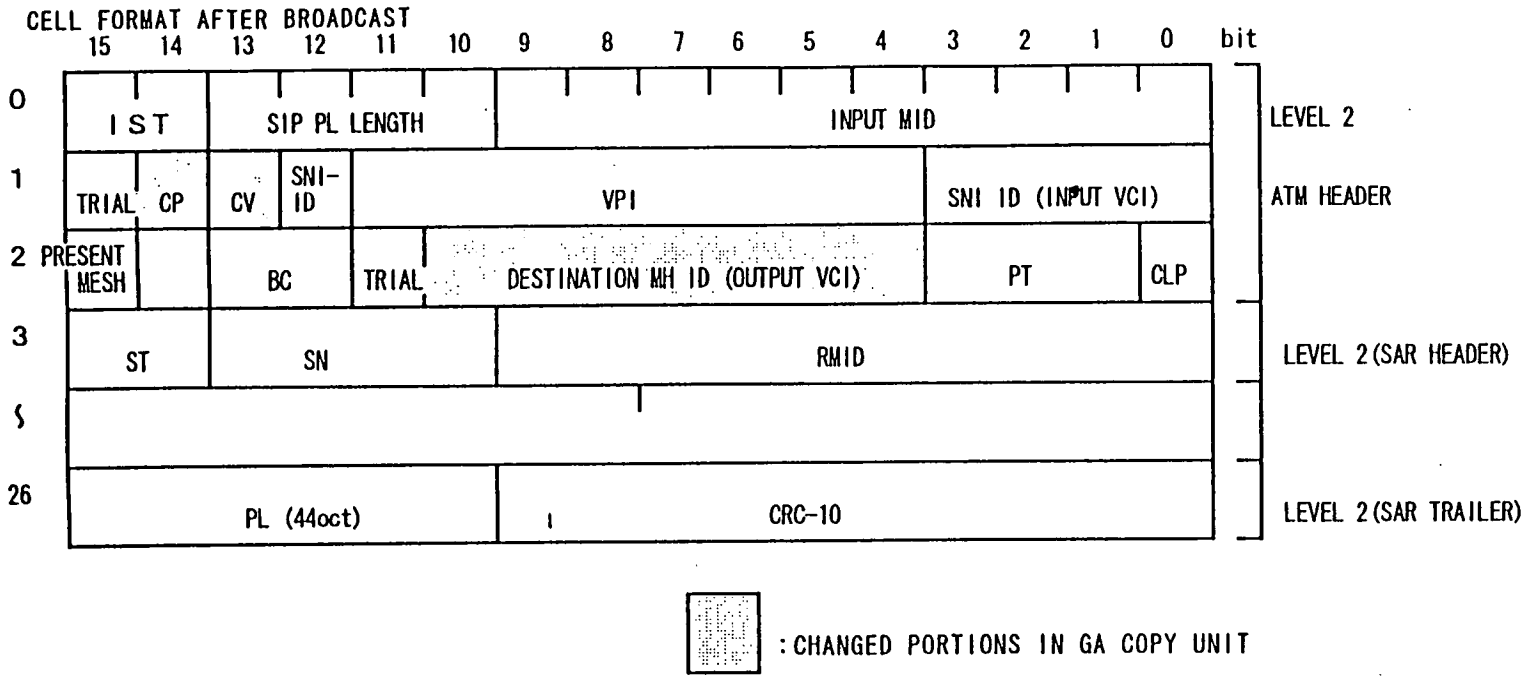


FIG. 275

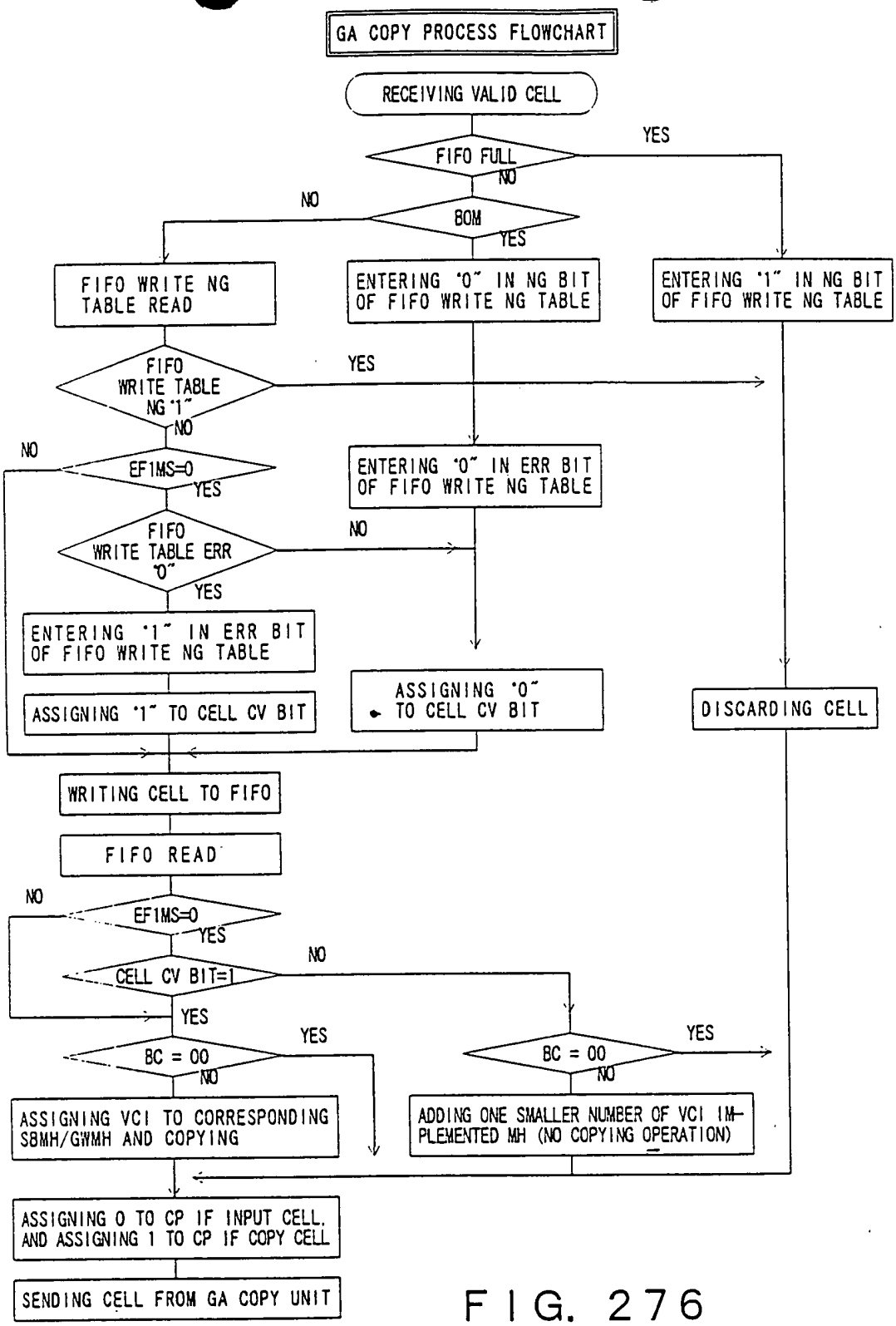

GA COPY PROCESS FLOWCHART
RECEIVING VALID CELL
FIFO FULL
YES
NO
BOM
NO
YES
FIFO WRITE NG TABLE READ
ENTERING "0" IN NG BIT OF FIFO WRITE NG TABLE
ENTERING "1" IN NG BIT OF FIFO WRITE NG TABLE
FIFO WRITE TABLE NG "1"
YES
NO
NO
EF1MS=0
YES
ENTERING "0" IN ERR BIT OF FIFO WRITE NG TABLE
FIFO WRITE TABLE ERR "0"
NO
YES
ENTERING "1" IN ERR BIT OF FIFO WRITE NG TABLE
ASSIGNING "1" TO CELL CV BIT
ASSIGNING "0" TO CELL CV BIT
DISCARDING CELL
WRITING CELL TO FIFO
FIFO READ
NO
EF1MS=0
YES
NO
CELL CV BIT=1
YES
YES
BC = 00
NO
YES
BC = 00
NO
ASSIGNING VCI TO CORRESPONDING SBMH/GWMH AND COPYING
ADDING ONE SMALLER NUMBER OF VCI IMPLEMENTED MH (NO COPYING OPERATION)
ASSIGNING 0 TO CP IF INPUT CELL, AND ASSIGNING 1 TO CP IF COPY CELL
SENDING CELL FROM GA COPY UNIT

FIG. 276

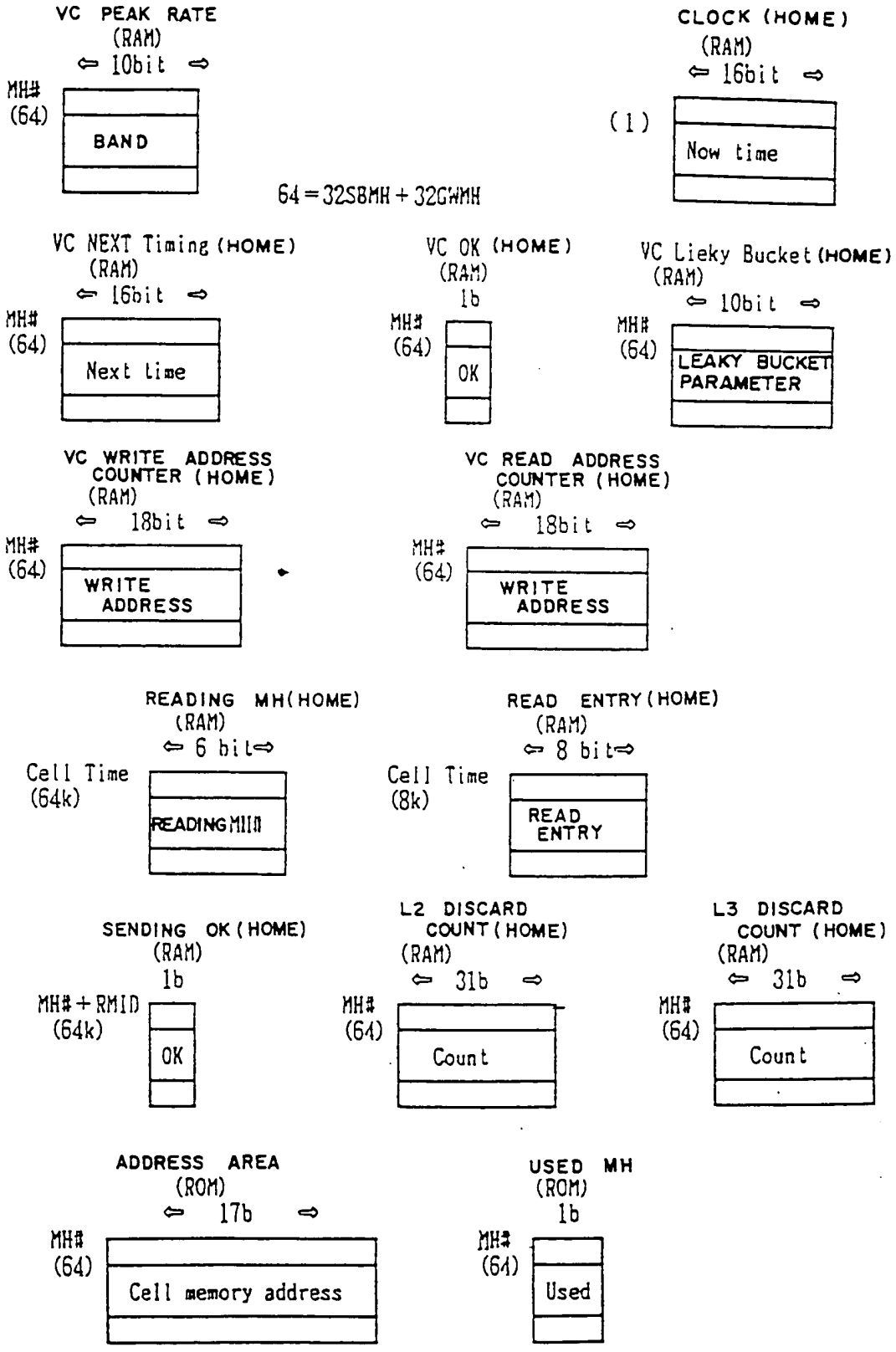

VC PEAK RATE
(RAM)
⇦ 10bit ⇨
MH#
(64)
BAND
64 = 32SBMH + 32GWMH
CLOCK (HOME)
(RAM)
⇦ 16bit ⇨
(1)
Now time
VC NEXT Timing (HOME)
(RAM)
⇦ 16bit ⇨
MH#
(64)
Next time
VC OK (HOME)
(RAM)
1b
MH#
(64)
OK
VC Lieky Bucket (HOME)
(RAM)
⇦ 10bit ⇨
MH#
(64)
LEAKY BUCKET
PARAMETER
VC WRITE ADDRESS
COUNTER (HOME)
(RAM)
⇦ 18bit ⇨
MH#
(64)
WRITE
ADDRESS
VC READ ADDRESS
COUNTER (HOME)
(RAM)
⇦ 18bit ⇨
MH#
(64)
WRITE
ADDRESS
READING MH(HOME)
(RAM)
⇦ 6 bit⇨
Cell Time
(64k)
READING MH
READ ENTRY(HOME)
(RAM)
⇦ 8 bit⇨
Cell Time
(8k)
READ
ENTRY
SENDING OK(HOME)
(RAM)
1b
MH# + RMID
(64k)
OK
L2 DISCARD
COUNT(HOME)
(RAM)
⇦ 31b ⇨
MH#
(64)
Count
L3 DISCARD
COUNT (HOME)
(RAM)
⇦ 31b ⇨
MH#
(64)
Count
ADDRESS AREA
(ROM)
⇦ 17b ⇨
MH#
(64)
Cell memory address
USED MH
(ROM)
1b
MH#
(64)
Used

FIG. 277

MID MANAGEMENT TABLE (HOME)
(RAM)
⇐8 bit ⇒

MII# x 256
(16k)



16k = (32SBMII + 32GWMII) x256

MID CONVERSION (HOME)
(RAM)
⇐9 bit ⇒

RMID+MII#
(10) (6)
(64k)



FLAG : 0 WHEN MID IS NOT ACQUIRED

NEXT READ / NEXT WRITE COUNTER
(RAM)
⇐9 bit ⇒

MII# x 2
(128)



128=(32SBMII +32GWMII) × 2 (NEXT READ /NEXT WRITE COUNTER)

FIG. 278

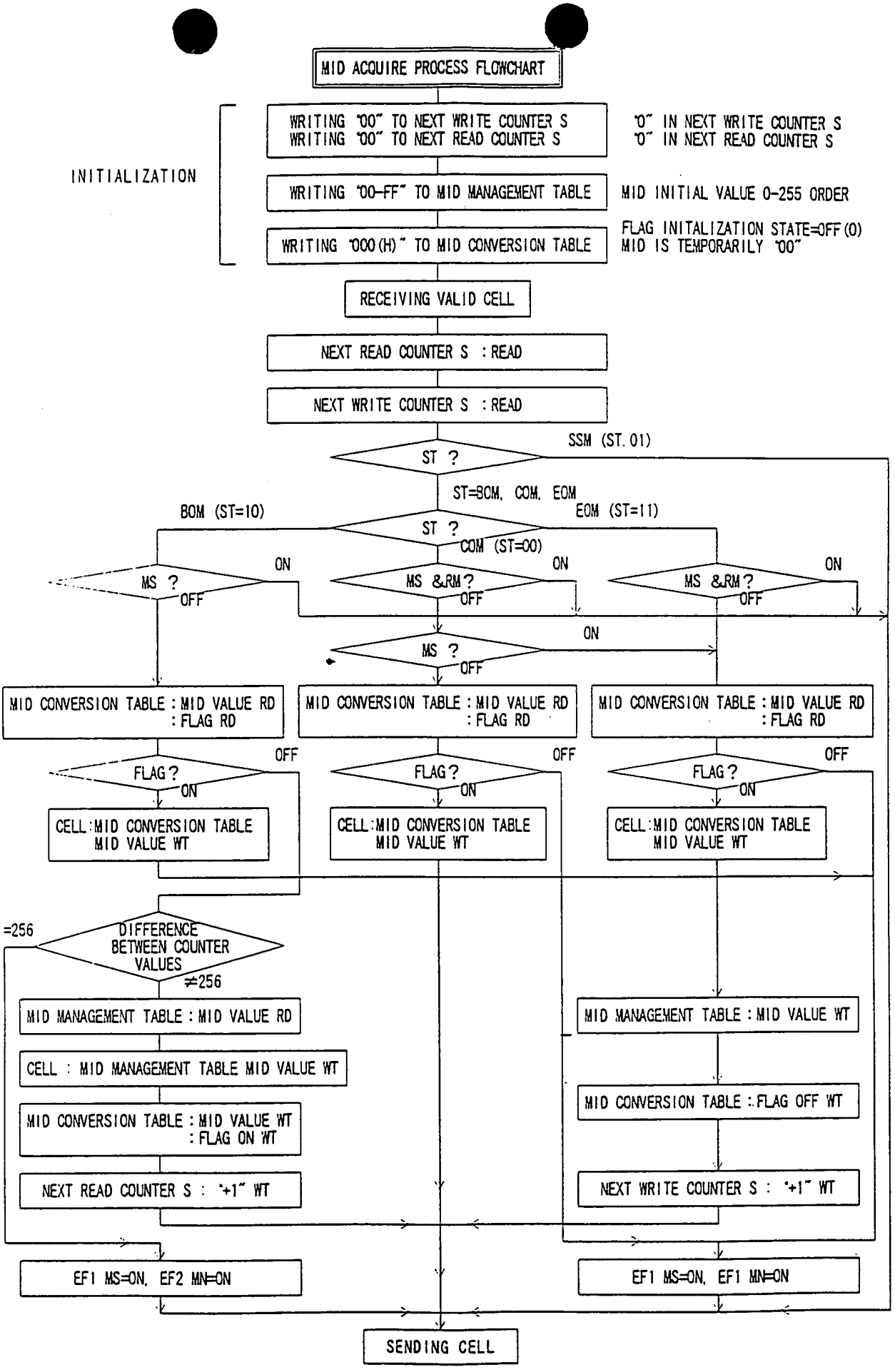

MID ACQUIRE PROCESS FLOWCHART
INITIALIZATION
WRITING "00" TO NEXT WRITE COUNTER S
WRITING "00" TO NEXT READ COUNTER S
"0" IN NEXT WRITE COUNTER S
"0" IN NEXT READ COUNTER S
WRITING "00-FF" TO MID MANAGEMENT TABLE
MID INITIAL VALUE 0-255 ORDER
WRITING "000(H)" TO MID CONVERSION TABLE
FLAG INITALIZATION STATE=OFF(0)
MID IS TEMPORARILY "00"
RECEIVING VALID CELL
NEXT READ COUNTER S : READ
NEXT WRITE COUNTER S : READ
SSM (ST. 01)
ST ?
ST=BOM, COM, EOM
BOM (ST=10)
EOM (ST=11)
COM (ST=00)
MS ?
MS &RM?
ON
OFF
MID CONVERSION TABLE : MID VALUE RD
: FLAG RD
FLAG?
CELL:MID CONVERSION TABLE
MID VALUE WT
=256
DIFFERENCE BETWEEN COUNTER VALUES
≠256
MID MANAGEMENT TABLE : MID VALUE RD
CELL : MID MANAGEMENT TABLE MID VALUE WT
MID CONVERSION TABLE : MID VALUE WT
: FLAG ON WT
NEXT READ COUNTER S : "+1" WT
MID MANAGEMENT TABLE : MID VALUE WT
MID CONVERSION TABLE : FLAG OFF WT
NEXT WRITE COUNTER S : "+1" WT
EF1 MS=ON, EF2 MN=ON
EF1 MS=ON, EF1 MN=ON
SENDING CELL

FIG. 279

SMLP TABLE (1/2)

PKG NAME	FUNCTION NAME	TABLE NAME	TYPE	HARDWARE ACCESS	SIZE(ADDRESS ×BIT WIDTH)	PKG No	ADDRESS	DATA	REMARKS
IMN03A	(9) DA CHECK S	① DA CHECK S	CAMLSI	READ	256×64	03	00000 ~ 000FF	00~63	CAM LSI× 1
	(6) MID CHECK S	① MID CHECK S	RAM	READ/WRITE	32k×1		80000 ~ 87FFF	04	MB81C84A ×2 (ODD PARITY)
	(7) SN CHECK S	① SN CHECK S	RAM	READ/WRITE	32k×4			00~03	
	(10) INGRESS FLOW CHECK S	① LEAKY BUCKET S	RAM	READ/WRITE	32×14		90000 ~ 9001F	00~13	MB81C79A ×2 (EVEN PARITY)
		② INCREMENTED OCTET NUMBER	RAM	READ	32×14		90020 ~ 9003F		
IMN04A	(15) SA CHECK S	① SA CHECK	CAMLSI	READ	256×64	04	00000 ~ 000FF	00~63	CAM LSI× 1
	(16) DA SCREENING S	① DS SCREENING	CAMLSI	READ	1k×64		00100 ~ 004FF	00~63	CAM LSI× 4
	(12) SIMULTANEOUS INPUT NUMBER CHECK S	① RMID CONVERSION S	AMDCAM	READ/WRITE	512×15		60000 ~ 601FF	00~14	AM99C10A ×2
		② MRI TIME S	AMDCAM	READ/WRITE	512×18		60200 ~ 603FF	00~17	AM99C10A ×2
		③ SIMULATNEOUS INPUT LIMIT NUMBER	RAM	READ	32×1		80000 ~ 8001F	00	MB81C79A (ODD PARITY)
		④ RMID ASSINGNING MANAGEMENT	RAM	READ/WRITE	512×13		90000 ~ 901FF	00~12	MB81C79A (ODD PARITY)
		④ RMID MANAGEMENT S	RAM	READ/WRITE	512×13		90200 ~ 903FF		
	(16) DA SCREENING S	② SC ATTRIBUTE	RAM	READ	32×2		A0000 ~ A001F	00~02	MB81C79A (EVEN PARITY)
	(18) BA SIZE MATCHING CHECK S	① BA SIZE VALUE S	RAM	READ/WRITE	512×16		B0000 ~ B01FF	00~15	MB81C79A ×2 (EVEN PARITY)
	(19) INFORMATION LENGTH CHECK S	① DOWN CNT VALUE S	RAM	READ/WRITE	512×16		B0200 ~ B03FF		
	(19) BE TAG MATCHING S	② BE TAG MATCHING S	RAM	READ/WRITE	512×16		B0400 ~ B05FF		
IMN05A	(25) ROUTING S	① INTRA-STATION ROUTING TALBE S	CAMLSI	READ	2k×64	05	00000 ~ 007FF	00~63	CAM-LSI×8
		② INTRA-STATION NUMBER TABLE S	AMDCAM	READ	64×48		60000 ~ 6003F	00~47	AM99C10A (MAX ADDRESS 256)
		③ EXTERNAL STATION NUMBER TABLE S	AMDCAM	READ	512×48		60100 ~ 602FF	00~47	AM99C10A ×2
	(26) CARRIER SCREENING S	① CARRIER SCREENING S	AMDCAM	READ	512×16		60300 ~ 604FF	00~47	AM99C10A ×2
	(22) ERROR EDITION IIS	① ERROR& DISCARD MEMORY S	RAM	READ/WRITE	64k×2		80000 ~ BFFFF	00~01	MB81C79A (EVEN PARITY)
	(24) CARRIER SELECTION S	① CARRIER SELECTION TABLE S	RAM	READ	32×16		90000 ~ 9001F	00~15	MB81C79A ×2 (EVEN PARITY)
	(25) ROUTING S	④ INTRA-STATION PHONE NUMBER VCI S	RAM	READ	2k×8		A0000 ~ A07FF	00~07	MB81C79A (EVEN PARITY)
		⑤ EXTERNAL STATION PHONE NUMBER VCI S	RAM	READ	512×8		B0000 ~ B01FF	00~07	MB81C79A (EVEN PARITY)
		⑦ RATING INFORMATION	RAM	READ/WRITE	512×10		C0000 ~ C01FF	00~09	MB81C79A (EVEN PARITY)
	(26) ENCAPSULATION S	CELL FIFO S	RAM	READ/WRITE	4k×18(FOR 128CELL)	MNG NO FIRMWARE ACCESS			AM7204A×2(PARITY ODD, EVEN MIXED)
		COPY MEMORY S	RAM	READ/WRITE	8k×18(FOR 1 CELL)				MB81C79A ×2(USED IN COMBINATION WITH PARITY OF CELL FIFO S)

FIG. 280

SMLP TABLE (2/2)

PKG NAME	FUNCTION NAME	TABLE NAME	TYPE	HARDWARE ACCESS	SIZE (ADDRESS × BIT WIDTH)	PKG No	ADDRESS	DATA	REMARKS
IMH06A	(28) OUTPUT BAND LIMIT S	⑧ READ ENTRY S	RAM	READ/WRITE	8k×8	06	30000 ~ 31FFF	00~07	MB81C79A (EVEN PARITY)
		① VC WRITE ADDRESS COUNTER S	RAM	READ/WRITE	256×18		32000 ~ 320FF	00~17	VCSH-LSI (EVEN PARITY)
		② VC READ ADDRESS COUNTER S	RAM	READ/WRITE	256×18		32100 ~ 321FF	00~17	VCSH-LSI (EVEN PARITY)
		③ VO PEAK RATE S	RAM	READ	256×10		32300 ~ 323FF	00~09	VCSH-LSI (EVEN PARITY)
		④ VC NEXT TIMING S	RAM	READ/WRITE	256×16		32000 ~ 320FF	11~26	VCSH-LSI (EVEN PARITY)
		⑤ VC OK S	RAM	READ/WRITE	256×1			10	
		⑥ VC LIEKY BUCKET S	RAM	READ/WRITE	256×10			00~09	
		⑦ SHAPER CLOCK S	RAM	READ/WRITE	1×16		32800	00~15	VCSH-LSI
		⑩ SHAPER TRANSMISSION OK S	RAM	READ/WRITE	64k×1		80000 ~ 8FFFF	00	MB81C84A (EVEN PARITY)
		⑪ L2 DISCARD COUNT S	D-RAM	READ/WRITE	4k×16	MSR μ-P DIRECTLY-CONNECTED MEMORY (LOGICAL DUPLEX CONFIGURATION)			IDT7024
		L3 DISCARD COUNT S	D-RAM	READ/WRITE					
		⑫ ENCAP. DISCARD COUNT S	D-RAM	READ/WRITE					
		CELL MEMORY S	RAM	READ/WRITE	(FOR 28k CELLS)	MNG NO FIRMWARE ACCESS			TC5516645×3 (VC・SH PARITY CONTROL
	(27) GA COPY S	① FIFO WRITE S	RAM	READ/WRITE	64k×1		90000 ~ 9FFFF	00	MB81C84A (ODD PARITY)
		② IMPLEMENTATION SB. GWMH S	RAM	READ	8×8		A0000 ~ A0007	00~07	MB81C79A (EVEN PARITY)
		CELL MEMORY S	RAM	READ/WRITE	16k×18 (FOR 606 CELLS)	MNG NO FIRMWARE ACCESS			IDT7206×3 (PARITY ODD/EVEN MIXED)
		COPY MEMORY S	RAM	READ/WRITE	8k×18 (FOR 1 CELL)				MB81C79A ×2 (USED IN COMBINATION WITH PARITY OF CELL FIFO S)
	(30) MID ACQUISITION S	① NEXT R & NEXT W COUNTER S	RAM	READ/WRITE	128×9		B0000 ~ B007F	00~08	TC5516645 (ODD PARITY)
		② MID MANAGEMENT TABLE S	RAM	READ/WRITE	16k×8		C0000 ~ C3FFF	00~07	TC5516645 (ODD PARITY)
		③ MID CONVERSION TABLE S	RAM	READ/WRITE	32k×9		D0000 ~ D7FFF	00~08	TC5516645 (ODD PARITY)

FIG. 281

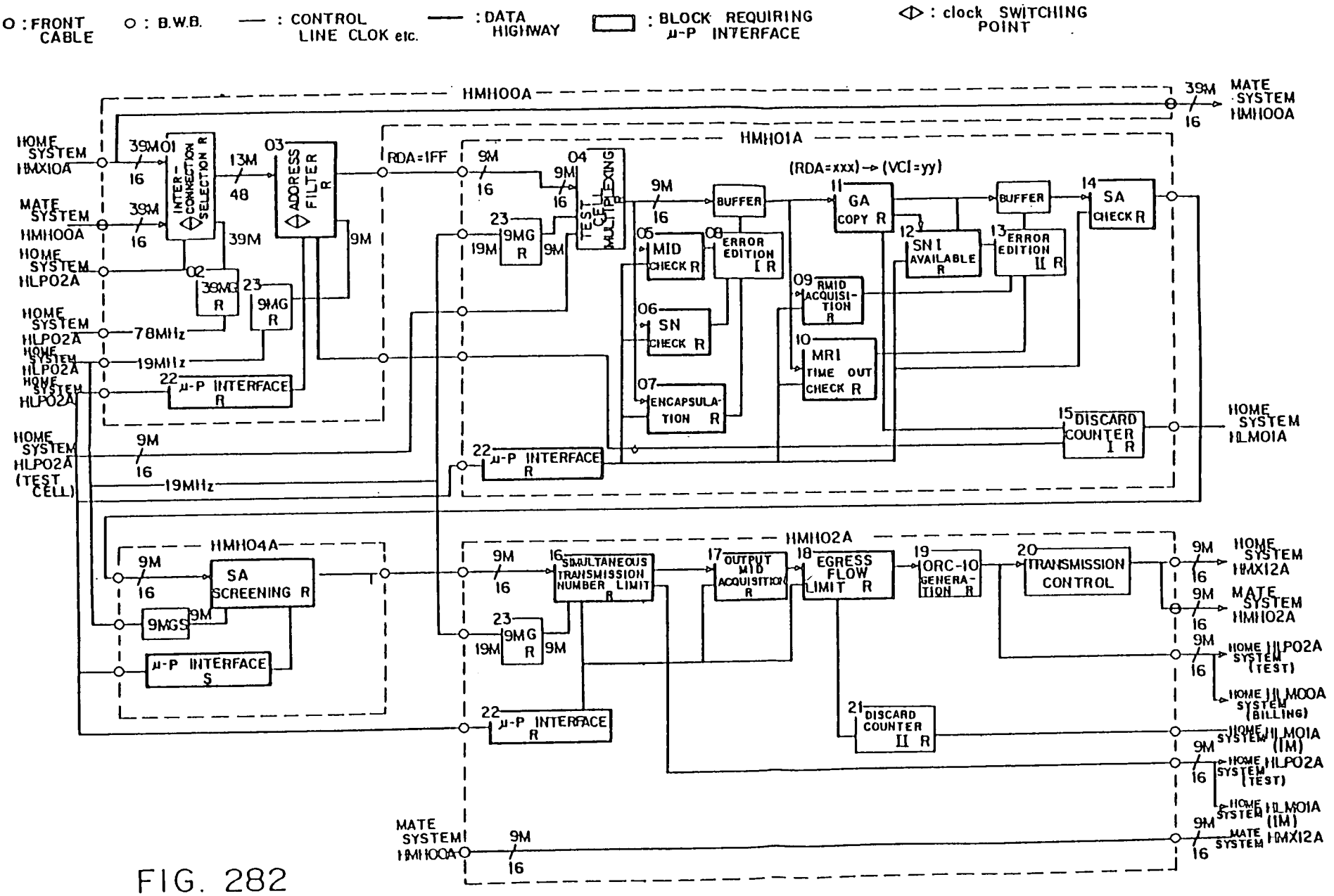

O : FRONT CABLE
O : B.W.B.
— : CONTROL LINE CLOK etc.
— : DATA HIGHWAY
: BLOCK REQUIRING μ-P INTERFACE
◇ : clock SWITCHING POINT
HMH00A
HMH01A
HMH02A
HMH04A
HOME SYSTEM HMX10A
MATE SYSTEM HMH00A
HOME SYSTEM HLP02A
HOME SYSTEM HLP02A 78MHz
HOME SYSTEM HLP02A 19MHz
HOME SYSTEM HLP02A (TEST CELL)
01 INTER-CONNECTION SELECTION R
02
03 ADDRESS FILTER R
04 TEST CELL MULTIPLEXING
05 MID CHECK R
06 SN CHECK R
07 ENCAPSULATION R
08 ERROR EDITION I R
09 RMID ACQUISITION R
10 MRI TIME OUT CHECK R
11 GA COPY R
12 SNI AVAILABLE R
13 ERROR EDITION II R
14 SA CHECK R
15 DISCARD COUNTER I R
16 SIMULTANEOUS TRANSMISSION NUMBER LIMIT R
17 OUTPUT MID ACQUISITION R
18 EGRESS FLOW LIMIT R
19 ORC-10 GENERATION R
20 TRANSMISSION CONTROL
21 DISCARD COUNTER II R
22 μ-P INTERFACE R
23 9MG R
SA SCREENING R
9MGS
μ-P INTERFACE S
BUFFER
RDA=1FF
(RDA=xxx)→(VCI=yy)
HOME SYSTEM HLM01A
HOME SYSTEM HMX12A
MATE SYSTEM HMH02A
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM00A (BILLING)
HOME SYSTEM HLM01A (IM)
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM01A (IM)
MATE SYSTEM HMX12A
MATE SYSTEM HMH00A
39M
13M
9M
19M
78MHz
19MHz
48
16

FIG. 282

ITEM	BLOCK NAME	CONTENTS [ ] : RELATED ERROR FLAG	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	SPE	AL	ERR	
01	INTER-CONNECTION SELECTION R	SELECTING MDX ACT SYSTEM DATA ACCORDING TO SWITCH SYSTEM INFORMATION.	—	○	○	—	MMH 00A
02	39 MG R	RECEVING 78MHZ CLOCK FROM MLP02A AND GENERATING 39MHZ CLOCK USED IN RMLP UNIT AND CELL FRAME.	—	—	—	—	
03	ADDRESS FILTER R	SELECTING CELL TO BE PROCESSED BY RMLP FROM CELLS OF 622M DATA. BUFFERING SELECTED CELLS. AND PASSING THEM TO 150M PROCESSING UNIT. ALSO DISCARDING TCG CELLS.	—	○	○	—	
04	TEST CELL MULTIPLEXING R	MULTIPLEXING TEST CELL FOR SNI LOOPBACK TEST INPUT FROM MLP02A WHEN LINE CONTAINS IDLE CELLS.	○	○	○	—	MMH 01A
05	MID CHECK R	CHECKING WHETHER VCI/MID IS NOT ACTIVE AT BOM. AND WHETHER VCI/MID IS ACTIVE AT COM AND EOM. [MS. MA. MC]	×	○	○	—	
06	SN CHECK R	INITIALIZING SN AT BOM AND SSM. AND CHECKING ORDER OF SN AT COM AND EOM [MS. SN]	×	○	○	—	
07	ENCAPSULATION R	RETRIEVING SIP FROM INTER-MM INF. PDU AND CHANGING ST (SEGMENT TYPE). [MS. SN]	○	○	○	—	
08	ERROR EDITION I R	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG. (MS. MA. MC. SN. EN)	○	○	○	○	
09	RMID ACQUISITION R	COMPRESSING VCI/MID FOR INTERNAL PROCESS. (VCI:8BIT, MID:10BIT) → (RMID:10BIT) [MS. MN. MD]	○	○	○	○	
10	MRI TIME OUT CHECK R	DETERMINING MRI TIMEOUT. (TIMEOUT VALUE: 177MS) TIMEOUT CELL IS TRANSMITTED WHEN TIMEOUT OCCURS. [MS. MT]	○	○	○		
11	GA COPY R	COPYING INPUT CELL IN WHICH DA IS INPUT BY GA AND OUTPUTTING IT TO EACH SUBSCRIBER. [MS. GA]	○	○	○	○	
12	SNI AVAILABLE R	DESCARDING CELL WHEN SNI INDICATES DT FAULT OR RECEPTION ERROR. [MS. DA]	○	×	○	○	
13	ERROR EDITION II R	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG. (MS. MN. MD. MT. GA. DA)	○	○	○	○	
14	SA CHECK R	RETURNING LOOPBACK CELL IN RESPONSE TO GA MESSAGE. [MS. DO]	○	×	○	×	
15	DISCARD COUNTER I R	COUNTING DISCARDED CELLS GENERATED IN 600M-155M CONVERSION UNIT AND GA COPY UNIT. AND REPORTING IT TO MLM01A.	○	×	○	×	

SUB : SNI LOOPBACK TEST CELL SPE: INTER-MM PVC TEST CELL (SPECIAL DA) AL : INTER-MM PVC TEST CELL (ALLOCATED DA)
ERR: ERROR CELL(MASTER ERROR FLAG ON) ○ : APPLIED FOR PROCESS OBJECT OR DURING PROCESS
× : NOT OBJECT OF PROCESS — : NO CELL PASSES OR NO RELATED CELLS

FIG. 283

ITEM	BLOCK NAME	CONTENTS [ ] : RELATED ERROR FLAG	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	SPE	ASS	ERR	
--	SA SCREENING R	LIMITING RECEPTION AT DESTINATION SNI . [MS, SS]	O	×	O	O	HMH 04A
16	SIMULTANEOUS TRANSMISSION NUMBER LIMIT	LIMITING NUMBER OF MESSAGES FOR EACH SNI. [MS, EM, ED]	O	×	O	O	HMH 02A
17	OUTPUT MID ACQUISTION R	CONVERTING FROM EMID (COMPRESSED MID) TO S OUTPUT MID.	O	—	O	—	
18	EGRESS FLOW LIMIT	LIMITING OUTPUT BAND (PEAK RATE) FOR EACH SNI.	O	—	O	—	
19	CRC-10 GENERATION R	GENERATING AND ASSIGNING CRC-10 OF CELL PAYLOAD.	O	—	O	—	
20	TRANSMISSION CONTROL R (DECAPUSLATION)	PREVENTING MHCOM FROM TRANSMITTING ENCAPUSLATED BOM.	O	—	O	—	
21	DISCARD DOUNTER II R	COUNTING CELLS DISCARDED IN EGRESS FLOW LIMITING UNIT AND REPORTING IT TO HLM01A.	O	—	O	—	
22	μ-P INTERFACE R	INTERFACING WITH MNG μ-P OF HLP02A (ACTUALLY USING SCTL2 LSI).	—	—	—	—	COMMON TO EACH PWCB
23	9MG R	RECEIVING 10MHZ CLOCK FROM HLP02A AND GENERATING 9MHZ CLOCK TO BE USED IN RMLP.	—	—	—	—	

SUB : SNI LOOPBACK TEST CELL SPE: TEST USING INTER-MH SPECIAL DA ASS: LOOPBACK TEST INTER-MH ASSIGNED DA
ERR: ERROR CELL(MASTER ERROR FLAG ON) O : APPLIED FOR PROCESS OBJECT OR DURING PROCESS
× : NOT OBJECT OF PROCESS — : NO CELL PASSES OR NO RELATED CELLS

FIG. 284

0 5 3 2 0 4 4 0 5 3 2 0 5

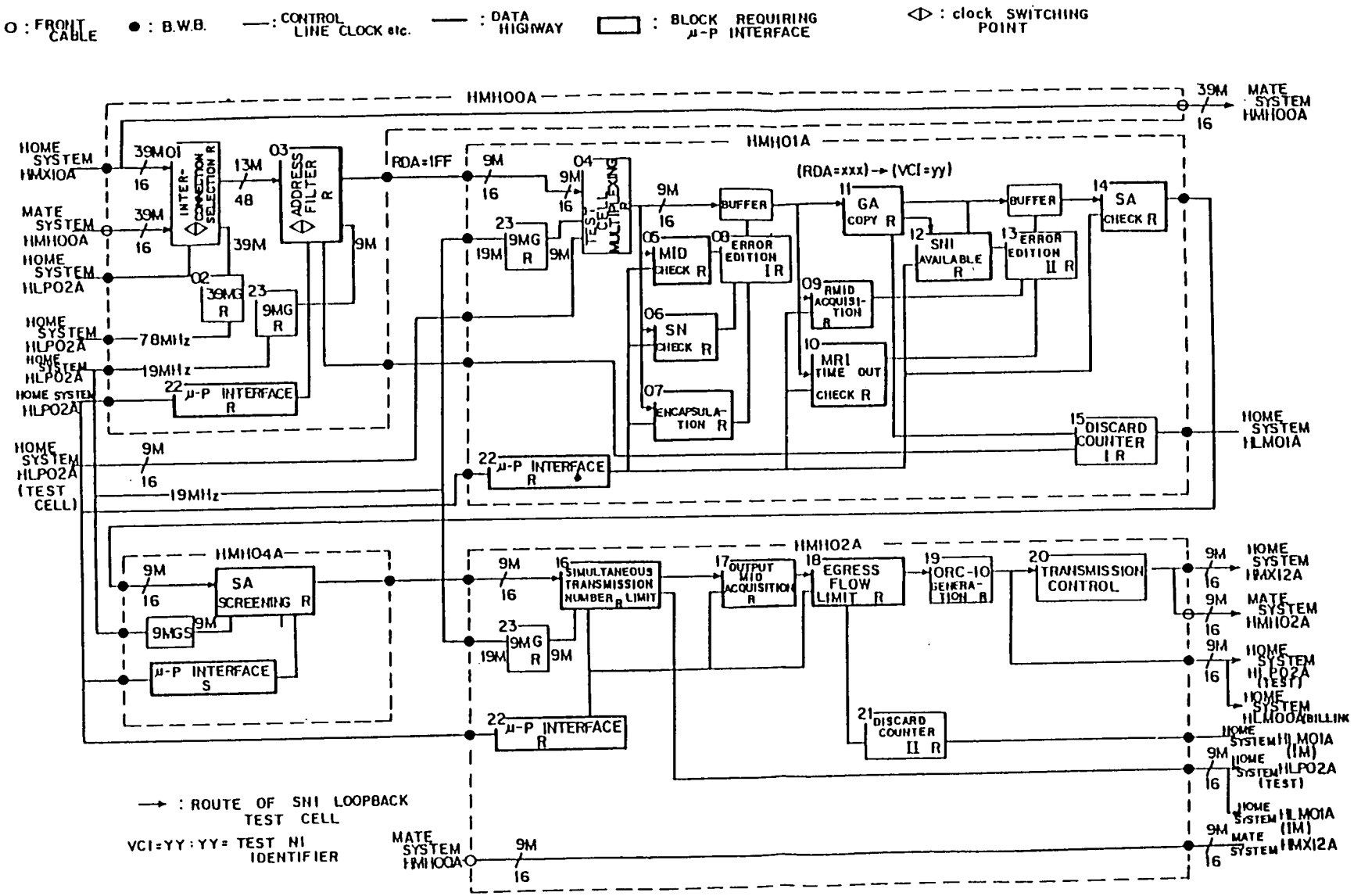

O : FRONT CABLE
● : B.W.B.
—: CONTROL LINE CLOCK etc.
— : DATA HIGHWAY
▭ : BLOCK REQUIRING μ-P INTERFACE
◁▷ : clock SWITCHING POINT
HMH00A
HMH01A
HMH02A
HMH04A
HOME SYSTEM HMX10A
MATE SYSTEM HMH00A
HOME SYSTEM HLP02A
HOME SYSTEM HLP02A (TEST CELL)
78MHz
19MHz
INTER-CONNECTION SELECTION R
ADDRESS FILTER R
RDA=1FF
(RDA=xxx)→(VCI=yy)
TEST LOOP
MULTI
BUFFER
GA COPY R
SA CHECK R
MID CHECK R
ERROR EDITION I R
ERROR EDITION II R
SNI AVAILABLE R
RMID ACQUISITION R
SN CHECK R
MRI TIME OUT CHECK R
ENCAPSULATION R
DISCARD COUNTER I R
DISCARD COUNTER II R
μ-P INTERFACE R
μ-P INTERFACE S
SA SCREENING R
SIMULTANEOUS TRANSMISSION NUMBER LIMIT R
OUTPUT M/O ACQUISITION R
EGRESS FLOW LIMIT R
ORC-IO GENERATION R
TRANSMISSION CONTROL
HOME SYSTEM HMX12A
MATE SYSTEM HMH02A
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM00A (BILLING)
HOME SYSTEM HLM01A (IM)
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM01A (IM)
MATE SYSTEM HMX12A
HOME SYSTEM HLM01A
→ : ROUTE OF SNI LOOPBACK TEST CELL
VCI=YY : YY= TEST NI IDENTIFIER

FIG. 285

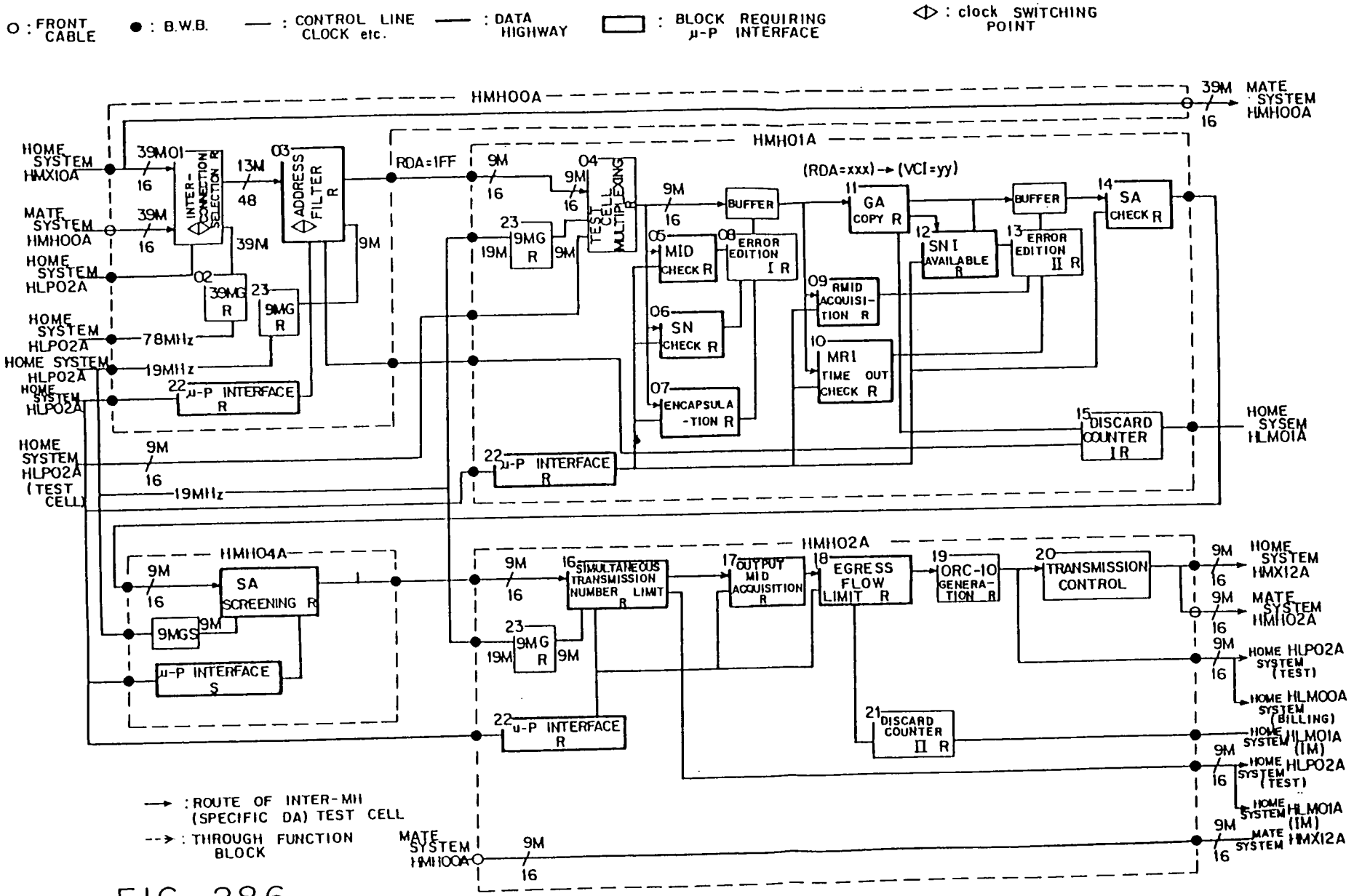

O : FRONT CABLE
● : B.W.B.
— : CONTROL LINE CLOCK etc.
— : DATA HIGHWAY
▭ : BLOCK REQUIRING μ-P INTERFACE
◇ : clock SWITCHING POINT
HMH00A
HMH01A
HMH02A
HMH04A
HOME SYSTEM HMX10A
MATE SYSTEM HMH00A
HOME SYSTEM HLP02A
HOME SYSTEM HLP02A
HOME SYSTEM HLP02A
HOME SYSTEM HLP02A
HOME SYSTEM HLP02A (TEST CELL)
39M01
INTER-CONNECTION SELECTION
13M
48
03 ADDRESS FILTER R
39M
16
9M
RDA=1FF
02 39MG R
23 9MG R
78MHz
19MHz
22 μ-P INTERFACE R
04 TEST CELL MULTIPLEXING R
(RDA=xxx)→(VCI=yy)
05 MID CHECK R
06 SN CHECK R
07 ENCAPSULATION R
08 ERROR EDITION I R
09 RMID ACQUISITION R
10 MRI TIME OUT CHECK R
11 GA COPY R
12 SNI AVAILABLE R
13 ERROR EDITION II R
14 SA CHECK R
15 DISCARD COUNTER I R
BUFFER
MATE SYSTEM HMH00A
HOME SYSEM HLM01A
SA SCREENING R
9MGS
μ-P INTERFACE S
16 SIMULTANEOUS TRANSMISSION NUMBER LIMIT R
17 OUTPUT MID ACQUISITION R
18 EGRESS FLOW LIMIT R
19 ORC-10 GENERATION R
20 TRANSMISSION CONTROL
21 DISCARD COUNTER II R
HOME SYSTEM HMX12A
MATE SYSTEM HMH02A
HOME HLP02A SYSTEM (TEST)
HOME HLM00A SYSTEM (BILLING)
HOME SYSTEM HLM01A (IM)
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM01A (IM)
MATE SYSTEM HMX12A
→ : ROUTE OF INTER-MH (SPECIFIC DA) TEST CELL
--→ : THROUGH FUNCTION BLOCK

FIG. 286

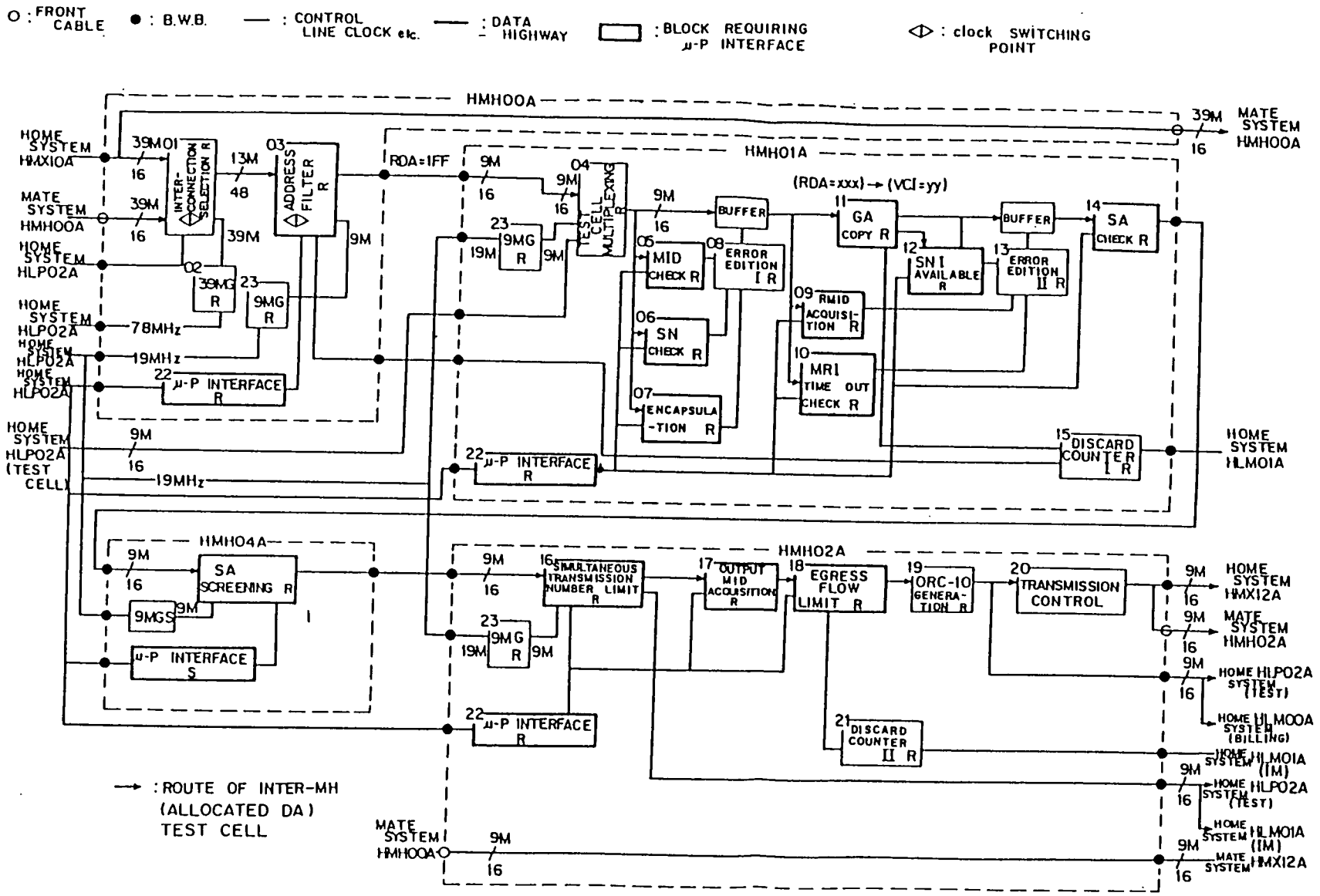

O : FRONT CABLE
● : B.W.B.
— : CONTROL LINE CLOCK etc.
— : DATA HIGHWAY
: BLOCK REQUIRING μ-P INTERFACE
: clock SWITCHING POINT
HMH00A
HMH01A
HMH04A
HMH02A
HOME SYSTEM HMX10A
MATE SYSTEM HMH00A
HOME SYSTEM HLP02A
HOME SYSTEM HLP02A
78MHz
HOME SYSTEM HLP02A
19MHz
HOME SYSTEM HLP02A
μ-P INTERFACE R
HOME SYSTEM HLP02A (TEST CELL)
19MHz
39M01
INTER-CONNECTION SELECTION R
02
39MG R
9MG R
03
ADDRESS FILTER R
RDA=1FF
04
TEST CELL MULTIPLEXING R
05
MID CHECK R
06
SN CHECK R
07
ENCAPSULATION R
08
ERROR EDITION I R
09
RMID ACQUISITION R
10
MRI TIME OUT CHECK R
11
GA COPY R
12
SNI AVAILABLE R
13
ERROR EDITION II R
14
SA CHECK R
15
DISCARD COUNTER I R
BUFFER
(RDA=xxx)→(VCI=yy)
HOME SYSTEM HLM01A
MATE SYSTEM HMH00A
16
SIMULTANEOUS TRANSMISSION NUMBER LIMIT R
17
OUTPUT MID ACQUISITION R
18
EGRESS FLOW LIMIT R
19
ORC-10 GENERATION R
20
TRANSMISSION CONTROL
21
DISCARD COUNTER II R
22
μ-P INTERFACE R
23
9MG R
SA SCREENING R
9MGS
μ-P INTERFACE S
HOME SYSTEM HMX12A
MATE SYSTEM HMH02A
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM00A (BILLING)
HOME SYSTEM HLM01A (IM)
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM01A (IM)
MATE SYSTEM HMX12A
→ : ROUTE OF INTER-MH (ALLOCATED DA) TEST CELL

FIG. 287

6698260 "ET27260

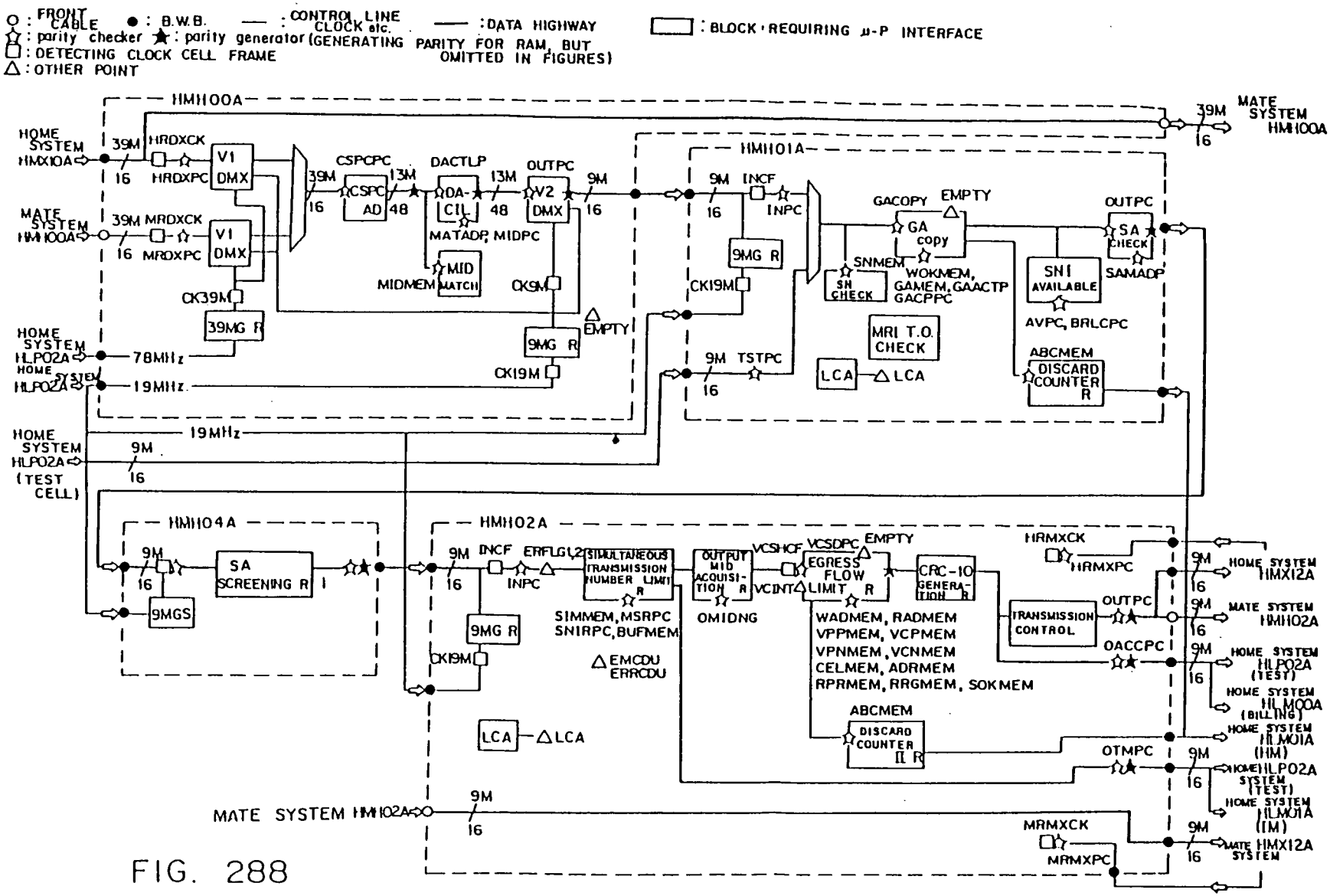


FIG. 288

6693E0 E12760

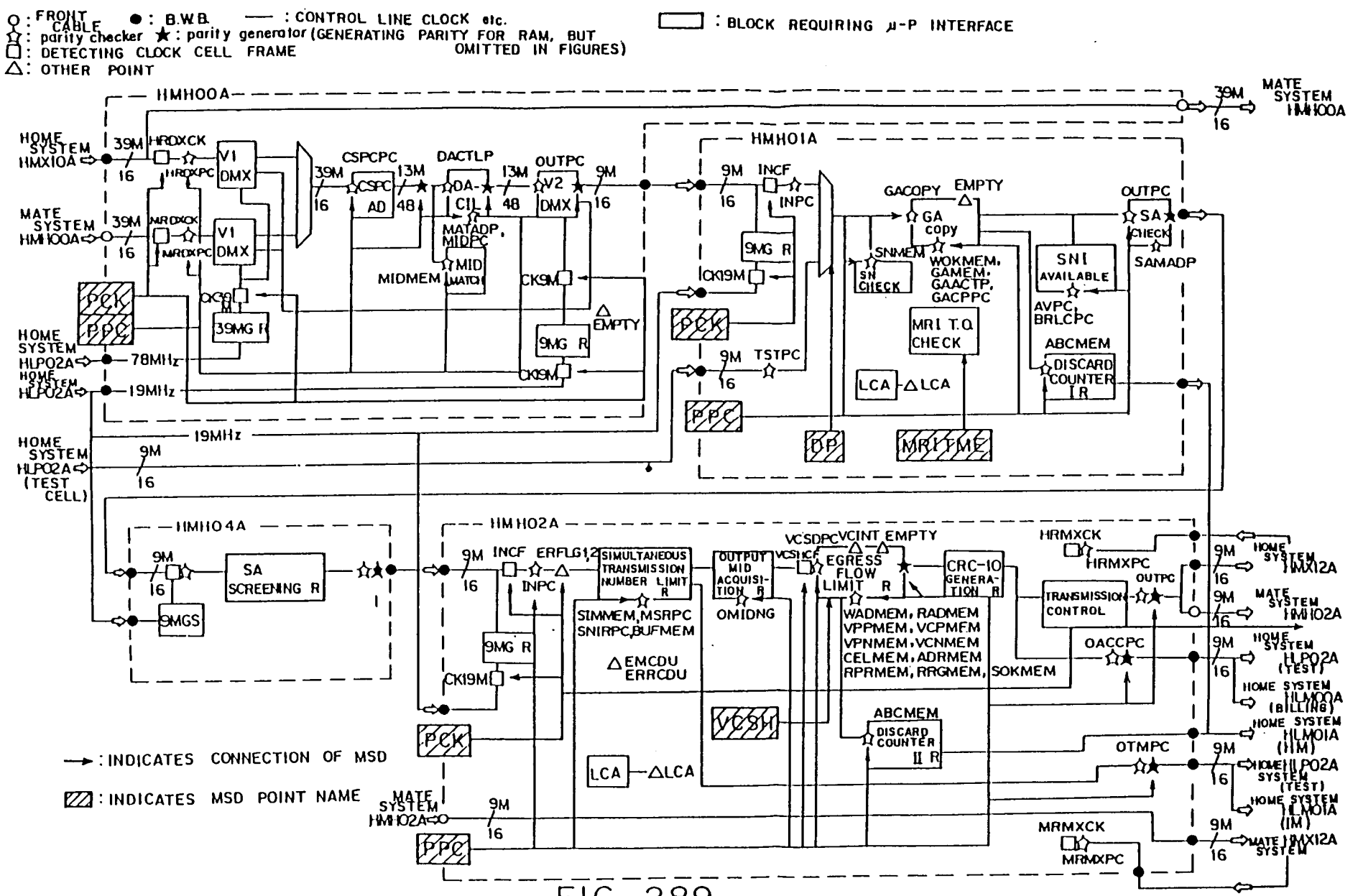


FIG. 289

BLOCK NAME \ EF	E1 MS	E2 MA	E1 MC	E2 SN	E2 EN	E2 MN	E1 MD	E2 MT	E1 GA	E2 DA	E2 DO	E2 SS	E2 EM	E1 ED	PVC TEST SUB	SPE	ASS
MID CHECK R (B/S) DM=0	ON	ON	–	–	–	–	–	–	–	–	–	–	–	–	×		
MID CHECK R (B/S) DM=1	–	ON	–	–	–	–	–	–	–	–	–	–	–	–	×		
MID CHECK R (C/E)	ON	–	ON	–	–	–	–	–	–	–	–	–	–	–	×		
SN CHECK R (C/E)	ON	–	–	ON	–	–	–	–	–	–	–	–	–	–	×		
ENCAPSULATION R (ISSIS)	ON	–	–	–	ON	–	–	–	–	–	–	–	–	–			
RMID ACQUISITION R (B/S)	ON	–	–	–	–	ON	–	–	–	–	–	–	–	–			
RMID ACQUISITION R (C/E)	ON	–	–	–	–	–	ON	–	–	–	–	–	–	–			
MRI TIMEOUT CHECK R (TO CELL)	ON	–	–	–	–	–	–	ON	–	–	–	–	–	–			
CELL ARRIVING AFTER TIMEOUT (C/E)	ON	–	–	–	–	–	ON	–	–	–	–	–	–	–			
GA COPY R	ON	–	–	–	–	–	–	–	ON	–	–	–	–	–			

IF IBOM ARRIVES BEFORE IEOM, MS AND GA IS SET ON (COPYING FOR RDA AFTER COPYING FOR RMID)
IF MS IS SET ON IN ICOM (EFMD IS ALSO SET ON), CELL IS TRANSMITTED WITH VCI=E0
WHEN CELL WHOSE E1MS IS SET ON IS COPIED, FLAG AT EF2 IS MASKED AND E1GA IS SET ON (TO PREVENT DOUBLE COUNT)

SNI AVAILABLE R (B/S)	ON	–	–	–	–	–	–	◇	–	ON	–	–	–	–		×	
SA CHECK R (B/S)	ON ○	–	–	–	–	–	–	–	–	–	ON	–	–	–		×	
SA SCREENING R (B/S)	ON	–	–	–	–	–	–	–	–	–	–	ON	–	–		×	
SIMULTANEOUS TRANSMISSION NUMBER LIMIT R (B)	ON	–	–	–	–	–	–	–	–	–	–	–	ON	–		×	
SIMULTANEOUS TRANSMISSION NUMBER LIMIT R (C/E)	ON	–	–	–	–	–	○	–	–	–	–	–	–	ON		×	

'ON' : EF WHICH IS SET ON WHEN CHECK RESULT INDICATES NG.
'○' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK.
'SUB' : SUBSCRIBER LOOPBACK TEST
'ASS' : TEST USING INTER-MH ASSIGNED DA
'–' : CHECK IS MADE REGARDLESS OF OK/NG OF EF WITH THIS MARK
'SPE' : TEST USING INTER-MH SPECIAL DA
'×' : NO CHECK IS MADE WHEN CELL TESTED IN SPECIFIED PVC TEST.

FIG. 290

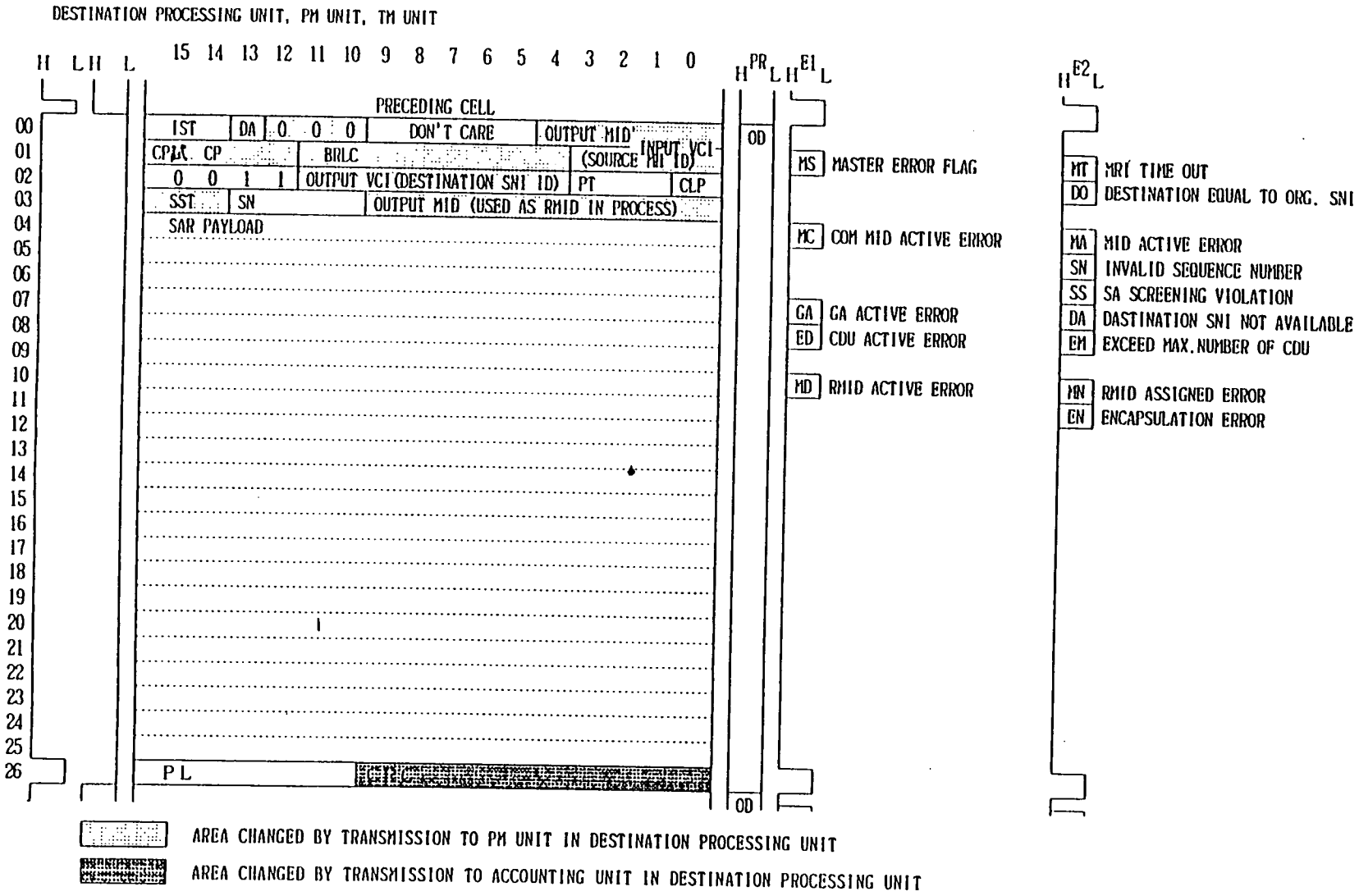

DESTINATION PROCESSING UNIT, PM UNIT, TM UNIT
H L H L
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
H PR L H EI L
H E2 L
PRECEDING CELL
00 IST DA 0 0 0 DON'T CARE OUTPUT MID
01 CPCS CP BRLC (SOURCE INPUT VCI ID)
02 0 0 1 1 OUTPUT VCI (DESTINATION SNI ID) PT CLP
03 SST SN OUTPUT MID (USED AS RMID IN PROCESS)
04 SAR PAYLOAD
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26 PL CRC
OD
OD
MS MASTER ERROR FLAG
MC COM MID ACTIVE ERROR
GA GA ACTIVE ERROR
ED CDU ACTIVE ERROR
MD RMID ACTIVE ERROR
MT MRI TIME OUT
DO DESTINATION EQUAL TO ORG. SNI
MA MID ACTIVE ERROR
SN INVALID SEQUENCE NUMBER
SS SA SCREENING VIOLATION
DA DASTINATION SNI NOT AVAILABLE
EM EXCEED MAX. NUMBER OF CDU
MN RMID ASSIGNED ERROR
EN ENCAPSULATION ERROR
AREA CHANGED BY TRANSMISSION TO PM UNIT IN DESTINATION PROCESSING UNIT
AREA CHANGED BY TRANSMISSION TO ACCOUNTING UNIT IN DESTINATION PROCESSING UNIT

FIG. 291

ITEM		INTER-MH BOM	SIP BOM	SIP COM	EOM	SIP SSM	INTER-MH SSM
CELL00	IST	10	00	00	01	01	11
CELL03	SST	10	10	10	01	11	11
CELL26	PL	2CH	2CH	2CH	4H-2CH	24H-2CH	—
E101	EFMS	ERRONEOUS OR (ERROR: L)					L
E201	EFMT	(NONE)		L AT MRI TIMEOUT		(NONE)	
E204	EFMA	L WHEN ACTIVE (NOT OBJECT OF EFMS)	(NONE)		L IN NO ACTIVE		L IN ACTIVE STATE (NOT OBJECT OF EFMS)
E104	EFMC	(NONE)	L WHEN NO ACTIVE		(NONE)		
E205	EFSN	NO CHECK	L AT SN ORDER ERROR				NO CHECK
E210	EFMN	L WHEN RMID IS UNAVAILABLE	(NONE)				L WHEN RMID IS UNAVAILABLE
E110	EFMD	(NONE)	L WHEN RMID IS NOT CONVERTIBLE				(NONE)
E211	EFEN	(NONE)					ALL "L"
E106	EFGA	DISCARDED CELL L WHEN RMID ACTIVE	(NONE)				L WHEN RMID ACTIVE
E207	EFDA	L WHEN DESTINATION SMI IS UNAVAILABLE	(STOP AT SIMULTANEOUS TRANSMISSION NUMBER LIMITING MECHANISM)				L WHEN DESTINATION SMI IS UNAVAILABLE
E202	EFDO	L AT SELF-LOOPBACK	(STOP AT SIMULTANEOUS TRANSMISSION NUMBER LIMITING MECHANISM)				L AT SELF-LOOPBACK
E206	EFSS	L AT SCREENING VIOLATION	(STOP AT SIMULTANEOUS TRANSMISSION NUMBER LIMITING MECHANISM)				L AT SCREENING VIOLATION
E208	EFEM	L AT DISCARD UNDER SIMULTANEOUS TRANSMISSION CONTROL	NONE				(NO CHECK)
E108	EFED	(NONE)	L AT STOP UNDER SIMULTANEOUS TRANSMISSION CONTROL				(NONE)

FIG. 292

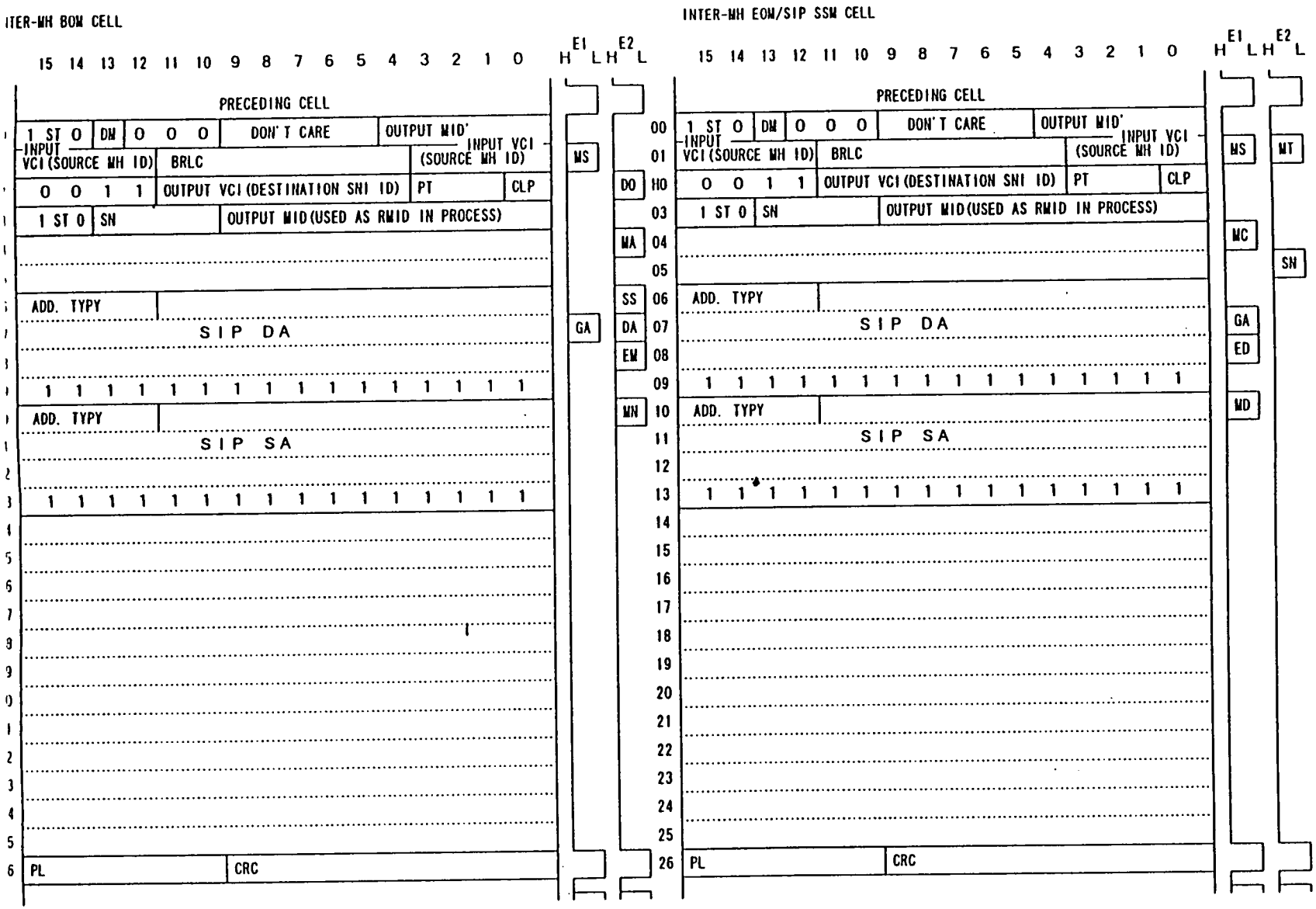

ITER-MH BOM CELL
INTER-MH EOM/SIP SSM CELL
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
E1 H L
E2 H L
PRECEDING CELL
1 ST 0
DM
0 0 0
DON'T CARE
OUTPUT MID'
INPUT VCI (SOURCE MH ID)
BRLC
INPUT VCI (SOURCE MH ID)
0 0 1 1
OUTPUT VCI (DESTINATION SNI ID)
PT
CLP
SN
OUTPUT MID (USED AS RMID IN PROCESS)
ADD. TYPY
SIP DA
SIP SA
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
PL
CRC
MS
GA
DO
MA
SS
DA
EM
MN
MT
MC
SN
ED
MD
00
01
H0
03
04
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
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21
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25
26

FIG. 293

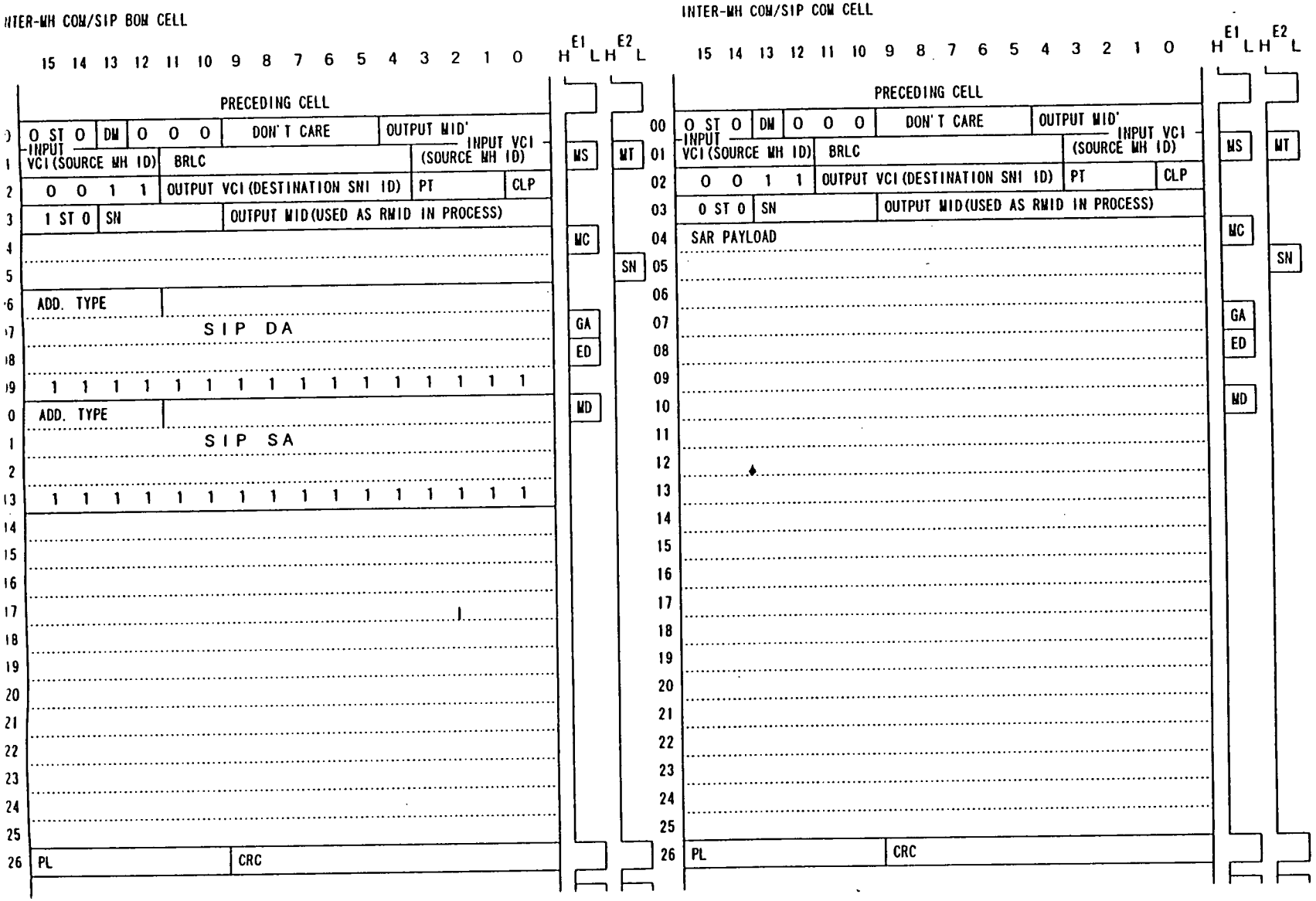

INTER-MH COM/SIP BOM CELL
INTER-MH COM/SIP COM CELL
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
E1 H L
E2 H L
PRECEDING CELL
0 ST 0
DM
DON'T CARE
OUTPUT MID
INPUT VCI (SOURCE MH ID)
BRLC
OUTPUT VCI (DESTINATION SNI ID)
PT
CLP
1 ST 0
SN
OUTPUT MID (USED AS RMID IN PROCESS)
SAR PAYLOAD
ADD. TYPE
SIP DA
SIP SA
PL
CRC
MS
MT
MC
SN
GA
ED
MD

FIG. 294

INTER MH EOM/SIP EOM CELL

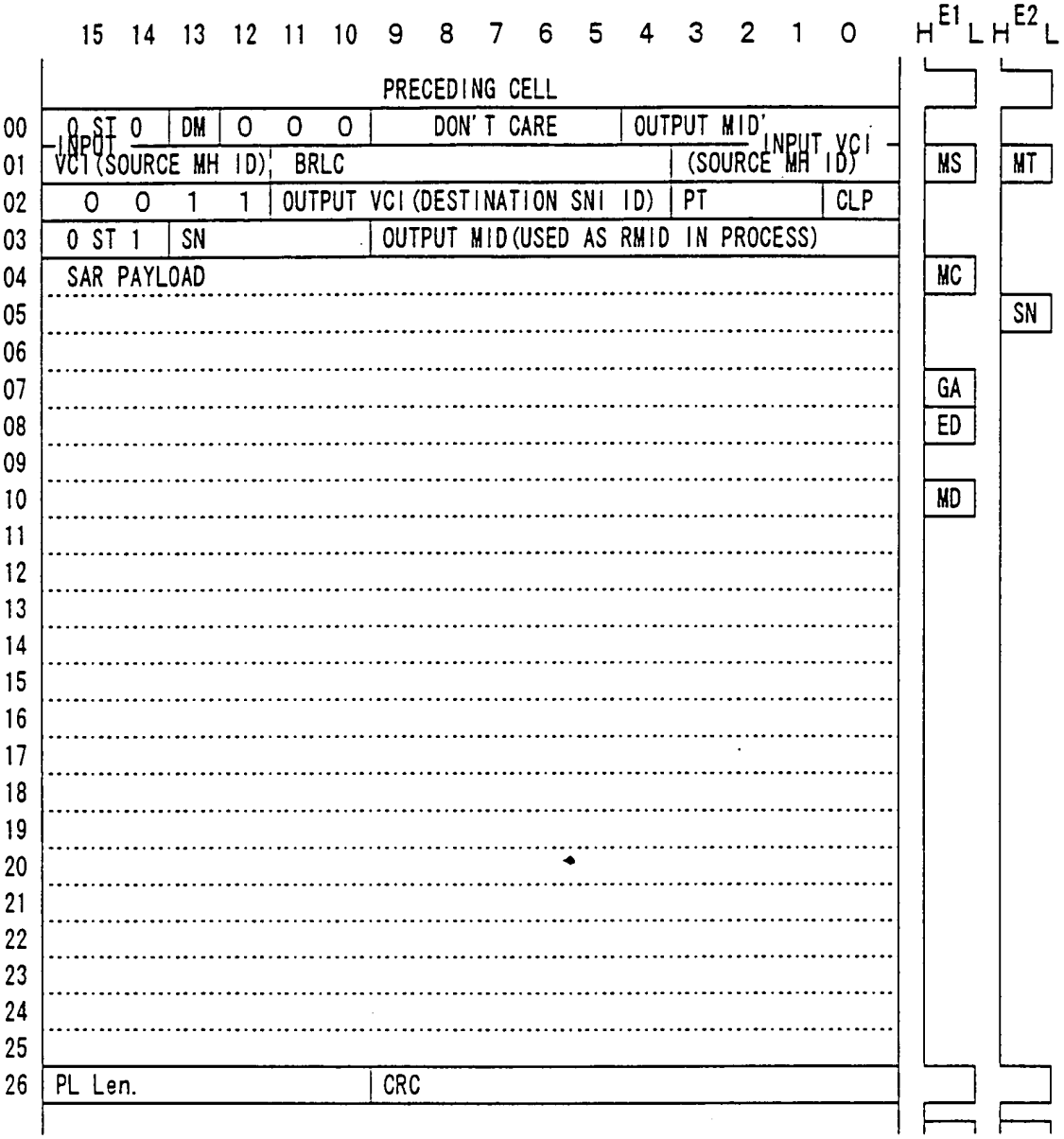


FIG. 295

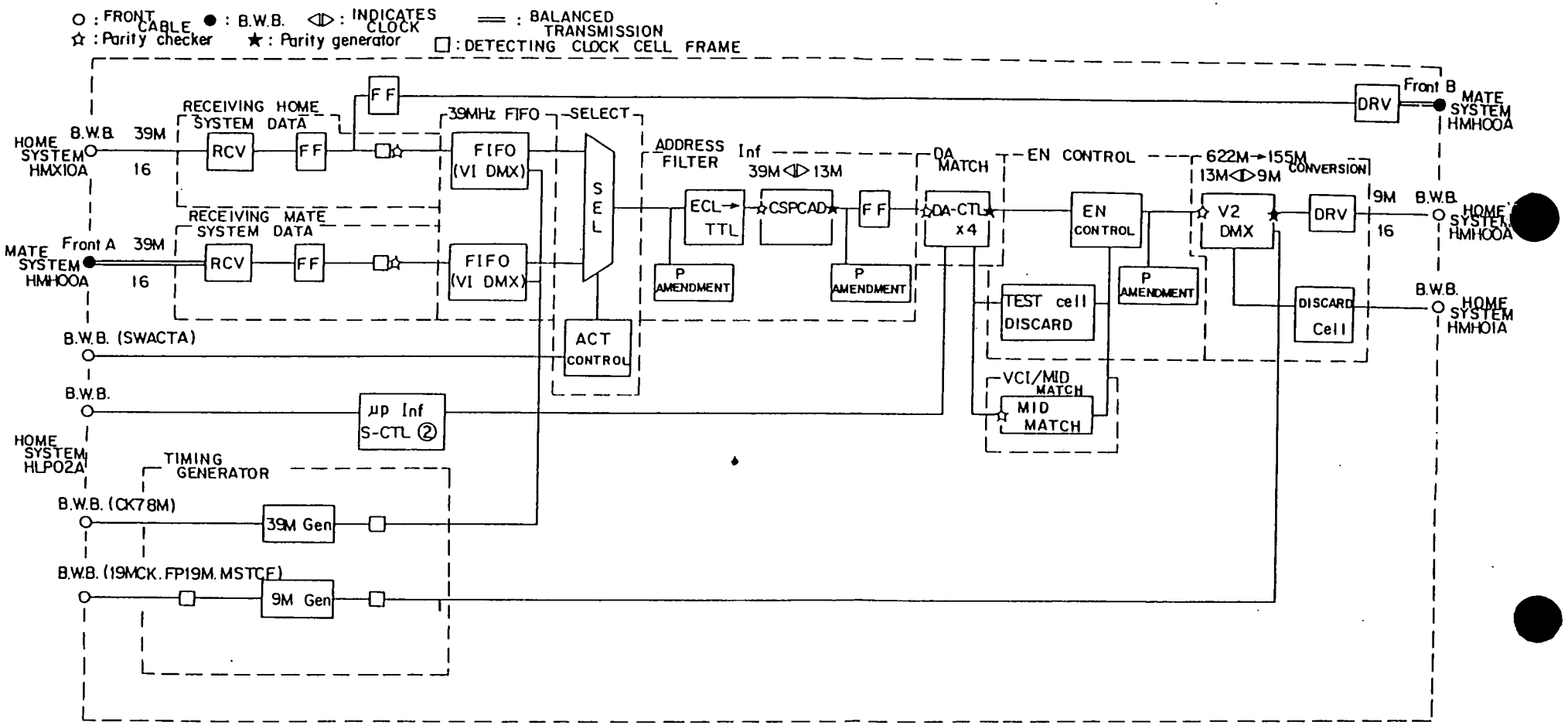

○ : FRONT CABLE
● : B.W.B.
◁▷ : INDICATES CLOCK
═ : BALANCED TRANSMISSION
☆ : Parity checker
★ : Parity generator
□ : DETECTING CLOCK CELL FRAME
HOME SYSTEM HMX10A
B.W.B.
39M
16
RECEIVING HOME SYSTEM DATA
RCV
FF
FF
39MHz FIFO
FIFO (VI DMX)
SELECT
SEL
ADDRESS FILTER
Inf
39M◁▷13M
ECL→TTL
CSPCAD
FF
OA MATCH
OA-CTL x4
EN CONTROL
EN CONTROL
622M→155M 13M◁▷9M CONVERSION
V2 DMX
DRV
9M
B.W.B.
HOME SYSTEM HMH00A
16
DRV
Front B
MATE SYSTEM HMH00A
MATE SYSTEM HMH00A
Front A
39M
16
RECEIVING MATE SYSTEM DATA
RCV
FF
FIFO (VI DMX)
P AMENDMENT
P AMENDMENT
P AMENDMENT
TEST cell DISCARD
DISCARD Cell
B.W.B.
HOME SYSTEM HMH01A
B.W.B. (SWACTA)
ACT CONTROL
B.W.B.
HOME SYSTEM HLP02A
μp Inf S-CTL ②
VCI/MID MATCH
MID MATCH
TIMING GENERATOR
B.W.B. (CK78M)
39M Gen
B.W.B. (19MCK. FP19M. MSTCE)
9M Gen

FIG. 296

ITEM	BLOCK NAME	REMARKS
01	CROSS-CONNECTION SELECT R	SELECTING ACTIVE SYSTEM DATA OF MDX ACCORDING TO SWITCH SYSTEM INFORMATION
02	TIMING GENERATOR R	RECEIVING 78MHz CLOCK FROM HLP02A FOR USE IN RMLP. GENERATING 39MHz AND 9MHz CLOCK AND CELL FRAME
03	ADDRESS FILTER R	SELECTING CELL TO BE PROCESSED AT RMLP FROM CELLS IN 622M DATA, AND BUFFERING AND PASSING SELECTED CELL TO 155M PROCESSING UNIT

FIG. 297

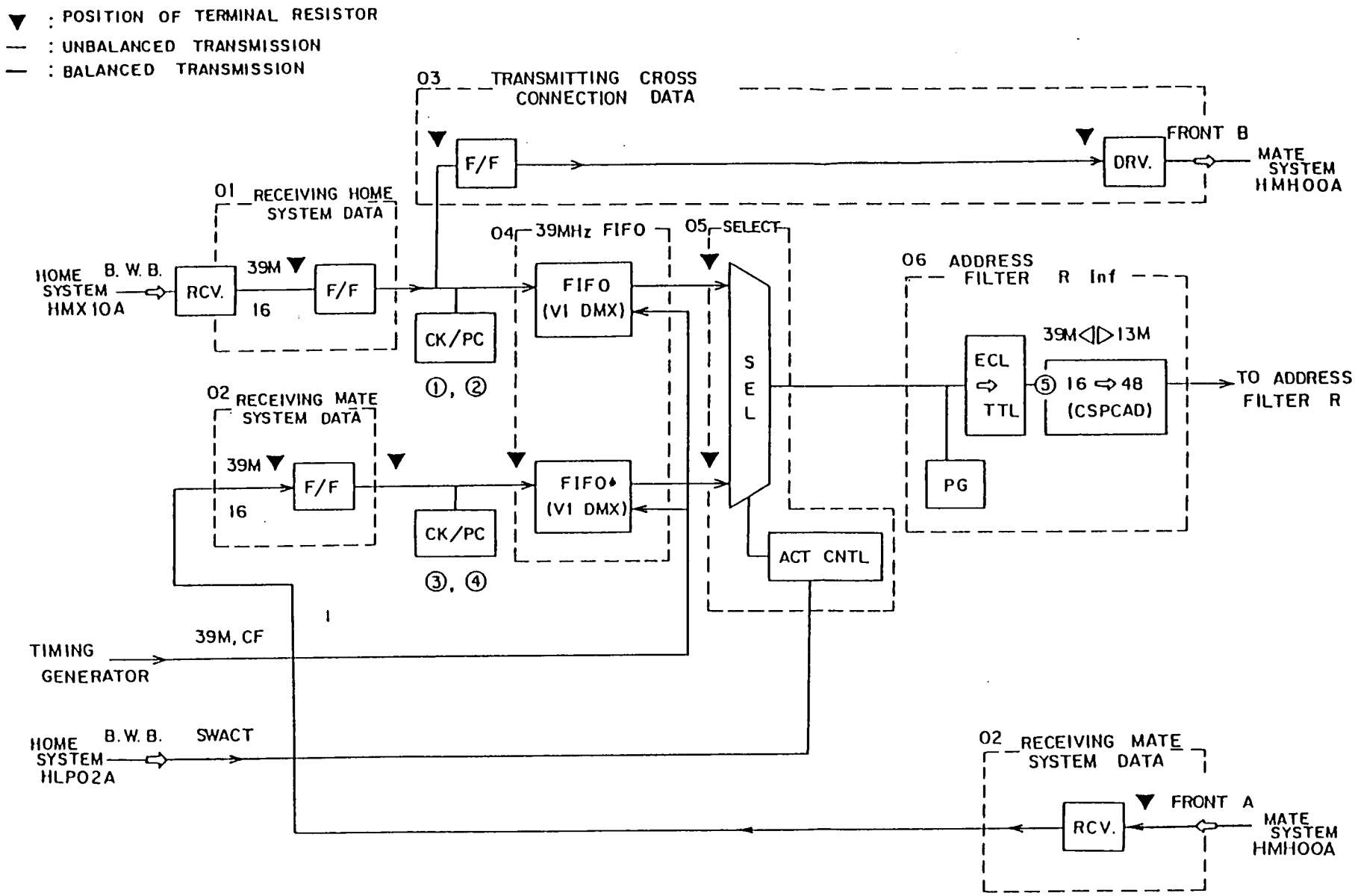

▼ : POSITION OF TERMINAL RESISTOR
— : UNBALANCED TRANSMISSION
— : BALANCED TRANSMISSION
03 TRANSMITTING CROSS CONNECTION DATA
F/F
DRV.
FRONT B
MATE SYSTEM HMH00A
01 RECEIVING HOME SYSTEM DATA
HOME SYSTEM HMX10A
B. W. B.
RCV.
39M
16
F/F
04 39MHz FIFO
FIFO (V1 DMX)
CK/PC
①, ②
05 SELECT
S E L
06 ADDRESS FILTER R Inf
39M◁▷13M
ECL ⇨ TTL
⑤ 16 ⇨ 48 (CSPCAD)
TO ADDRESS FILTER R
PG
02 RECEIVING MATE SYSTEM DATA
39M
16
F/F
FIFO (V1 DMX)
CK/PC
③, ④
ACT CNTL
TIMING GENERATOR
39M, CF
HOME SYSTEM HLP02A
B. W. B.
SWACT
02 RECEIVING MATE SYSTEM DATA
RCV.
FRONT A
MATE SYSTEM HMH00A

FIG. 298

ITEM	FUNCTION BLOCK NAME	REMARKS
01	RECEIVING HOME SYSTEM DATA	RECEIVING 39M16 PARALLEL DATA AS ECL UNBALANCED FROM HOME SYSTEM MHCOM THROUGH B.W.B CHECKING CLOCK, CELL FRAME DISCONNECTION, AND PARITY
02	RECEIVING MATE SYSTEM DATA	RECEIVING 39M16 PARALLEL DATA AS ECL BALANCED FROM MATE SYSTEM MHCOM THROUGH FRONT ACONN. CHECKING CLOCK, CELL FRAME DISCONNECTION, AND PARITY.
03	TRANSMITTING CROSS-CONNECTION DATA	TRANSMITTING DATA RECEIVED FROM HOME MHCOM THROUGH B.W.B TO HMH00A OF MATE SYSTEM.
04	39MHz FIFO	REALLOCATING CLOCK USING V1 DMX LSI. READING DATA RECEIVED BY HOME AND MATE SYSTEMS IN SYNCHRONISM WITH READING CLOCK AND CELL FRAME.
05	SELECTING CROSS-COMMECTION DATA	SELECTING DATA RECEIVED FROM MHCOM OF HOME AND MATE SYSTEM ACCORDING TO ACT OF MHCOM. SWITCHING SYSTEMS IN SYNCHRONISM WITH FIFO READ CELL FRAME.
06	ADDRESS FILTER R INF	CONVERTING 39M/16 PARALLEL ECL DATA INTO 13M/48 PARALLEL TTL USING CSPCAD LSI TO INTERFACE WITH ADDRESS FILTER R.

FIG. 299

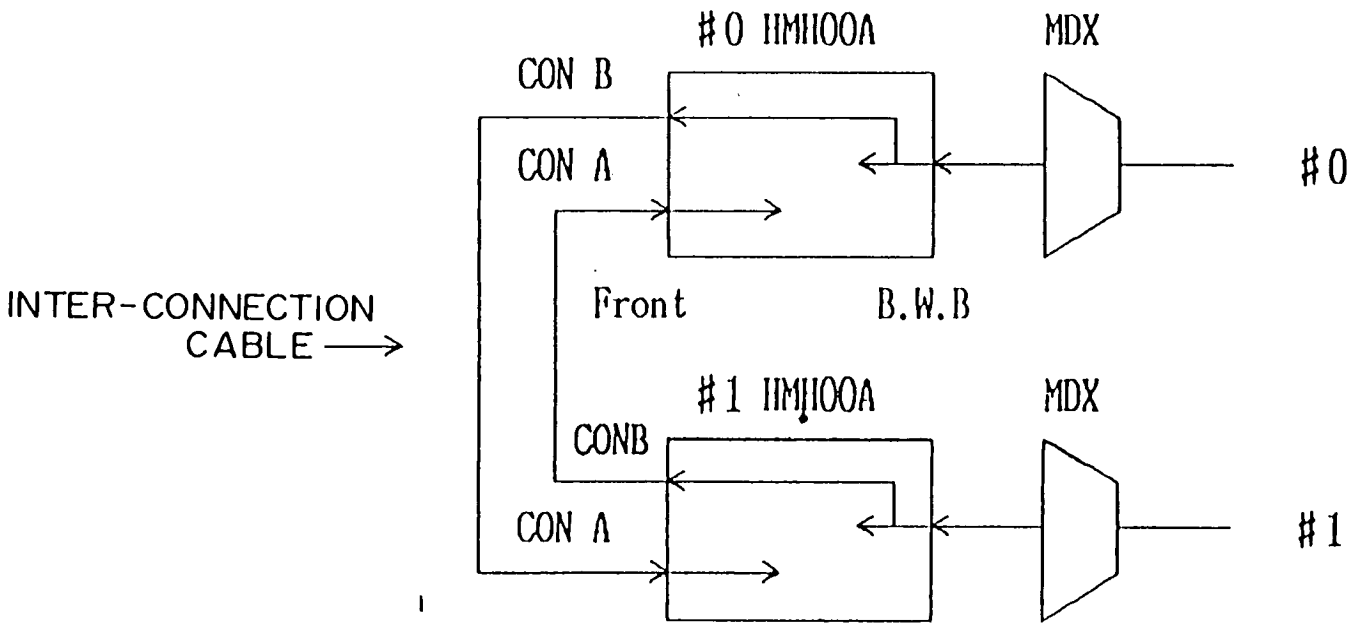

#0 HMH00A
MDX
CON B
CON A
#0
INTER-CONNECTION
CABLE
Front
B.W.B
#1 HMH00A
MDX
CONB
CON A
#1

FIG. 300

669260-ET22260

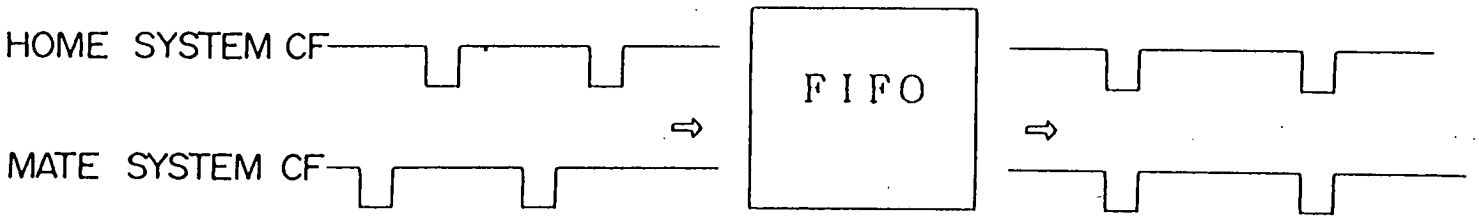


FIG. 301

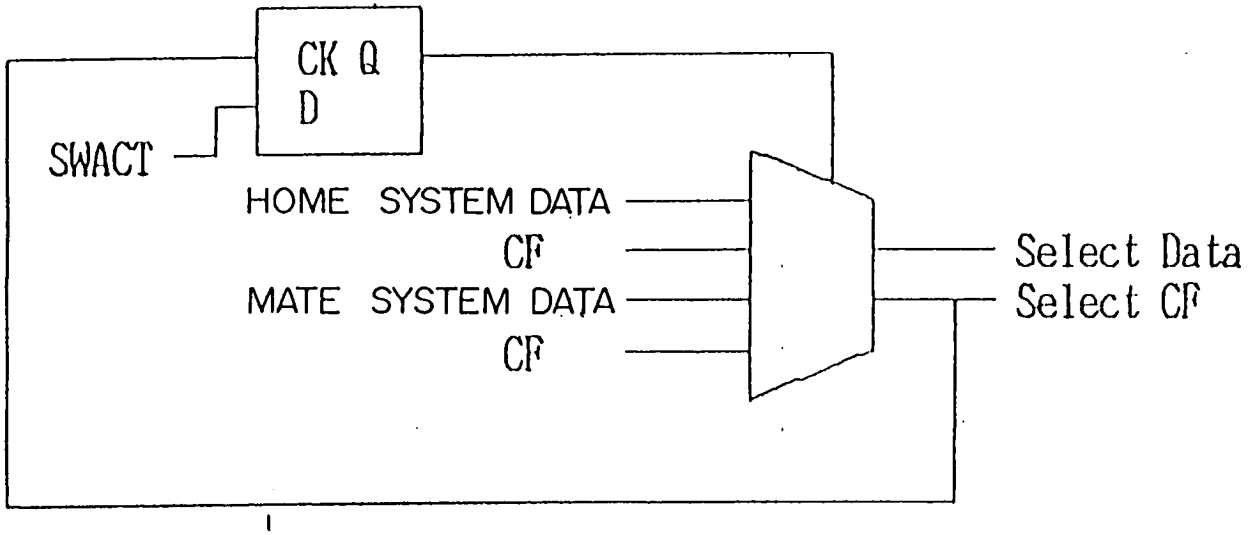

CK Q
D
SWACT
HOME SYSTEM DATA
CF
MATE SYSTEM DATA
CF
Select Data
Select CF

FIG. 302

ITEM	POINT NAME	REMARKS
①	HRDXCK	DISCONNECTION OF INPUT CLOCK 39M AND CELL FRAME FROM HOME SYSTEM MHCOM
②	HRDXPC	PARITY HECK ERROR OF INPUT DATA FROM HOME SYSTEM MHCOM
③	MRDXCK	DISCONNECTION OF INPUT CLOCK 39M AND CELL FRAME FROM MATE SYSTEM MHCOM
④	MRDXPC	PARITY CHECK ERROR OF INPUT DATA FROM MATE SYSTEM MHCOM
⑤	CSPCPC	PARITY CHECK ERROR OF INPUT DATA TO CSPCAD LSI

FIG. 303

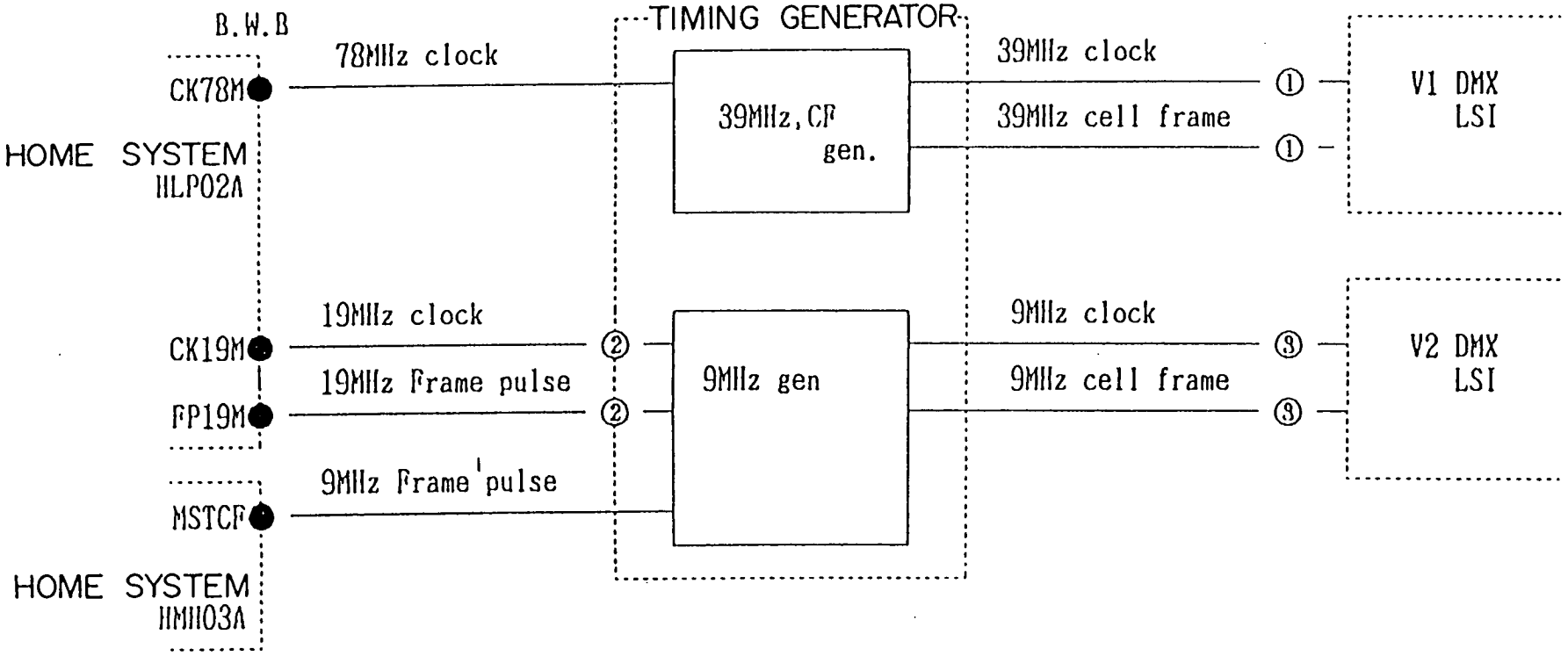

B.W.B
78MHz clock
CK78M
HOME SYSTEM
HLP02A
TIMING GENERATOR
39MHz,CF
gen.
39MHz clock
39MHz cell frame
①
①
V1 DMX
LSI
19MHz clock
CK19M
19MHz Frame pulse
FP19M
②
②
9MHz gen
9MHz clock
9MHz cell frame
③
③
V2 DMX
LSI
9MHz Frame pulse
MSTCF
HOME SYSTEM
HMI03A

FIG. 304

ITEM	FUNCTION BLOCK NAME	REMARKS
01	39MHz GEN.	RECEIVING 78MHz CLOCK AND GENERATING 39MHz CLOCK AND FRAME PULSE
02	39MHz CF GEN.	GENERATING READ CF OF V2 DMX LSI FROM GENERATED CLOCK AND FRAME PULSE
03	9MHz GEN.	RECEIVING 19MHz CLOCK AND FRAME PULSE, GENERATING 9MHz CLOCK, AND MAKING CELL FRAME IN SYNCHRONISM WITH MSTCF. READING V2 DMX LSI USING THIS CLOCK AND CELL FRAME.

FIG. 305

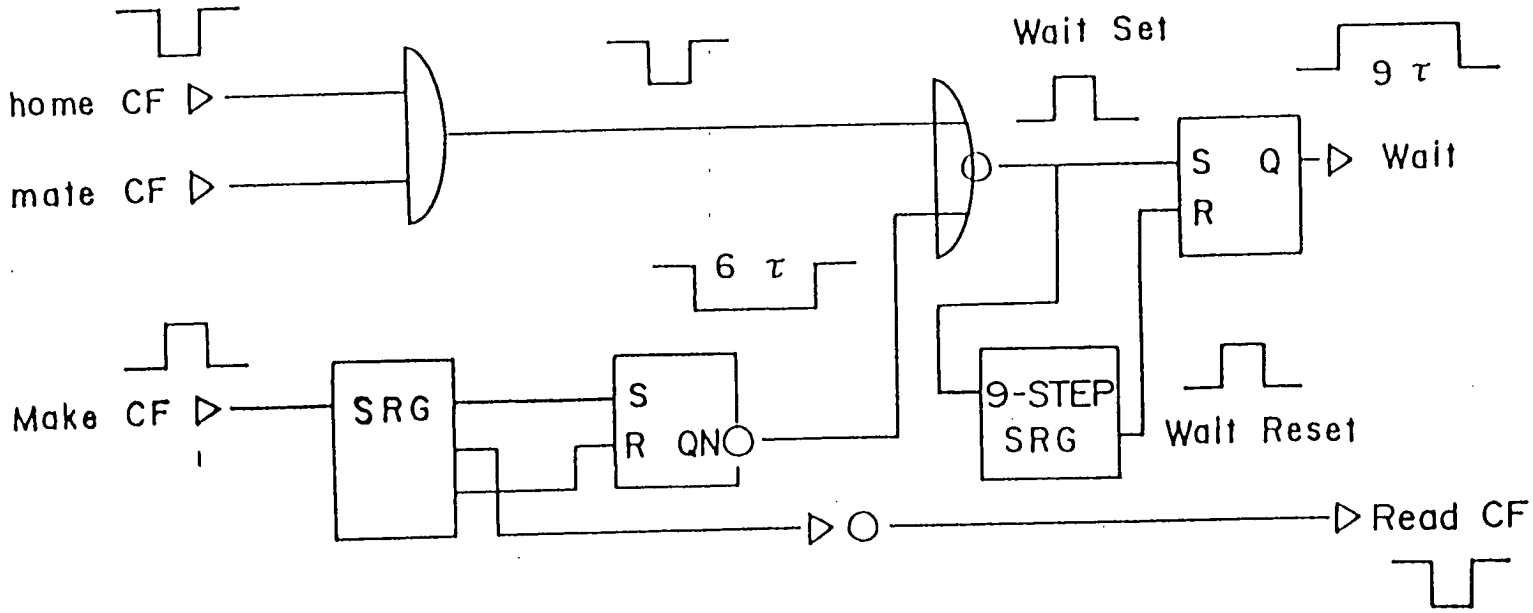

home CF
mate CF
Make CF
SRG
S
R QN
6 τ
Wait Set
9 τ
S Q
R
Wait
9-STEP
SRG
Wait Reset
Read CF

FIG. 306

ITEM	POINT NAME	REMARKS
①	CK39M	DISCONNECTION OF GENERATED 39M CLOCK AND CELL FRAME
②	CK19M	DISCONNECTION OF GENERATED 9M CLOCK AND FRAME PULSE
③	CK9M	DISCONNECTION OF GENERATED 9M CLOCK AND CELL FRAME

FIG. 307

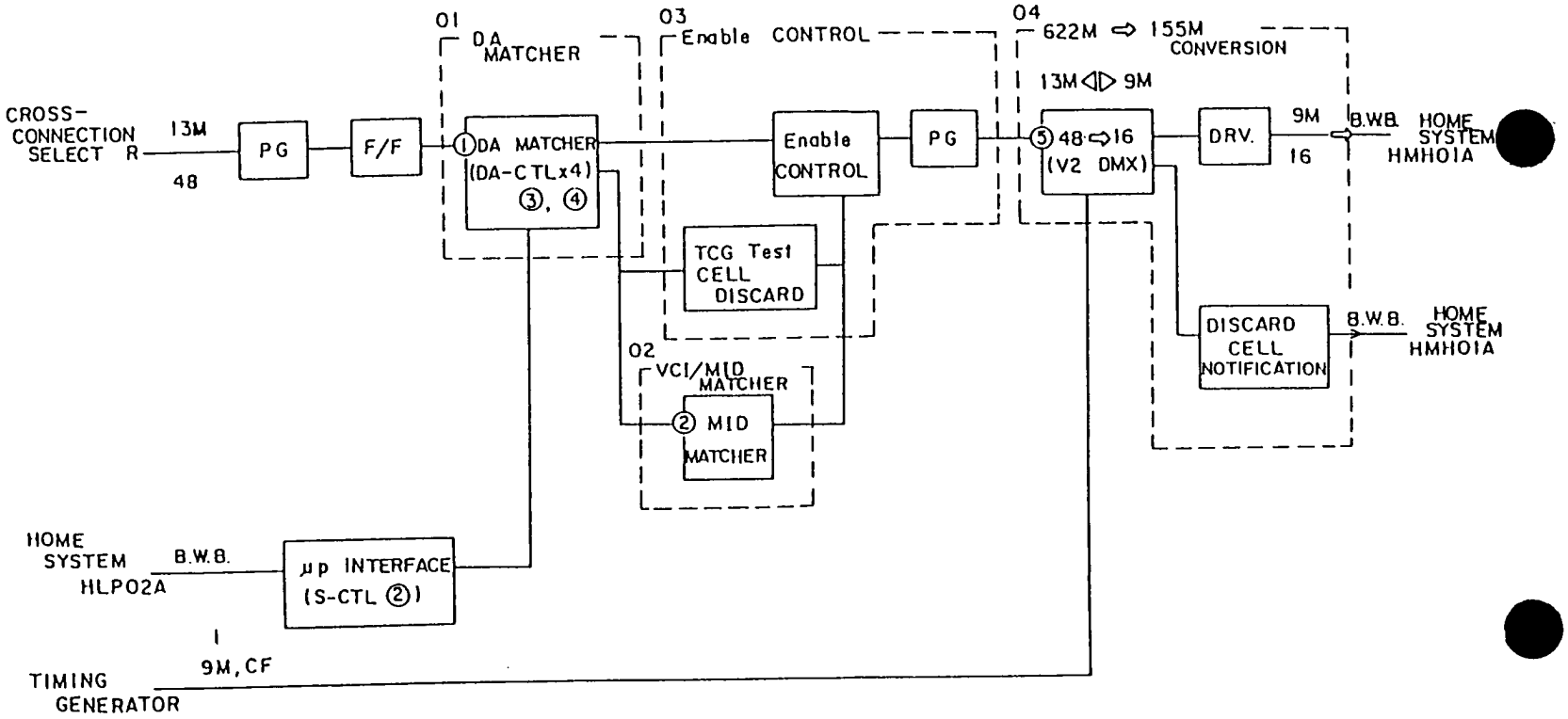

01
DA MATCHER
03
Enable CONTROL
04
622M ⇨ 155M CONVERSION
13M ◁▷ 9M
CROSS-CONNECTION SELECT R
13M
48
PG
F/F
① DA MATCHER (DA-CTLx4) ③, ④
Enable CONTROL
PG
⑤ 48⇨16 (V2 DMX)
DRV.
9M
16
B.W.B.
HOME SYSTEM HMH01A
TCG Test CELL DISCARD
DISCARD CELL NOTIFICATION
B.W.B.
HOME SYSTEM HMH01A
02
VCI/MID MATCHER
② MID MATCHER
HOME SYSTEM HLP02A
B.W.B.
μp INTERFACE (S-CTL ②)
9M, CF
TIMING GENERATOR

FIG. 308

ITEM	FUNCTION BLOCK NAME	REMARKS
01	DA MATCHER	OPERATING MATCHER ON BOM ADN SSM USING DA-CTL LSI AT DESTINATION ADDRESS (DA). WRITING T TAG PORTION DEGENERATED RDA ARISING AT DA FILTER.
02	VCI/MID	OPERATING MATCHER ON COM AND EOM AT VCI/MID.
03	ENABLE CONTROL	OUTPUTTING ONLY MATCHING CELLS TO PROCESSING UNIT ACCORDING TO RESULT OF DA MATCHER AND MID MATCHER.
04	622M⇨155M CONVERSION	CONVERTING SPEED OF 622M (13M, 48 PARALLEL) INTO 155M (9M, 16 PARALLEL) USING V2 DMX LSI.

FIG. 309

OOBT	SEGMENT TYPE		DA-CTL MATCH	READ DATA	WRITE DATA	ENABLE PROCESS	REMARKS
	ST01	ST00					
1	—	—	—	—	—	INVALID	DISCARD
0	0	0	—	0	—	INVALID	DISCARD
	COM						
	0	0	—	1	—	VALID	FETCH
	0	1	—	0	—	INVALID	DISCARD
	EOM						
	0	1	—	1	0	VALID	FETCH AND WRITE "0"
	1	0	0	0	—	INVALID	DISCARD
	BOM						
	1	0	0	1	0	VALID	FETCH AND WRITE "0"
	BOM						
	1	0	1	—	1	VALID	FETCH AND WRITE "1"
	1	1	0	0	—	INVALID	DISCARD
	SSM						
	1	1	0	1	0	VALID	FETCH AND WRITE "0"
	SSM						
	1	1	1	—	0	VALID	FETCH AND WRITE "0"

FIG. 310

ITEM	POINT NAME	REMARKS
①	DACTLP	PARITY CHECK ERROR OF INPUT DATA TO DACTL LSI
②	MIDMEM	PARITY CHECK ERROR BY DATA WRITE/READ IN RAM FOR VCI/MID MATCHER
③	MATADP	DACTL LSI MATCH ADDRESS PARITY ERROR
④	MIDPC	DACTL LSI VCI/ST/MID PARITY ERROR
⑤	OUTPC	PARITY CHECK ERROR OF INPUT DATA TO V2 DMX LSI

FIG. 311

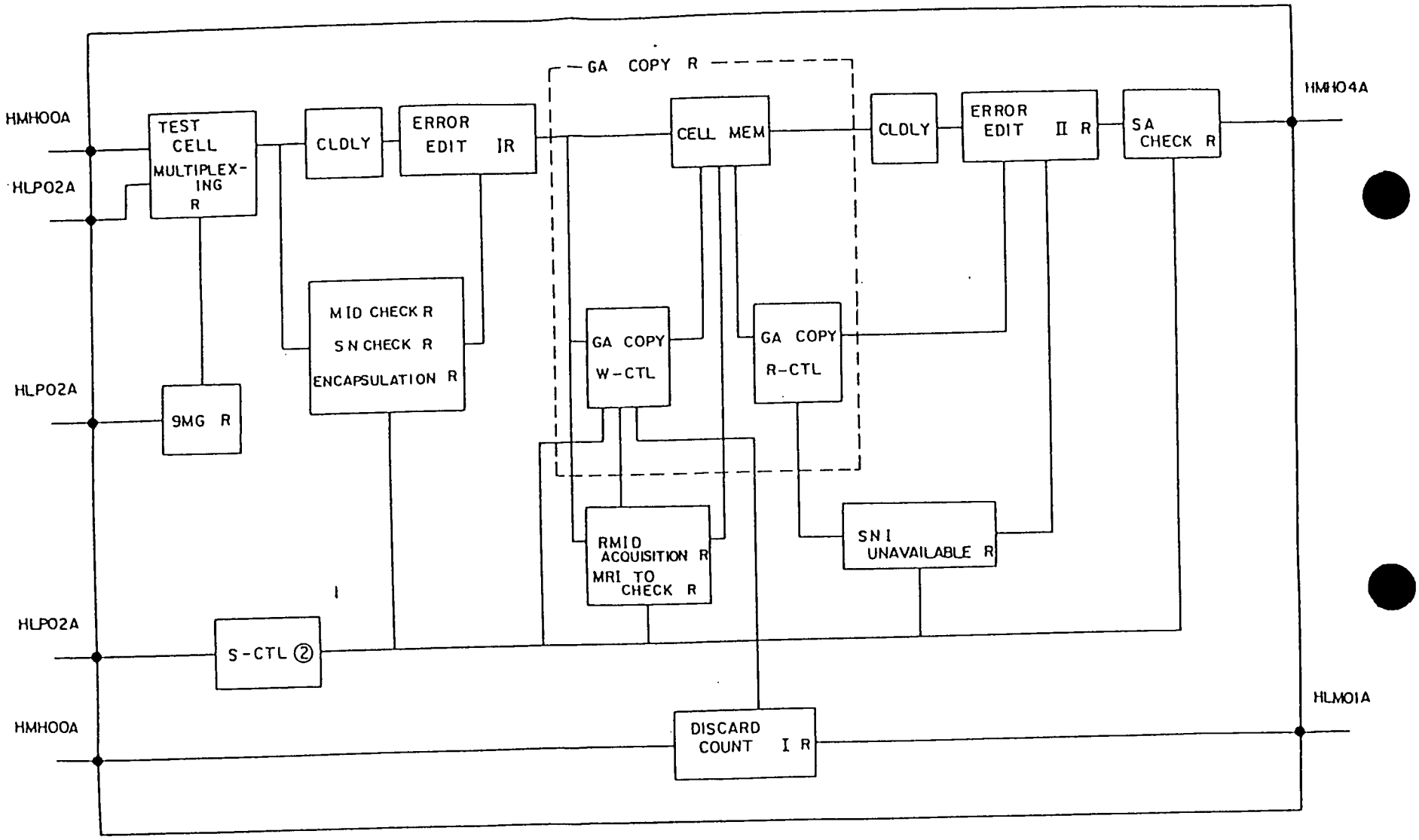

GA COPY R
HMH00A
HLP02A
HLP02A
HLP02A
HMH00A
TEST CELL MULTIPLEX-ING R
CLDLY
ERROR EDIT IR
CELL MEM
CLDLY
ERROR EDIT II R
SA CHECK R
HMH04A
MID CHECK R
SN CHECK R
ENCAPSULATION R
9MG R
GA COPY W-CTL
GA COPY R-CTL
RMID ACQUISITION R
MRI TO CHECK R
SNI UNAVAILABLE R
S-CTL ②
DISCARD COUNT I R
HLM01A

FIG. 312

ITEM	BLOCK NAME	C O N T E N T S
0 1	TEST CELL MULTIPLEX R 9MG R	MULTIPLEXING TEST CELL WHEN LINE CONTAINS IDLE CELLS GENERATING 9MCK USING 19MCK AND FP FROM HLP02A
0 2	MID CHECK R	CHECKING WHETHER OR NOT VCI/MID IS NOT ACTIVE AT BOM AND WHETHER OR NOT VCI/MID IS ACTIVE AT COM AND EOM.
0 3	SN CHECK R	INITIALIZING SN AT BON AND SSM AND CHECKING SEQUENCE IN SN AT COM AND EOM.
0 4	ENCAPSULATION R	FETCHING SIP INF. PDU FROM INTER-MH INF. PDU AND CHANGING SEGMENT TYPE(ST).
0 5	ERROR EDIT I R	ASSIGNING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG
0 6	RMID ACQUISITION R	COMPRESSING MID FOR INTERNAL PROCESS
0 7	MID TIMEOUT CHECK R	DETERMINING MRI TIMEOUT
0 8	GA COPY R	OUTPUTTING CELL INPUT AT GA TO EACH SUBSCRIBER
0 9	SNI AVAILABLE R	DISCARDING CELL AT DT FAULT OF SNI OR OTHER DISABLED RECEPTION
1 0	ERROR EDIT II R	ASSIGNING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG
1 1	SA CHECK R	RETURNING SELF-LOOPBACK CELL IN RESPONSE TO GA MESSAGE
1 2	DISCARD COUNTER IR	COUNTING DISCARDED CELLS AT V2 DMX OF HMH00A AND GA COPY UNIT OF HMH01A

FIG. 313

ITEM	FUNCTION BLOCK NAME	REMARKS
01	TEST CELL RECEPTION	RECEIVING TEST CELL TRANSMITTED BY HLP02A
02	TEST CELL TRANSMISSION CONTROL	MONITORING IDLE CELL IN LINE AND TRANSMITTING RECEIVED TEST CELL. NOTIFYING HLP02A AFTER TRANSMITTING.

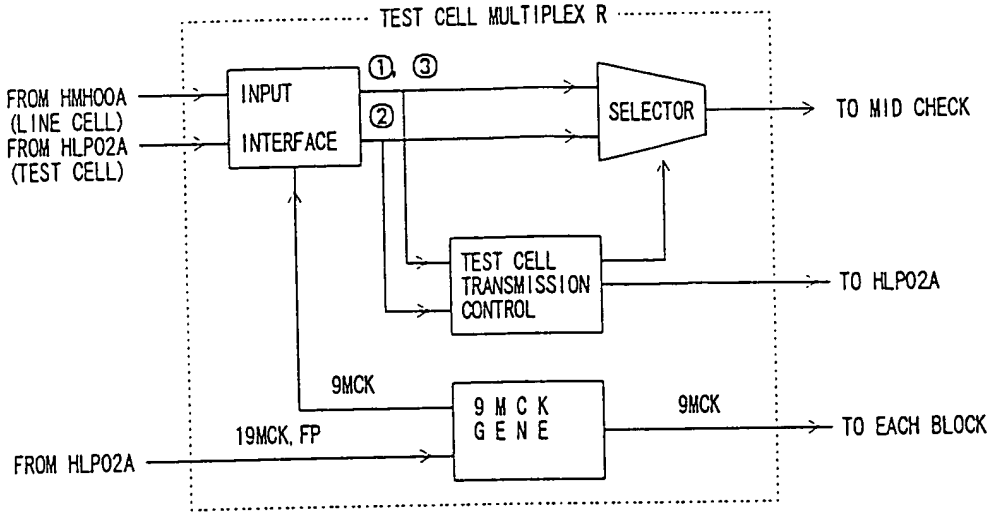


FIG. 314

ITEM	POINT NAME	REMARKS
①	INPC	PARITY CHECK ERROR OF INPUT DATA (LINE CELL) FROM HMH00A
②	TSTPC	PARITY CHECK ERROR OF INPUT DATA (TEST CELL) FROM HMH02A
③	INCF	DISCONNECTION CHECK OF 9MCK GENERATED BASED ON INPUT CELL FRAME FROM HMH00A AND 19MCK AND FP FROM HLP02A

FIG. 315

ITEM	FUNCTION BLOCK NAME	REMARKS
01	ST CHECK	LATCHING SEGMENT TYPE (ST) OF INPUT CELL AND STORING FOR PROCESS FOR EACH ST.
02	MID CHECK	CHECKING THAT VCI/MID IS NOT IN USE AT BOM AND SSM AND THAT VCI/MID IS IN USE AT COM AND EOM.

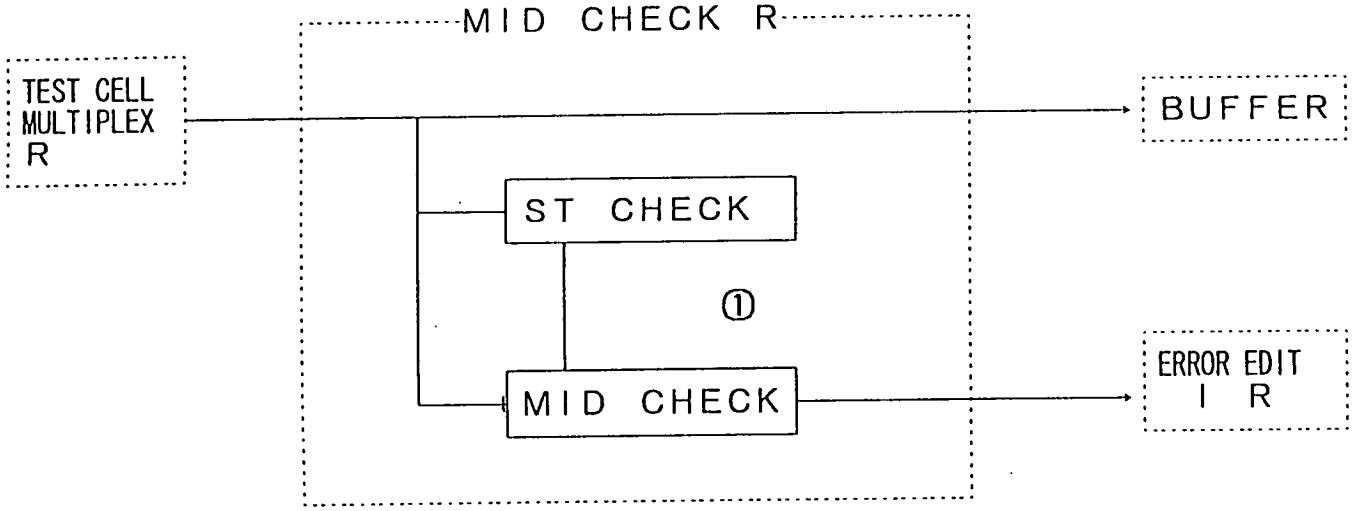


FIG. 316

SEGMENT TYPE	DM	RAM INFORMATION(READ)	PROCESS
INTER-MH BOM	MATCH	ACT	SETTING IN ACT STATE
INTER-MH BOM	UNMATCH	ACT	RELEASING
INTER-MH BOM	MATCH	NOT ACT	SETTING IN ACT STATE
INTER-MH BOM	UNMATCH	NOT ACT	RELEASING
INTER-MH SSM	MATCH	ACT	RELEASING
INTER-MH SSM	UNMATCH	ACT	RELEASING
INTER-MH SSM	MATCH	NOT ACT	RELEASING
INTER-MH SSM	UNMATCH	NOT ACT	RELEASING
INTER-MH COM	D.C.	ACT	SETTING IN ACT STATE
INTER-MH COM	D.C.	NOT ACT	RELEASING
INTER-MH EOM	D.C.	ACT	RELEASING
INTER-MH EOM	D.C.	NOT ACT	RELEASING

FIG. 317

Segment Type	error	DM	Error Flag	
Inter-MH BOM	VCI/MID Is Active	0	EF1	EFMS(Master Error Flag)
			EF2	EFMA(MID Active Error)
		1	EF2	EFMA(MID Active Error)
Inter-MH SSM	VCI/MID Is Active	0	EF1	EFMS(Master Error Flag)
			EF2	EFMA(MID Active Error)
		1	EF2	EFMA(MID Active Error)
Inter-MH COM	VCI/MID Is Not Active	EF1	EF1	EFMC(COM MID Active Error) EFMS(Master Error Flag)
Inter-MH EOM	VCI/MID Is Not Active	EF1	EF1	EFMC(COM MID Active Error) EFMS(Master Error Flag)

FIG. 318

ITEM	POINT NAME	address	bit	REMARKS
①	SNMEM	0210	06	SN check memory parity NG

FIG. 319

ITEM	FUNCTION BLOCK NAME	REMARKS
01	SN+1	ADDING 1 TO SEQUENCE NUMBER(SN)
02	SN CHECK	STORING SN+1 WHEN BOM ARRIVES. COMPARING LATCHED SN WITH STORED SN WHEN COM ARRIVES TO CHECK WHETHER OR NOT THEY MATCH (SEQUENTIAL). EOM AND COM PERFORM SIMILAR PROCESSES. SSM IS NOT OBJECT OF CHECK.

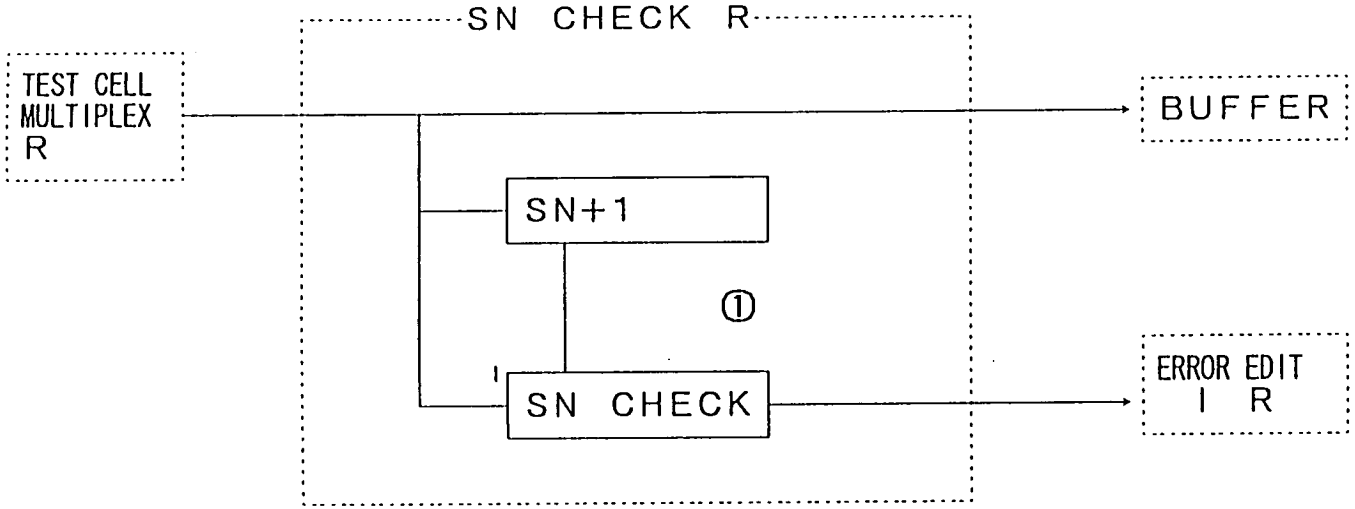


FIG. 320

Segment Type	error	Error Flag	
Inter-MH COM	DIFFERENT SEQUENCES	EF1	EFMS(Master Error Flag)
		EF2	EFSN(Invalid Sequence Number)
Inter-MH EOM	DIFFERENT SEQUENCES	EF1	EFMS(Master Error Flag)
		EF2	EFSN(Invalid Sequence Number)

FIG. 321

ITEM	POINT NAME	address	bit	REMARKS
①	SNMEM	0210	06	SN check memory parity NG

FIG. 322

ITEM	FUNCTION BLOCK NAME	REMARKS
01	SN CHECK	LATCHING SEGMENT TYPE(ST) OF INPUT CELL AND STORING IT FOR USE IN PROCESS OF EACH ST.
02	ENCAPSULATION	CHANGING INTO BOM IF COM IS NEXT TO BOM, AND INTO SSM IF EOM IS NEXT TO BOM.

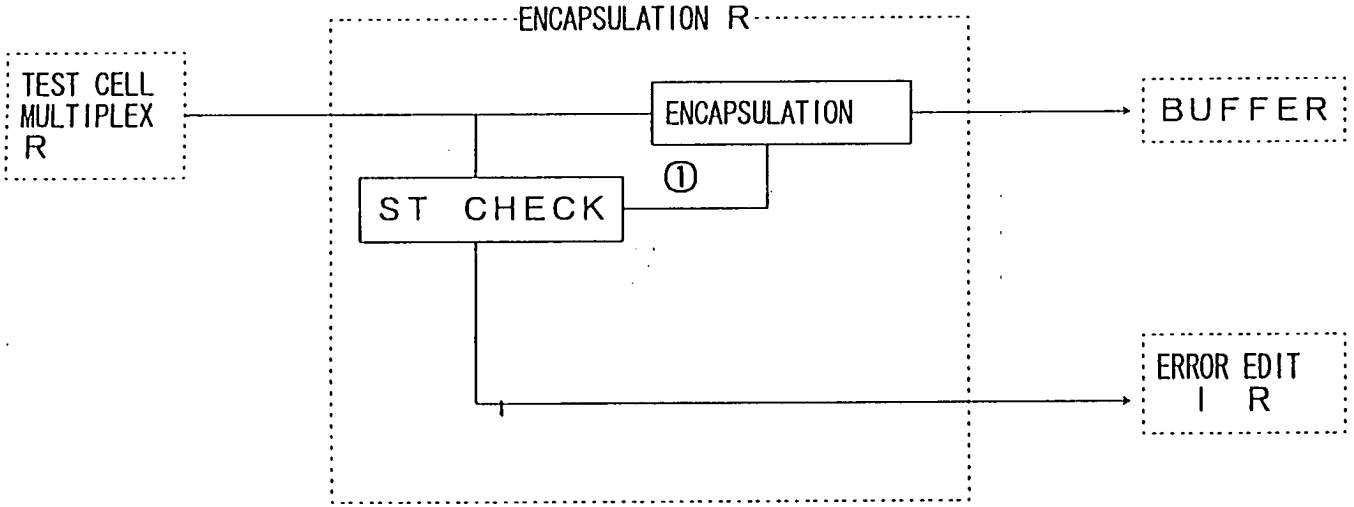


FIG. 323

Segment Type	error	Error Flag	
Inter-MH SSM	UNCONDITIONAL ERROR	EF1	EFMS(Master Error Flag)
		EF2	EFEN(Encapsulation Error)

FIG. 324

ITEM	POINT NAME	address	bit	REMARKS
①	SNMEM	0210	06	SN check memory parity NG

FIG. 325

ITEM	FUNCTION BLOCK NAME	REMARKS
01	DEFINING ERROR	ASSIGNING ERROR INFORMATION OF EACH CHECKER TO POSITION OF EACH ERROR FLAG.

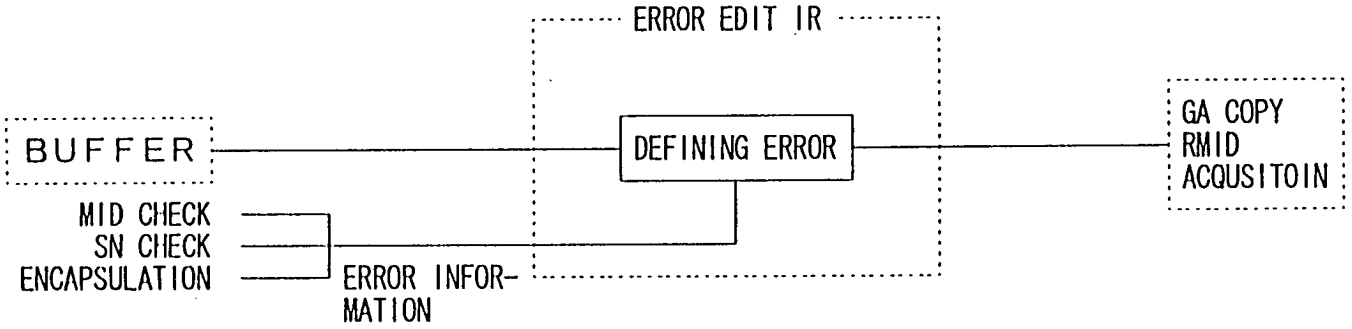


FIG. 326

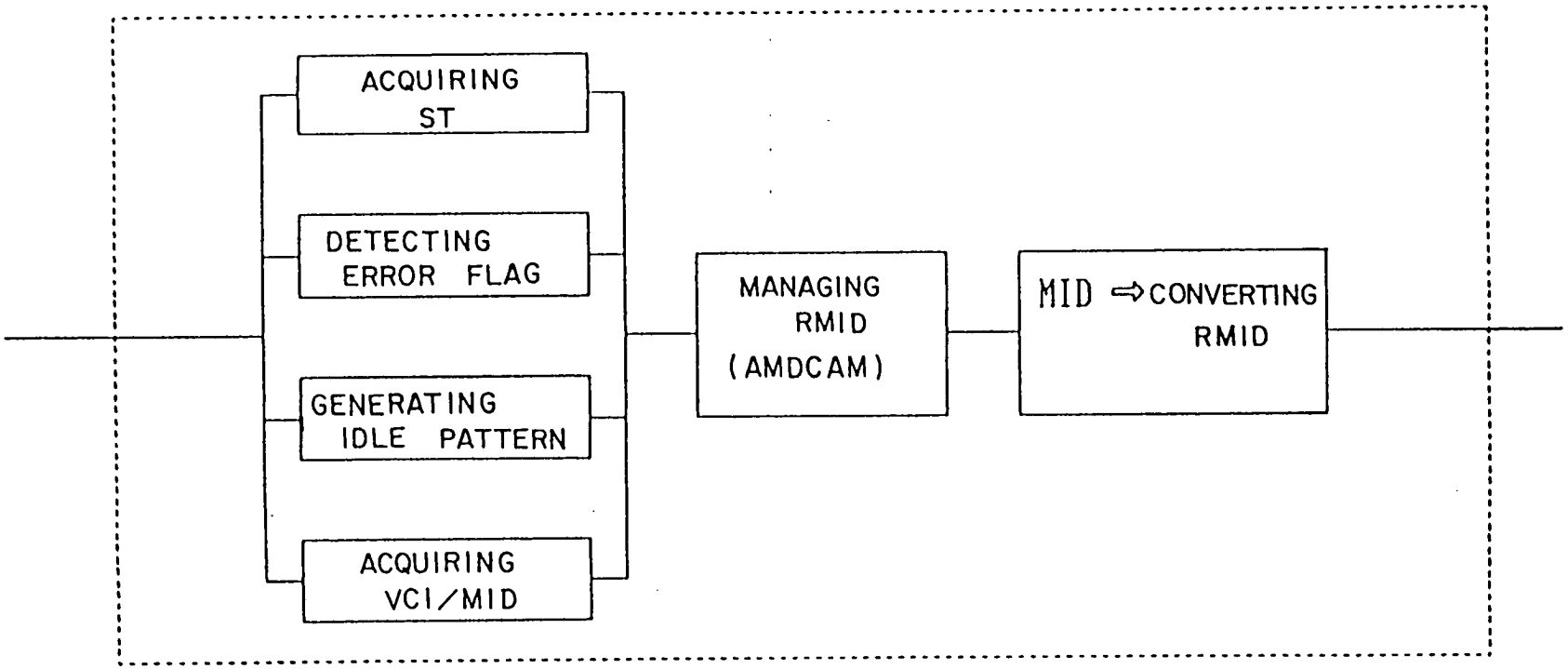

ACQUIRING ST
DETECTING ERROR FLAG
GENERATING IDLE PATTERN
ACQUIRING VCI/MID
MANAGING RMID (AMDCAM)
MID ⇨ CONVERTING RMID

FIG. 327

ITEM	FUNCTION BLOCK NAME	REMARKS
01	ACQUIRING ST	FETCHING ST OF VALID CELL AND DETERMINING ST.
02	GENERATING IDLE PATTERN	TRANSMITTING IDLE PATTERN (ALL 1) TO AMD-CAM AS INITIALIZATION
03	ACQUIRING VCI/MID	ACQUIRING VCI/MID OF VALID CELL AND TRANSMITTING IT TO RMID MANAGEMENT
04	MANAGING RMID (AMD-CAM)	DETERMINING WHETHER OR NOT ACQUIRED VCI/MID MATCH IF MATCHING, MATCH ADDRESS SIGNAL IS OUTPUT
05	CONVERTING RMID ⇨ MID	OVERWRITING MATCH ADDRESS SIGNAL (RMID) OUTPUT AT AMD-CAM ON MID OF CELL

FIG. 328

SEGMENT TYPE	E R R O R	ERROR FLAG	
INTER-MH BOM	WHEN RMID CANNOT BE ACQUIRED	EF1	EFMS(MASTER ERROR FLAG)
		EF2	EFMN(RMID ASSIGNED ERROR)
INTER-MH SSM	WHEN RMID CANNOT BE ACQUIRED	EF1	EFMS(MASTER ERROR FLAG)
		EF2	EFMN(RMID ASSIGNED ERROR)
INTER-MH COM	WHEN RMID IS NOT ACQUIRED PREVIOUSLY, AND IS RELEASED	EF1	EFMD(RMID ACTIVE ERROR) EFMS(MASTER ERROR FLAG)
INTER-MH EOM	WHEN RMID IS NOT ACQUIRED PREVIOUSLY, AND IS RELEASED	EF1	EFMD(RMID ACTIVE ERROR) EFMS(MASTER ERROR FLAG)

FIG. 329

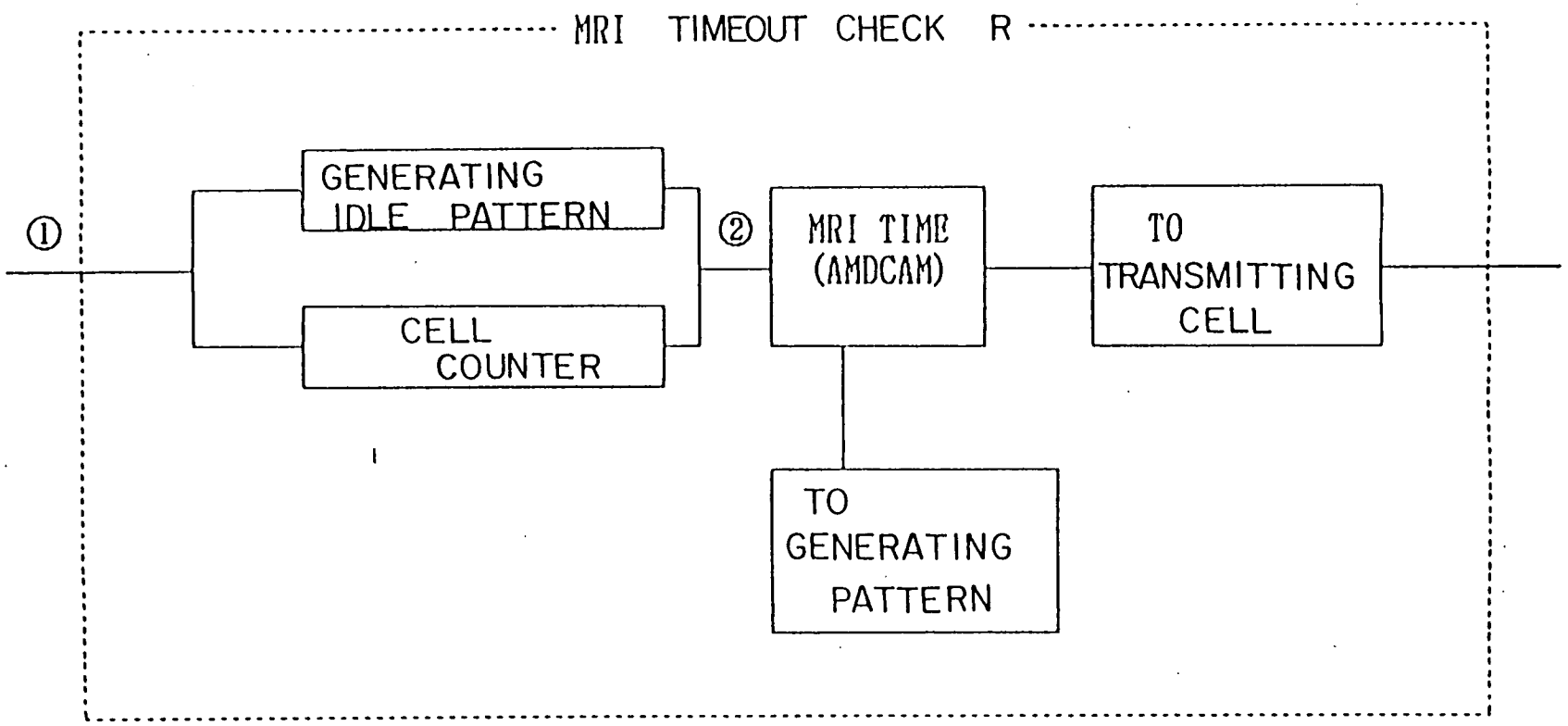

MRI TIMEOUT CHECK R
①
GENERATING IDLE PATTERN
CELL COUNTER
②
MRI TIME (AMDCAM)
TO TRANSMITTING CELL
TO GENERATING PATTERN

FIG. 330

ITEM	FUNCTION BLOCK NAME	REMARKS
01	CELL ST DETERMINATION (CONCURRENT WITH MID COMPRESSION)	FETCHING ST OF VALID CELL AND DETERMINING ST.
02	CELL COUNTER	CELL COUNTER HAVING MODE IN WHICH CELLS ARE COUNTED EACH TIME ALL CELLS ARRIVE AND HAVING MODE IN WHICH ONLY VALID CELLS ARE COUNTED
03	GENERATING IDLE PATTERN (CONCURRENT WITH MID COMPRESSION)	INITIALIZING MRI TIME (AMD-CAM) TRANSMITTING IDLE PATTERN FOR BOM
04	MRI TIME(AMDCAM)	CHECKING FOR TIMEOUT FOR EACH CELL
05	TO GENERATING PATTERN	OUTPUTTING TO PATTERN TO MRI TIME (AMD-CAM) AT TIMEOUT
06	TO TRANSMITTING CELL	OUTPUTTING TO CELL INSTEAD OF EOM OF TIMEOUT MESSAGE

FIG. 331

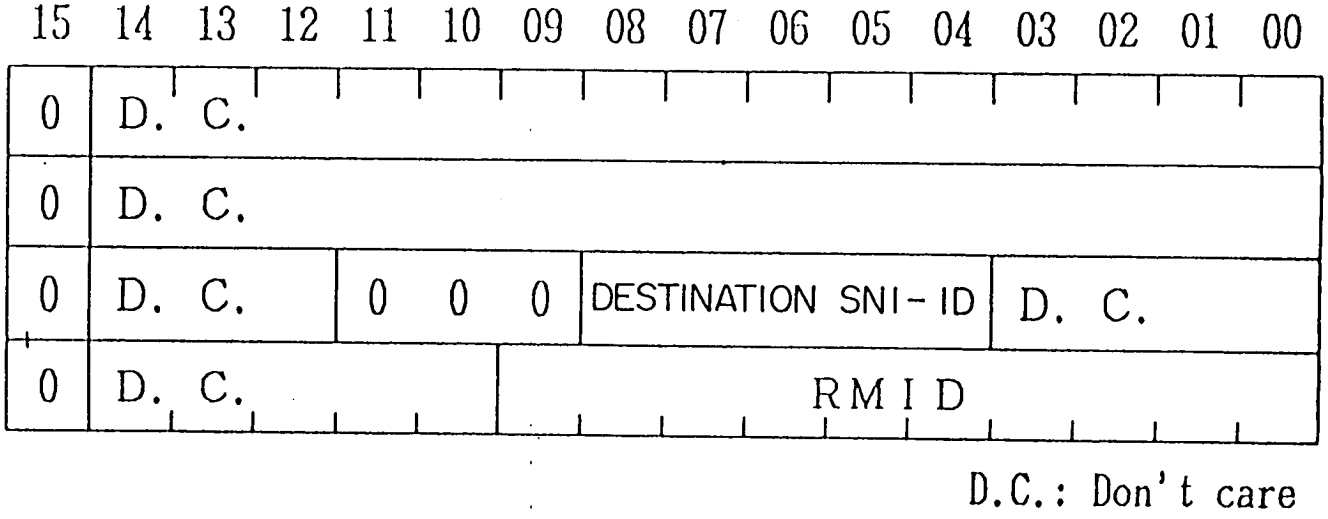

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
0 D. C.
0 D. C.
0 D. C. 0 0 0 DESTINATION SNI-ID D. C.
0 D. C. RMID
D.C.: Don't care

FIG. 332

Segment Type	error	Error Flag	
Inter MII COM	IEOM DOES NOT ARRIVE WITHIN 177MS AFTER IBOM ARRIVED	EF1	EFMS(Master Error Flag)
		EF2	EFMT(MRI time out)
Inter MII COM Inter MII EOM	CELL ARRIVED AFTER TO CELL IS TRANSMITTED	EF1	EFMD(RMID Active Error) EFMS(Master Error Flag)

FIG. 333

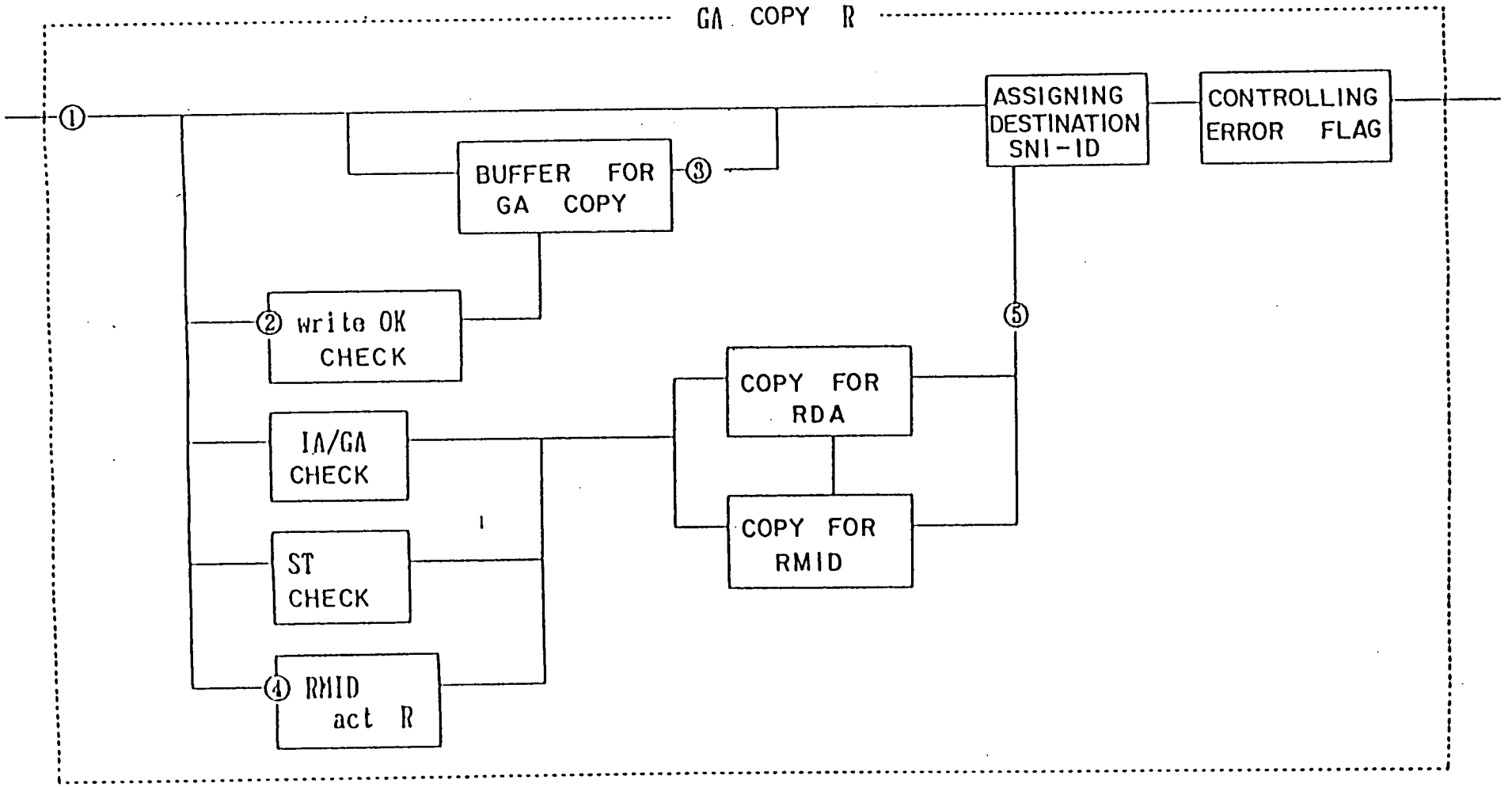

GA COPY R
①
ASSIGNING DESTINATION SNI-ID
CONTROLLING ERROR FLAG
BUFFER FOR GA COPY
③
② write OK CHECK
⑤
COPY FOR RDA
IA/GA CHECK
COPY FOR RMID
ST CHECK
④ RMID act R

FIG. 334

ITEM	FUNCTION BLOCK NAME	REMARKS
01	WRITE OK CHECK	READING WRITE O.K.R TABLE ACCORDING TO VCI/MID AND DETERMINING WHETHER OR NOT DATA CAN BE WRITTEN TO BUFFER FOR GA COPY. IF BUFFER IS FULL (NOT WRITABLE), DISCARD SIGNAL IS TRANSMITTED TO DISCARD COUNT.
02	BUFFER FOR GA COPY	BUFFER IN WHICH CELLS ARE WRITTEN TO MAKE COPIES AT GA COPY.
03	RMID ACT R	STORING FOR EACH RMID, INFORMATION ABOUT WHETHER OR NOT PRESENTLY RECEIVED MESSAGE IS BEING GA COPIED.
04	IA/GA CHECK	DETERMINING WHETHER RDA OF EACH MESSAGE IS IA OR GA.
05	ST CHECK	LATCHING SIP SEGMENT TYPE(SST) OF INPUT CELL AND STORING IT TO PROCESS IT FOR EACH ST.
06	COPY FOR RDA	IF RDA IS GA IN IBOM, COPIED-TO SNI IS DETERMINED FROM GA COPY R TABLE USING ADDRESS OF RDA AND COPIED CELL IS TRANSMITTED.
07	COPY FOR RMID	IF RDA OF ICOM AND IEOM IS GA, COPIED-TO SNI IS DETERMINED FROM MESSAGE COPY TABLE USING ADDRESS OF RMID AND COPIED CELL IS TRANSMITTED.
07	ASSIGNING DESTINATION SNI-ID	ASSIGNING DESTINATION SNI-ID TO TRANSMITTED CELL. IF RDA IS IA, IT IS OBTAINED DIRECTLY FROM RDA. IF RDA IS GA, IT IS OBTAINED FROM COPY TABLE.
09	CONTROLLING ERROR FLAG	IF EFMS(MASTER ERROR FLAG) OF CELL IS SET "ON" AND CELL IS COPIED, ERROR FLAG AT EF2 IS MASKED TO PREVENT DOUBLE COUNT AT TM PORTION OF HLM01A.

FIG. 335

0350242

Segment Type	error	Error Flag	
Inter MII BOM	IEOM HAS NOT ARRIVED AND IBOM HAVING SAME RMID ARRIVES	EF1	EFMS(Master Error Flag)
			EFGA(GA Active Error)
Inter MII BOM' Inter MII COM Inter MII EOM	EFMS (MASTER ERROR FLAG) OF CELL IS SET "ON" AND CELL IS COPIED	EF1	EFGA(GA Active Error)

FIG. 336

ITEM	POINT NAME	REMARKS
①	GACOPY	GA COPY INPUT UNIT LINE ERROR
②	WOKMEM	Write OK memory Parity Check Error
③	GAMEM	GA copy cell memory Parity Check Error
④	GAACTP	GA ACT Parity Check Error
⑤	GACPPC	GA copy bit map Parity Check Error

FIG. 337

ITEM	FUNCTION BLOCK NAME	REMARKS
01	SNI BLOCK INFORMATION	SUPPRESSING TRANSMISSION OF MESSAGE TO SNI ACCORDING TO BLOCK INFORMATION.

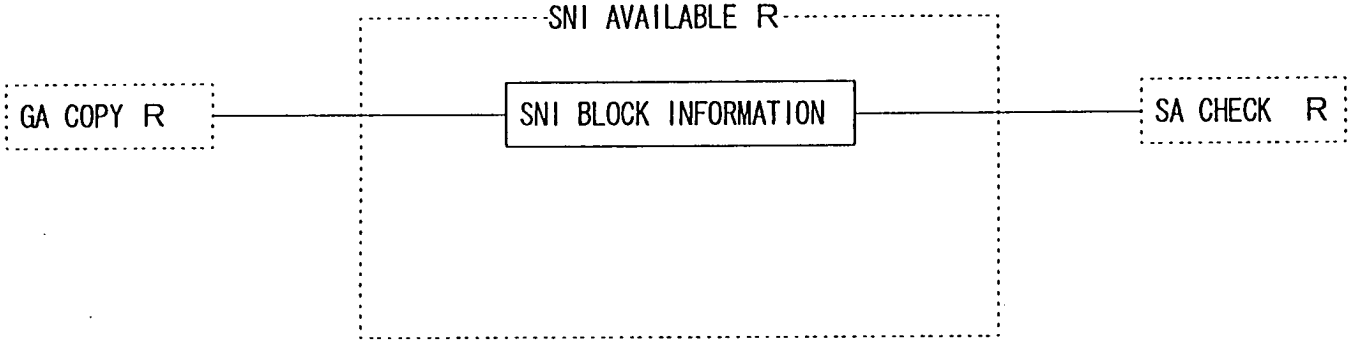


FIG. 338

Segment Type	error	Error Flag	
Inter-MH BOM	not Available	EF1	EFMS(Master Error Flag)
		EF2	EFDA(Destination SNI not Available)
Inter-MH SSM	not Available	EF1	EFMS(Master Error Flag)
		EF2	EFDA(Destination SNI not Available)

FIG. 339

ITEM	POINT NAME	REMARKS
①	AVPC	SNI AVAILABLE PARITY CHECK ERROR
②	BRLCPC	BRLC NUMBER PARITY CHECK ERROR

FIG. 340

ITEM	FUNCTION BLOCK NAME	REMARKS
01	DEFINING ERROR	ASSIGNING ERROR INFORMATION OF EACH CHECKER TO POSITION OF EACH ERROR FLAG.

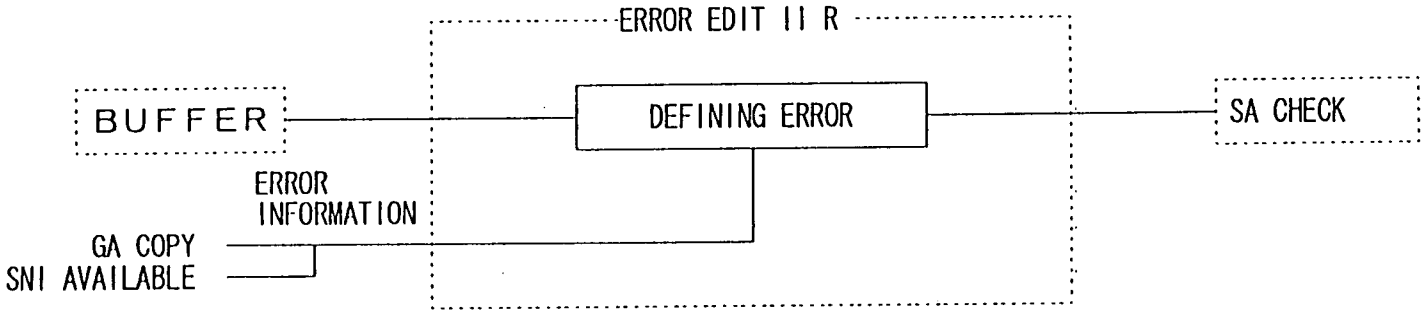


FIG. 341

ITEM	FUNCTION BLOCK NAME	REMARKS
01	SA CHECK	RETURNING LOOPBACK CELL RECEIVED FROM ENTERED SA

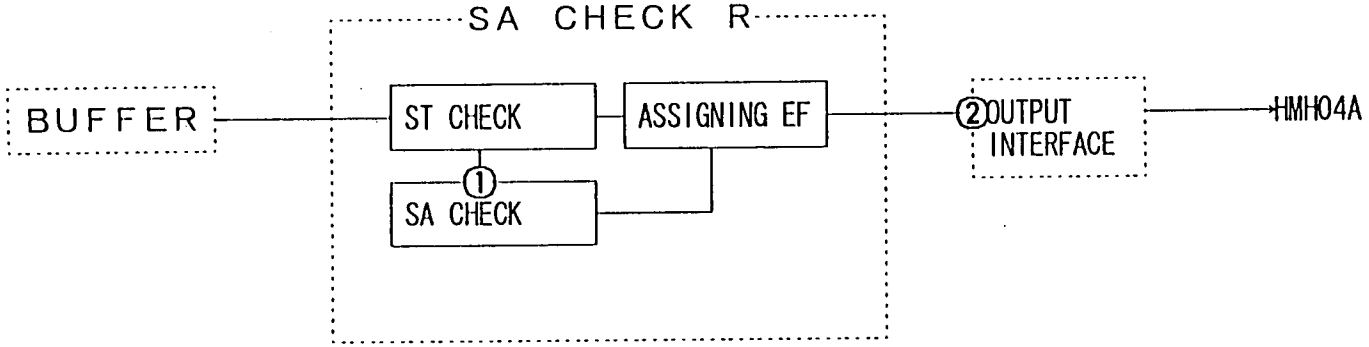


FIG. 342

Segment Type	error	Error Flag	
Inter-MH BOM	SELF-LOOPBACK CELL	EF1	EFMS(Master Error Flag)
		EF2	EFDO(Destination equal to Org.SNI)
Inter-MH SSM	SELF-LOOPBACK CELL	EF1	EFMS(Master Error Flag)
		EF2	EFDO(Destination equal to Org.SNI)

NOTE: INTER-MH COM AND INTER-MH COM ARE D.C.
NOT OBJECT OF CHECK IF HIGHEST ORDER BIT OF DESTINATION SNI-ID IS 1
NOT OBJECT OF CHECK IF EFMS OF CELL HAS ALREADY BEEN SET "ON"

FIG. 343

ITEM	POINT NAME	REMARKS
①	SAMADP	PARITY CHECK ERROR OF SA CHECK MATCH ADDRESS
②	OUTPC	HMH01A EXIT PARITY CHECK ERROR

FIG. 344

SC ATTRIBUTE	WHEN MATCHING AT CAM	WHEN NON-MATCHING AT CAM
1	ERROR (UNACCEPTABLE AT ENTERD ADDRESS)	TRANSMISSION ENABLED
2	TRANSMISSION ENABLED	ERROR (UNACCEPTABLE AT ADDERSS OTHER THEN ENTERED ADDRESS)

FIG. 345

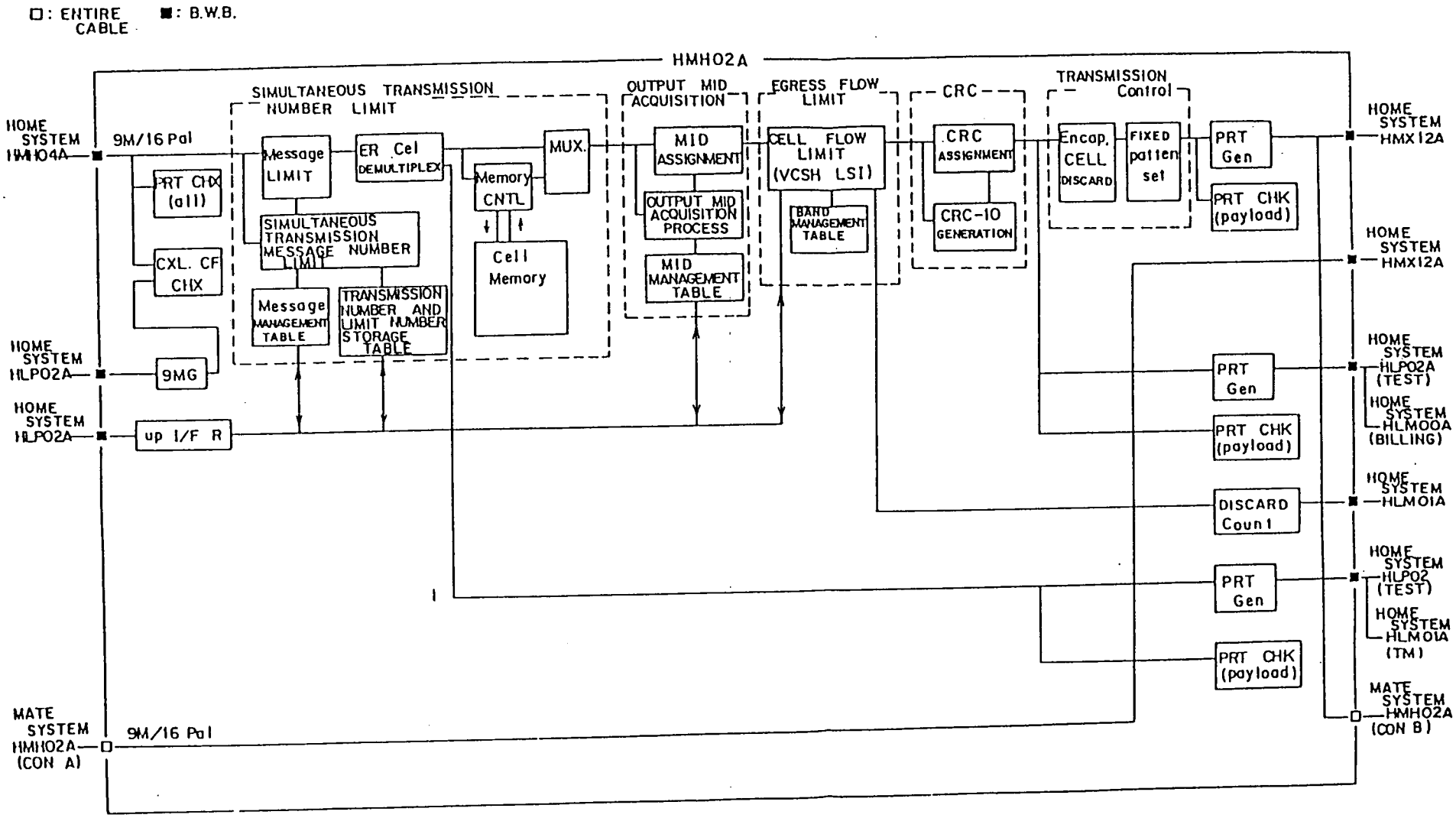

□: ENTIRE CABLE
■: B.W.B.
HMH02A
HOME SYSTEM HMH04A
9M/16 Pal
SIMULTANEOUS TRANSMISSION NUMBER LIMIT
Message LIMIT
ER Cel DEMULTIPLEX
Memory CNTL
MUX.
Cell Memory
PRT CHK (all)
CXL. CF CHK
SIMULTANEOUS TRANSMISSION MESSAGE NUMBER LIMIT
Message MANAGEMENT TABLE
TRANSMISSION NUMBER AND LIMIT NUMBER STORAGE TABLE
OUTPUT MID ACQUISITION
MID ASSIGNMENT
OUTPUT MID ACQUISITION PROCESS
MID MANAGEMENT TABLE
EGRESS FLOW LIMIT
CELL FLOW LIMIT (VCSH LSI)
BAND MANAGEMENT TABLE
CRC
CRC ASSIGNMENT
CRC-10 GENERATION
TRANSMISSION Control
Encap, CELL DISCARD
FIXED pattern set
PRT Gen
PRT CHK (payload)
HOME SYSTEM HMX12A
HOME SYSTEM HMX12A
HOME SYSTEM HLP02A
9MG
HOME SYSTEM HLP02A
up I/F R
PRT Gen
PRT CHK (payload)
HOME SYSTEM HLP02A (TEST)
HOME SYSTEM HLM00A (BILLING)
DISCARD Count
HOME SYSTEM HLM01A
PRT Gen
PRT CHK (payload)
HOME SYSTEM HLP02 (TEST)
HOME SYSTEM HLM01A (TM)
MATE SYSTEM HMH02A (CON A)
9M/16 Pal
MATE SYSTEM HMH02A (CON B)

FIG. 346

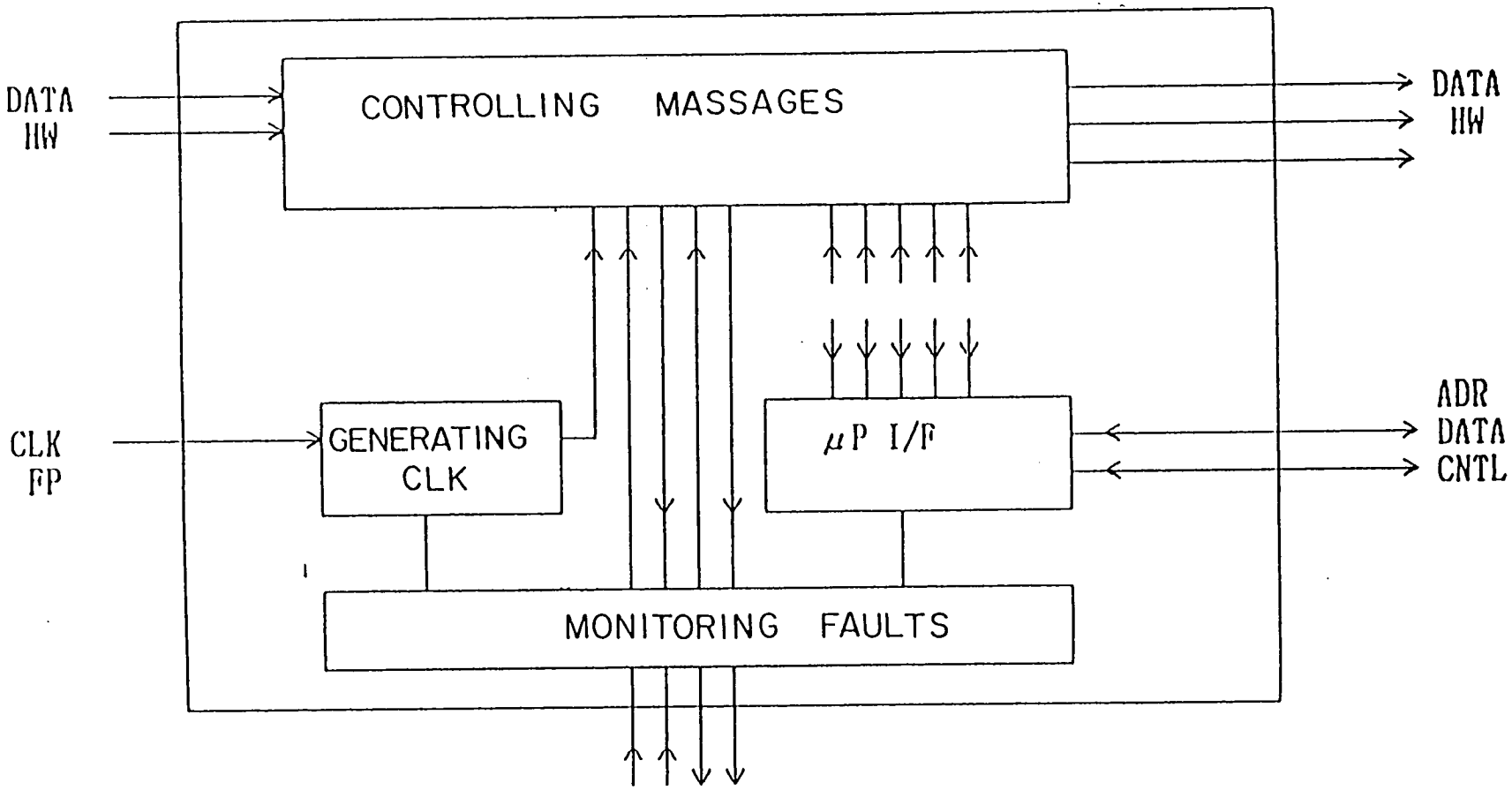

DATA
HW
CONTROLLING MASSAGES
DATA
HW
CLK
FP
GENERATING
CLK
μP I/F
ADR
DATA
CNTL
MONITORING FAULTS

FIG. 347

ITEM	FUNCTION	REMARKS
01	CONTROLLING MESSAGE	TRANSMISSION LIMIT OF MESSAGE AND BAND CONTROL
02	μP I/F	RECEIVING VARIOUS CONTROL SIGNAL TRANSMITTED FROM μP AND DATA, AND INTERNAL CONTROL
03	GENERATING CLK	GENERATING 9MHz. CLK BASED ON RECEIVED 19MHz. CLK
04	MONITORING FAULTS	MONITORING FAULT MONITOR OBJECT POINT IN PWCB

FIG. 348

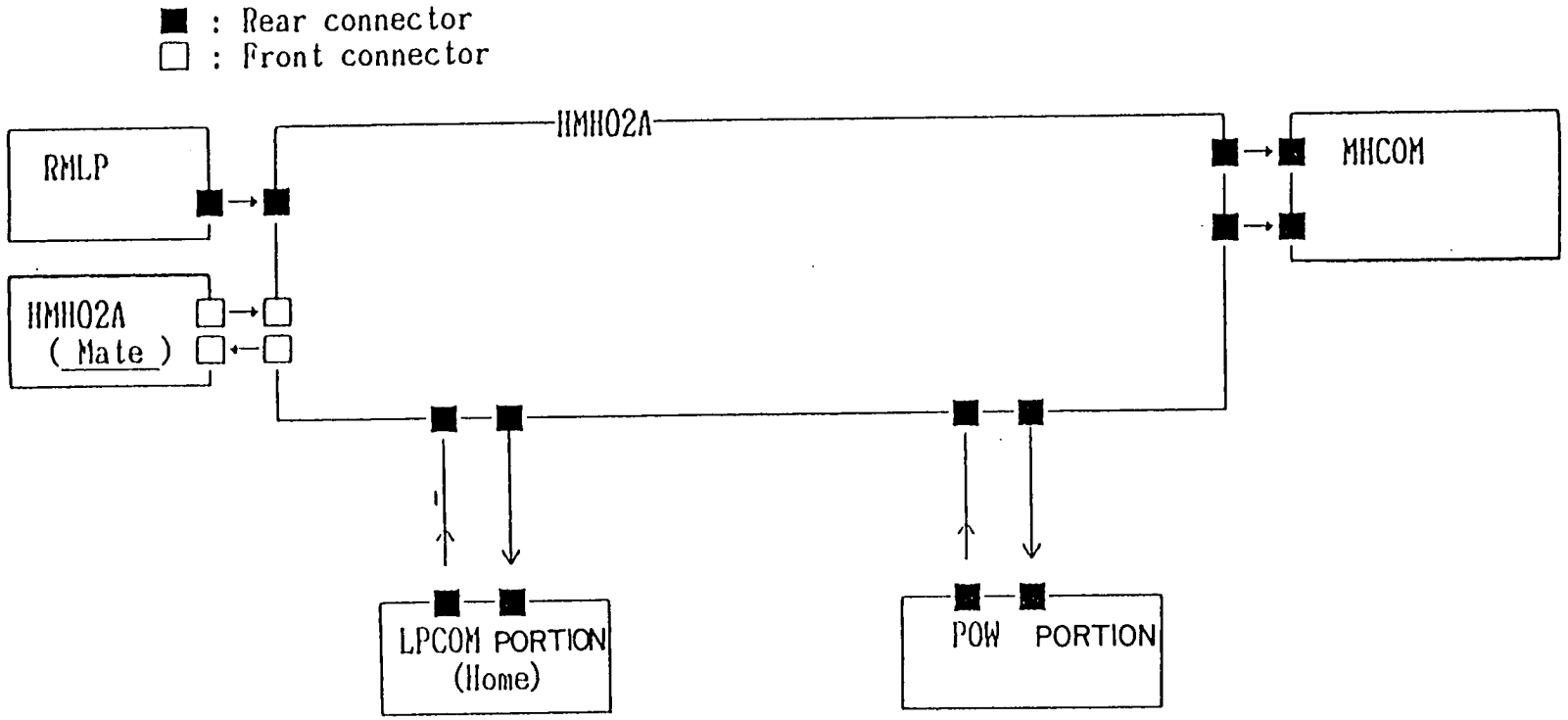

■ : Rear connector
□ : Front connector
RMLP
HMH02A
HMH02A
(Mate)
HMH02A
MHCOM
LPCOM PORTION
(Home)
POW PORTION

FIG. 349

ITEM	FUNCTION	
01	SIMULTANEOUS TRANSMISSION LIMIT	LIMITING NUMBER OF MESSAGES FOR EACH SNI
02	OUTPUT MID ACQUISITION	CONVERTING RMID (COMPRESSED MID) INTO OUTPUT MID
03	EGRESS FLOW LIMIT	LIMITING OUTPUT BAND (PEAK RATE) FOR EACH SNI
04	DISCARD COUNTER	COUNTING AND STORING CELLS AND MESSAGES DISCARD AT EGRESS FLOW LIMITING UNIT
05	CRC-10 GENERATION	GENERATING AND ASSIGNING CRC-10 OF CELL PAYLOAD
06	TRANSMISSION CONTROL	MANIPULATING HEADER PATTERN FOR SPECIFIED CELL AND RELEASING ENCAPSULATION
07	INTER-SYSTEM CROSS-CONNECTION	FETCHING HW DATA FROM HMH02A OF MATE SYSTEM AND TRANSMITTING DATA TO MDX UNIT OF HOME SYSTEM

FIG. 350

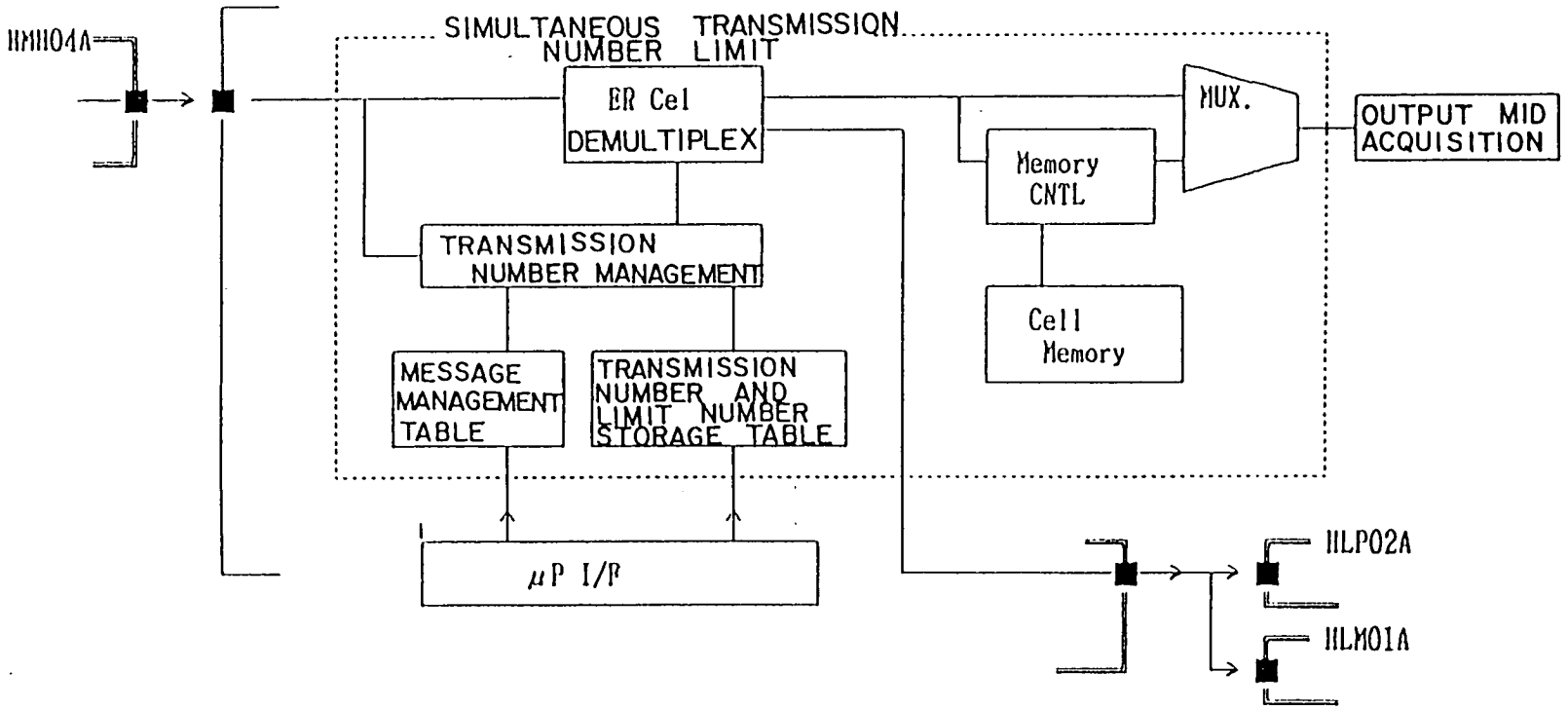

HMH04A
SIMULTANEOUS TRANSMISSION NUMBER LIMIT
ER Cel DEMULTIPLEX
MUX.
OUTPUT MID ACQUISITION
Memory CNTL
Cell Memory
TRANSMISSION NUMBER MANAGEMENT
MESSAGE MANAGEMENT TABLE
TRANSMISSION NUMBER AND LIMIT NUMBER STORAGE TABLE
μP I/F
HLP02A
HLM01A

FIG. 351

LIMIT NUMBER	TRANSMISSION NUMBER : LIMIT NUMBER	
1	NUMBER OF MESSAGES = 0	MESSAGE TRANSMISSION ENABLED
	NUMBER OF MESSAGES = 1	NEXT MESSAGE IS BUFFERED AND SUBSEQUENT MESSAGES CANNOT BE TRANSMITTED
16	16 > NUMBER OF MESSAGES	MESSAGE TRANSMISSION ENABLED
	NUMBER OF MESSAGES = 16	NEXT MESSAGE IS BUFFERED AND SUBSEQUENT MESSAGES CANNOT BE TRANSMITTED

FIG. 352

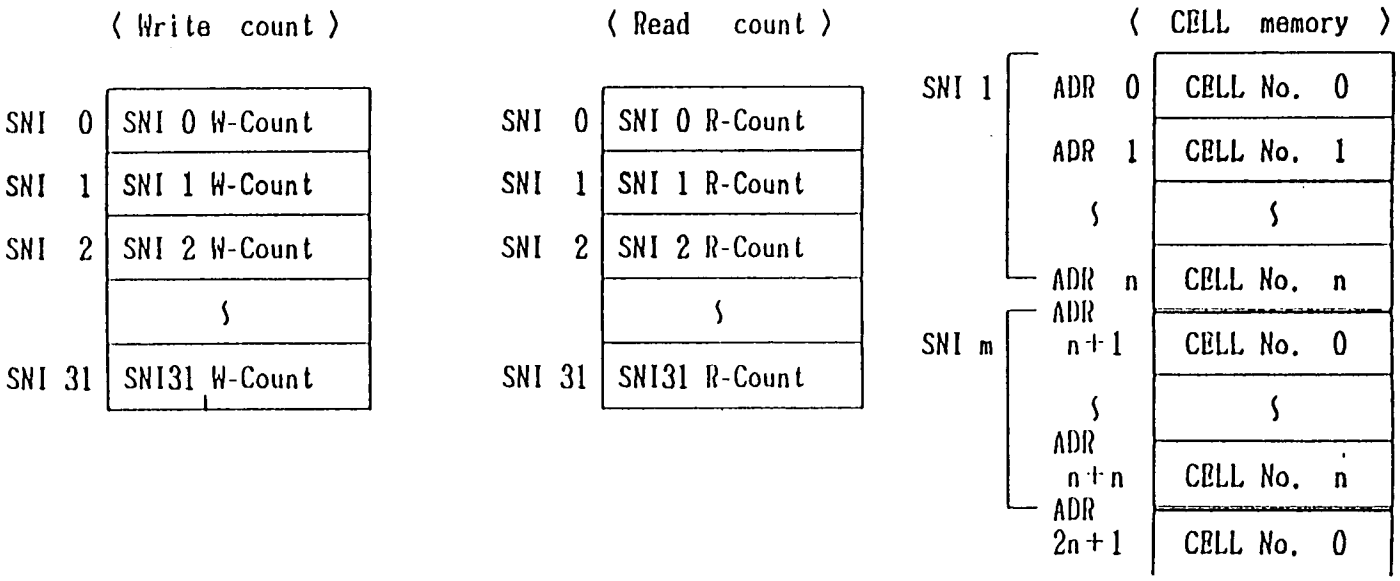

〈 Write count 〉
SNI 0
SNI 0 W-Count
SNI 1
SNI 1 W-Count
SNI 2
SNI 2 W-Count
SNI 31
SNI31 W-Count
〈 Read count 〉
SNI 0
SNI 0 R-Count
SNI 1
SNI 1 R-Count
SNI 2
SNI 2 R-Count
SNI 31
SNI31 R-Count
〈 CELL memory 〉
SNI 1
ADR 0
CELL No. 0
ADR 1
CELL No. 1
ADR n
CELL No. n
SNI m
ADR n+1
CELL No. 0
ADR n+n
CELL No. n
ADR 2n+1
CELL No. 0

FIG. 353

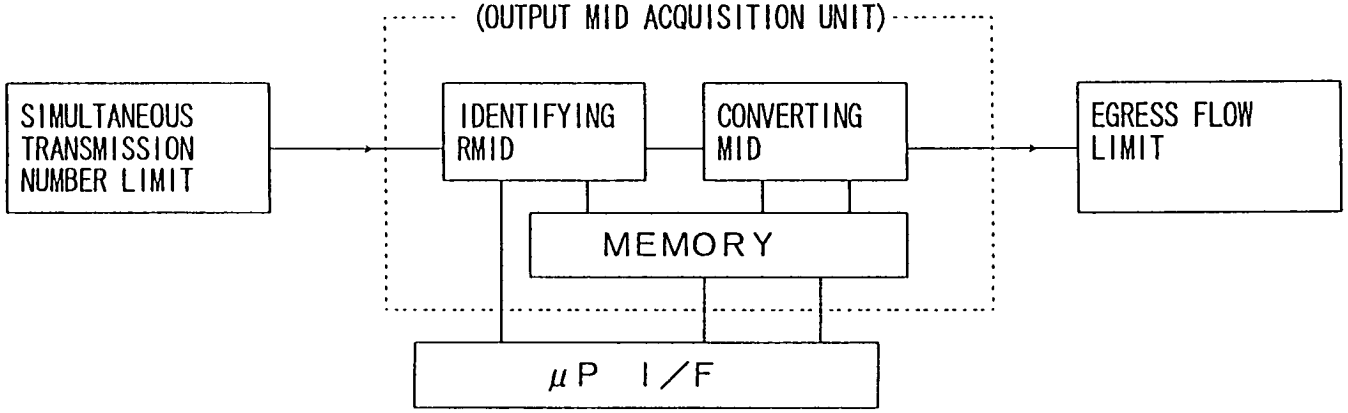

(OUTPUT MID ACQUISITION UNIT)
SIMULTANEOUS TRANSMISSION NUMBER LIMIT
IDENTIFYING RMID
CONVERTING MID
EGRESS FLOW LIMIT
MEMORY
μP I/F

FIG. 354

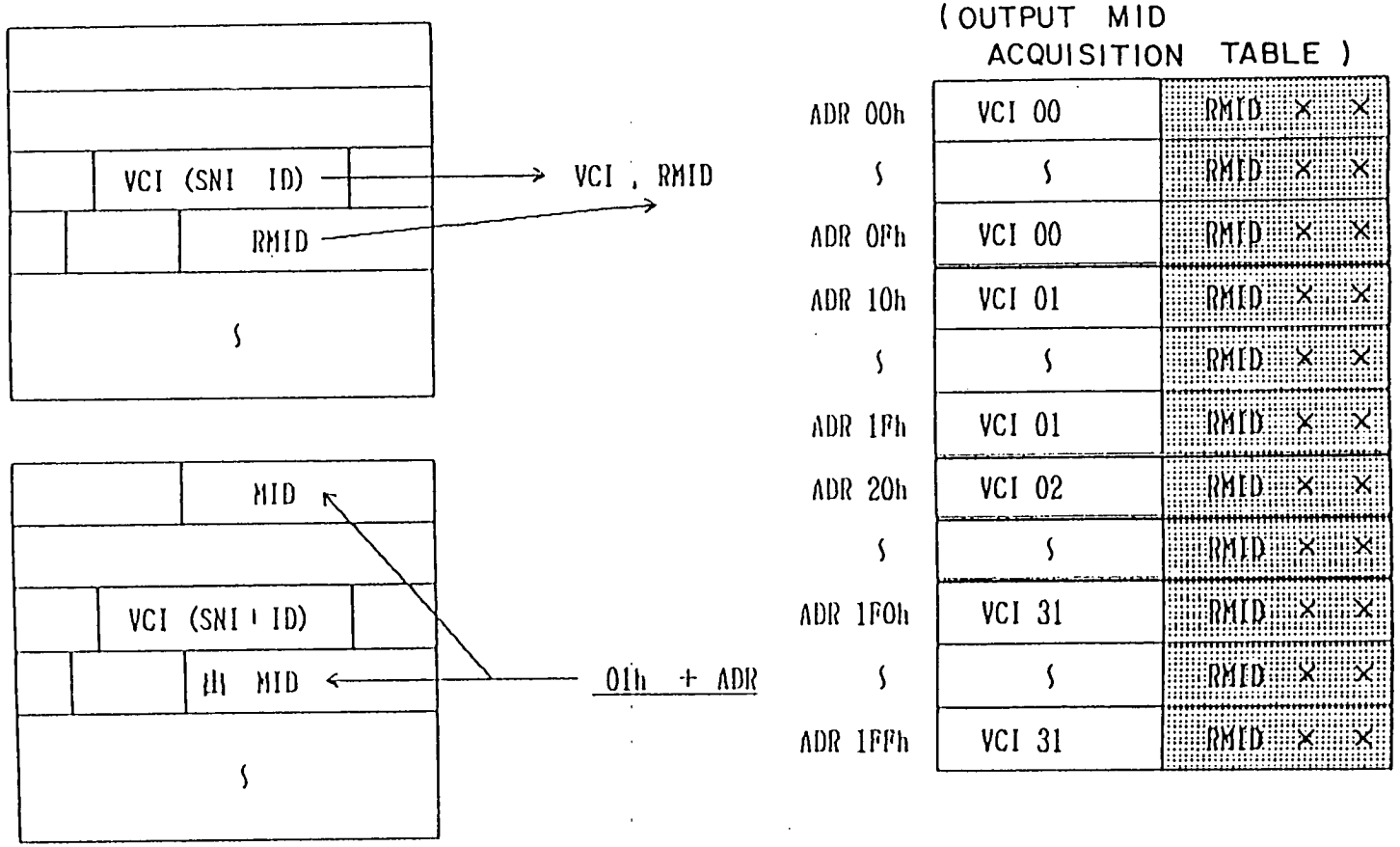

VCI (SNI ID)
VCI , RMID
RMID
MID
VCI (SNI ID)
MID
01h + ADR
(OUTPUT MID ACQUISITION TABLE)
ADR 00h
VCI 00
RMID × ×
ADR 0Fh
VCI 00
RMID × ×
ADR 10h
VCI 01
RMID × ×
ADR 1Fh
VCI 01
RMID × ×
ADR 20h
VCI 02
RMID × ×
ADR 1F0h
VCI 31
RMID × ×
ADR 1FFh
VCI 31
RMID × ×

FIG. 355

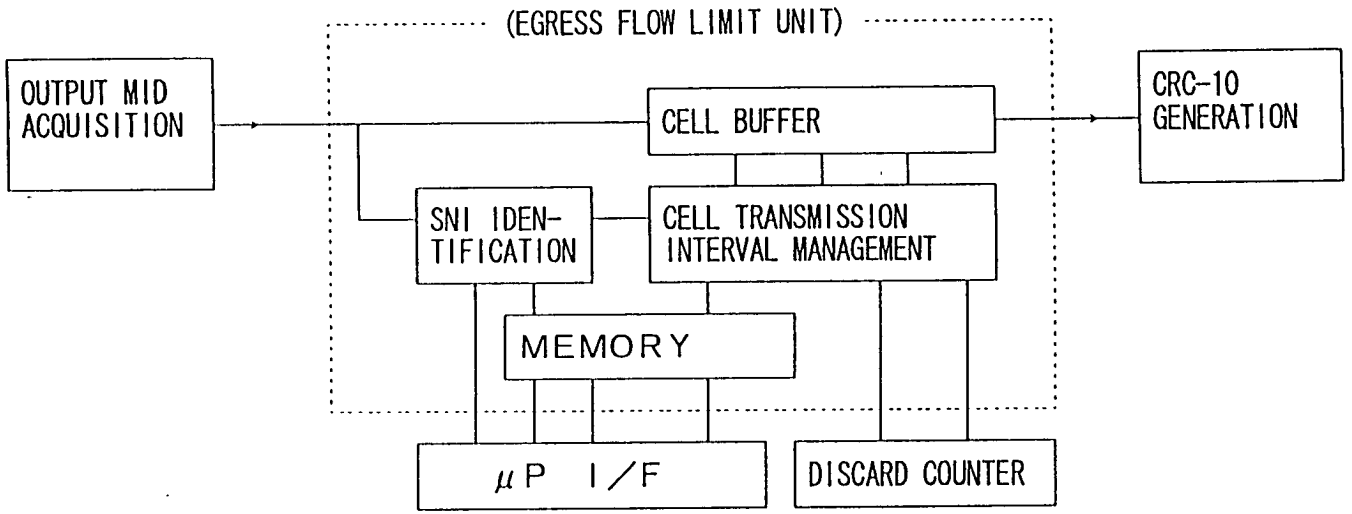

(EGRESS FLOW LIMIT UNIT)
OUTPUT MID ACQUISITION
CELL BUFFER
CRC-10 GENERATION
SNI IDEN-TIFICATION
CELL TRANSMISSION INTERVAL MANAGEMENT
MEMORY
μP I/F
DISCARD COUNTER

FIG. 356

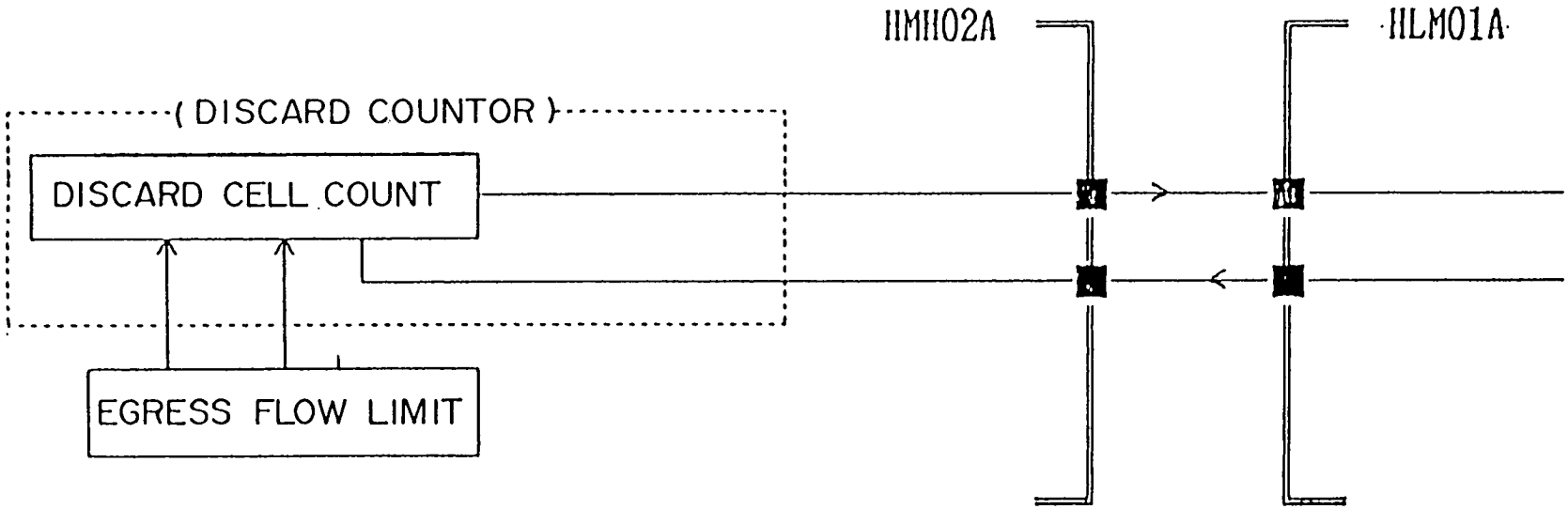

HMH02A
HLM01A
(DISCARD COUNTOR)
DISCARD CELL COUNT
EGRESS FLOW LIMIT

FIG. 357

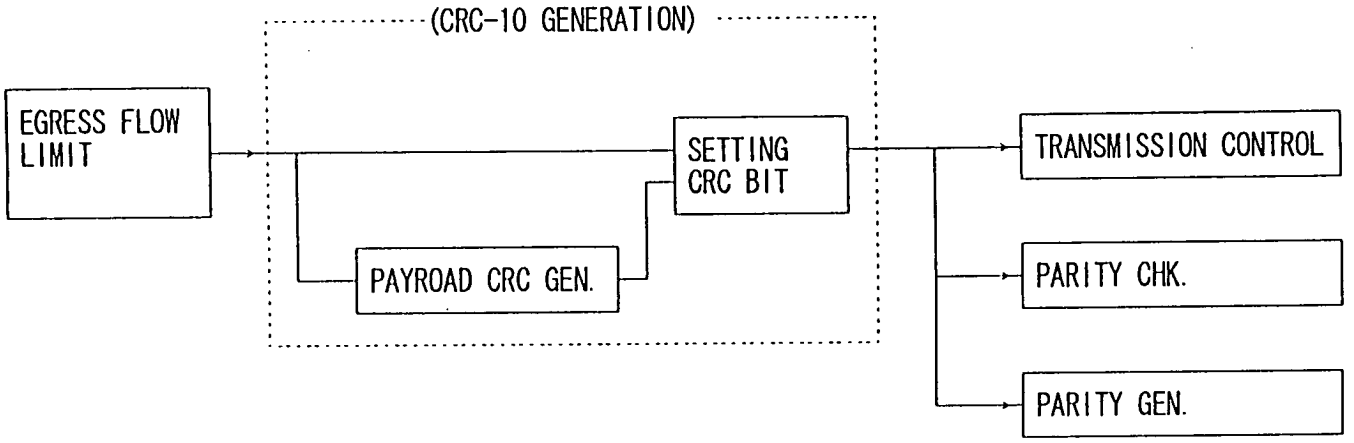

(CRC-10 GENERATION)
EGRESS FLOW LIMIT
SETTING CRC BIT
PAYROAD CRC GEN.
TRANSMISSION CONTROL
PARITY CHK.
PARITY GEN.

FIG. 358

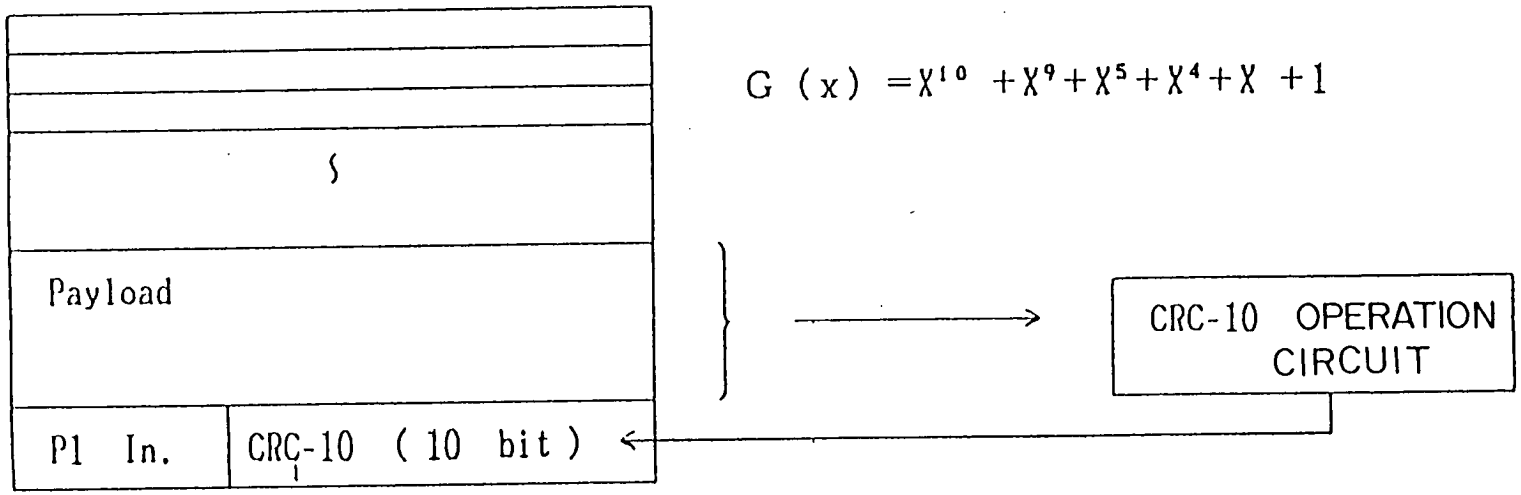

G (x) =X10 +X9+X5+X4+X +1
Payload
P1 In.
CRC-10 (10 bit)
CRC-10 OPERATION CIRCUIT

FIG. 359

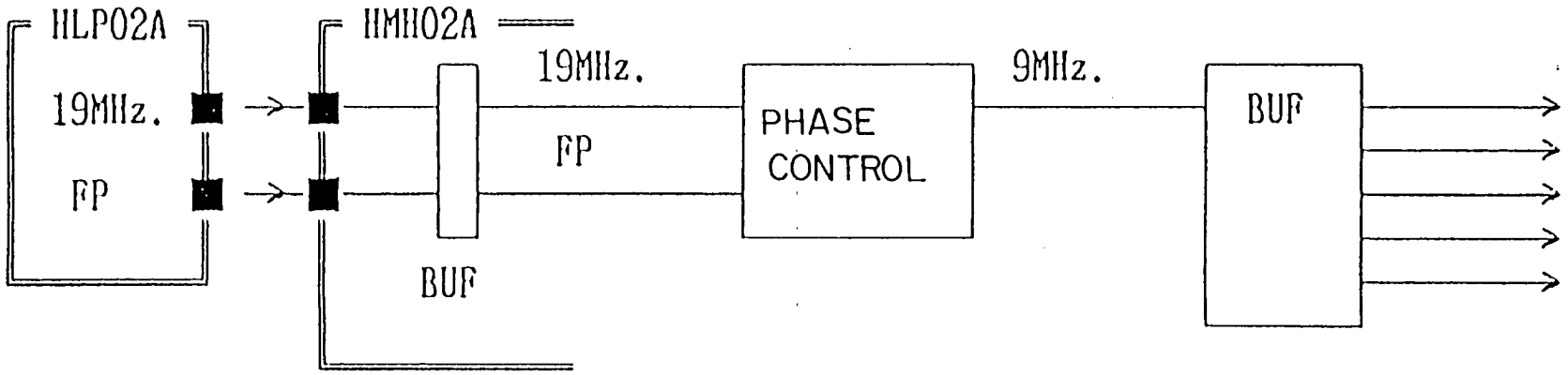


FIG. 360

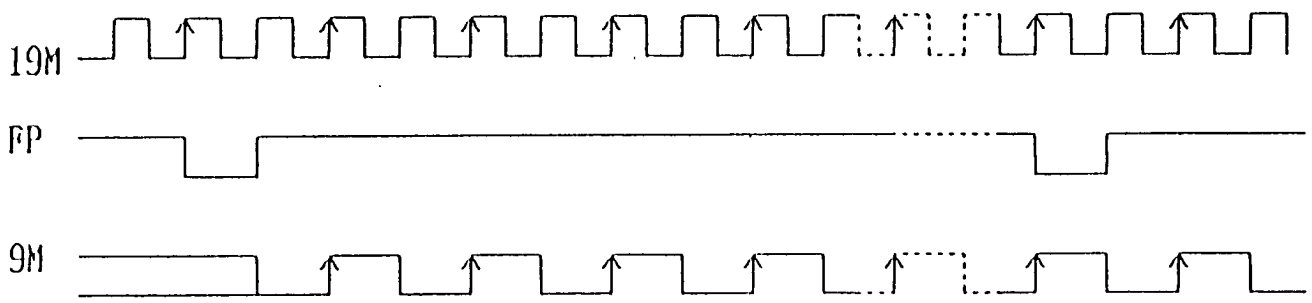


FIG. 361

ITEM	FUNCTION	
01	MESSAGE CONTROL CONTROL	CONTROLLING EACH FUNCTION OF MESSAGE CONTROL UNIT
02	MEMORY WRT/RED CONTROL	MANAGING AND CONTROLLING MEMORY OF EACH FUNCTION BLOCK
03	I/F	INTERFACING WITH MNG μ-P OF HLP02A

FIG. 362

PWCB CODE	OUTLINE OF FUNCTIONS
HMX10A	SMUX FUNCTION (MULTIPLEXING ATM-CELL FROM SMLP TO 622 MBPS HIGHWAY)
	RDMX FUNCTION (TRANSMITTING 622MBPS HIGHWAY FROM ASSW TO RMLP)
	TDMX FUNCTION (DMUXING TEST CELL FROM 622 MBPS HIGHWAY FROM ASSW)
HMX11A	RMUX FUNCTION (MULTIPLEXING ATM-CELL FROM RMLP TO 622 MBPS HIGHWAY)
	SDMX FUNCTION (DMUXING SMLP CELL FROM 622 MBPS HIGHWAY FROM ASSW)
	SIG-MUX FUNCTION (MULTIPLEXING INTRA-STATION COMMUNICATIONS CELL TO 622 MBPS HIGHWAY TO ASSW)
	SIG-DMX FUNCTION (DMUXING INTRA-STATION COMMUNICATIONS CELL FROM 622 MBPS HIGHWAY FROM ASSW)
HMX12A	SVCC FUNCTION (VCCM-CONVERTING ATM CELL FROM SMLP)
	RVCC FUNCTION (VCCM-CONVERTING ATM CELL FROM RMLP)
	TMUX FUNCTION (MULTIPLEXING TEST CELL DMUXED IN TDMX OF HMX10A TO RMLP HIGHWAY, AND MULTIPLEXING CELL DMUXED IN SDMX OF HMX11A TO SMLP HIGHWAY)
	SCHEDULER FUNCTION (CONTROLLING SMUX/RMUX OPERATION)
HSF05A	LAP TERMINATING FUNCTION (TERMINATING INTRA-STATION COMMUNICATIONS SIMPLE LAP AND COMMUNICATING WITH BSGC-SH)
	MSCN/MSD TERMINATING/EDITING FUNCTION
	VCC COPY FUNCTION
	CLOCK DISTRIBUTING FUNCTION

FIG. 363

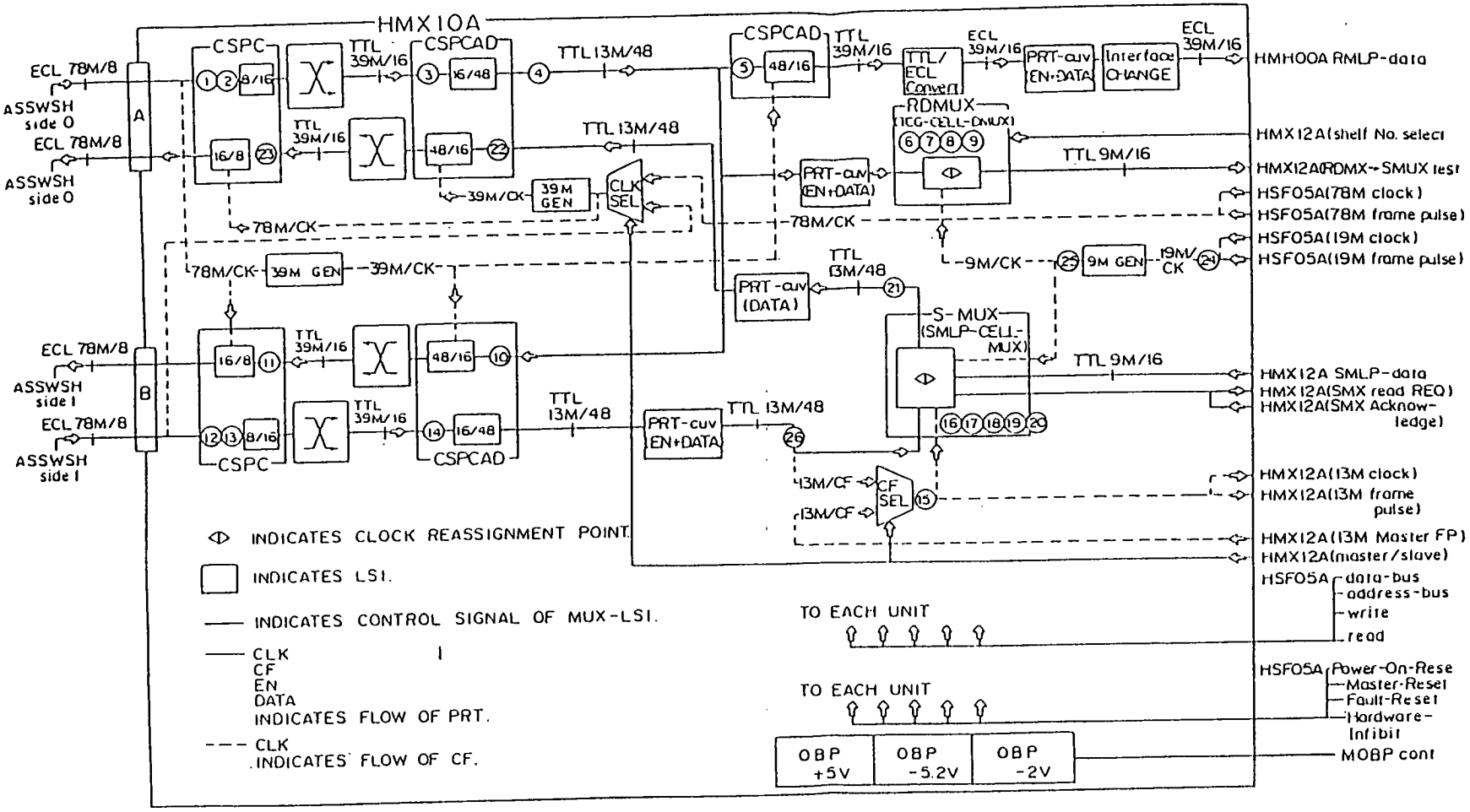

HMX10A
CSPC
CSPCAD
ECL 78M/8
ASSWSH side 0
ASSWSH side 1
TTL 39M/16
TTL 13M/48
ECL 39M/16
TTL/ ECL Convert
PRT-cuv EN+DATA
Interface CHANGE
HMH00A RMLP-data
RDMUX (ICG-CELL-DMUX)
HMX12A(shelf No. select
HMX12A(RDMX→SMUX test
TTL 9M/16
HSF05A(78M clock)
HSF05A(78M frame pulse)
HSF05A(19M clock)
HSF05A(19M frame pulse)
78M/CK
39M/CK
39M GEN
9M GEN
19M/CK
9M/CK
CLK SEL
PRT-cuv (DATA)
S-MUX (SMLP-CELL-MUX)
HMX12A SMLP-data
HMX12A(SMX read REQ)
HMX12A(SMX Acknowledge)
HMX12A(13M clock)
HMX12A(13M frame pulse)
13M/CF
CF SEL
HMX12A(13M Master FP)
HMX12A(master/slave)
HSF05A data-bus address-bus write read
HSF05A Power-On-Reset Master-Reset Fault-Reset Hardware-Inhibit
TO EACH UNIT
TO EACH UNIT
OBP +5V
OBP -5.2V
OBP -2V
MOBP cont
INDICATES CLOCK REASSIGNMENT POINT.
INDICATES LSI.
INDICATES CONTROL SIGNAL OF MUX-LSI.
CLK
CF
EN
DATA
INDICATES FLOW OF PRT.
CLK
INDICATES FLOW OF CF.

FIG. 364

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
CSINPC		ASSW(UPWARS DAISY CHAIN) ⇨ INPUT HW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSINCK		ASSW(UPWARS DAISY CHAIN) ⇨ INPUT HW 78MHz CLOCK CHECK (78MHz CLOCK)	CSPC INTERNAL MONITOR
ADINPC		ASSW(UPWARS DAISY CHAIN) ⇨ INPUT HW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
DXINCK		DMUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR
RADPC		RMLP SIDE CSPCAD INPUT PARITY CHECK (RMLP-CSPCAD P/S INPIT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
RDXPC		RTCG-DMUX INPUT PARITY CHECK (RTCG-DMUX INPUT) DATA+EN ODD PARITY	RTCG-DMUX INTERNAL MONITOR
TDXFIPC		RTCG-DMUX INTERNAL PARITY CHECK (RTCG-DMUX INTERNAL FIFO) DATA+EN ODD PARITY	RTCG-DMUX INTERNAL MONITOR
TDXSLD 0		RTCG-DMUX CONGESTION STATE CHECK (P=0,CON=0) (RTCG-DMUX INTERNAL FIFO)	RTCG-DMUX INTERNAL MONITOR
TDXSLD 1		RTCG-DMUX CONGESTION STATE CHECK (P=0,CON=1) (RTCG-DMUX INTERNAL FIFO)	
TDXSLD 2		RTCG-DMUX CONGESTION STATE CHECK (P=1,CON=0) (RTCG-DMUX INTERNAL FIFO)	
TDXSLD 3		RTCG-DMUX CONGESTION STATE CHECK (P=1,CON=1) (RTCG-DMUX INTERNAL FIFO)	
TDXBFFL		RTCG-DMUX BUFFER-FULL CHECK (RTCG-DMUX INTERNAL FIFO)	RTCG-DMUX INTERNAL MONITOR
ADIMOPC		ASSW ⇨ DOWNWARD DAISY CHAIN PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSIMOPC		ASSW ⇨ DOWNWARD DAISY CHAIN PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSIMIPC		DOWNWARD DAISY CHAIN ⇨ ASSW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
CSIMICK		DOWNWARD DAISY CHAIN ⇨ ASSW 78MHz CLOCK CHECK (78MHz CLOCK)	CSPC INTERNAL MONITOR
ADIMIPC		DOWNWARD DAISY CHAIN ⇨ ASSW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
MXINCK		MUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR

FIG. 365

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
MXINPC		DOWNWARD DAISY CHAINAIN) ⇒ ASSW HIGH-SPEED PARITY CHECK (HIGH-SPEED INPUT) DATA+EN ODD PARITY	SMLP-MUX INTERNAL MONITOR EXCKUDING LOWEST ORDER SH
MXSPC		SMLP-MUX INPUT PARITY CHECK (SMLP-MUX INPUT) DATA+EN ODD PARITY	SMLP-MUX INTERNAL MONITOR
MXFIPC		SMLP-MUX INTERNAL PARITY CHECK (SMLP-MUX INTERNAL FIFO) DATA+EN ODD PARITY	CSPCAD INTERNAL MONITOR
MXSLD 0		SMLP ⇒ SMLP-MUX CONGESTION STATE CHECK (P=0, COM=0) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	SMLP-MUX INTERNAL MONITOR
MXSLD 1		SMLP ⇒ SMLP-MUX CONGESTION STATE CHECK (P=0, COM=1) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSLD 2		SMLP ⇒ SMLP-MUX CONGESTION STATE CHECK (P=1, COM=0) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSLD 3		SMLP ⇒ SMLP-MUX CONGESTION STATE CHECK (P=1, COM=1) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXBFFL		SMLP ⇒ SMLP-MUX BUFFER-FULL CHECK (SMLP-MUX INTERNAL FIFO)	SMLP-MUX INTERNAL MONITOR
MXOCK		SMLP-MUX ⇒ ASSW(UPWARD DAISY CHAIN) 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR
ADOPC		SMLP-MUX ⇒ ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSOPC		SMLP-MUX ⇒ ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
19MCK		HSF05A ⇒ MASTER 19MHz CLOCK CHECK (19MHYz CLOCK)	PWCB INTERNAL MONITOR
9MCK		PWCB INTERNAL ,ASTER 9MHz CLOCK CHECK (9MHz CLOCK)	PWCB INTERNAL MONITOR
SMXICK		SMUX INPUT 13 MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR

FIG. 366

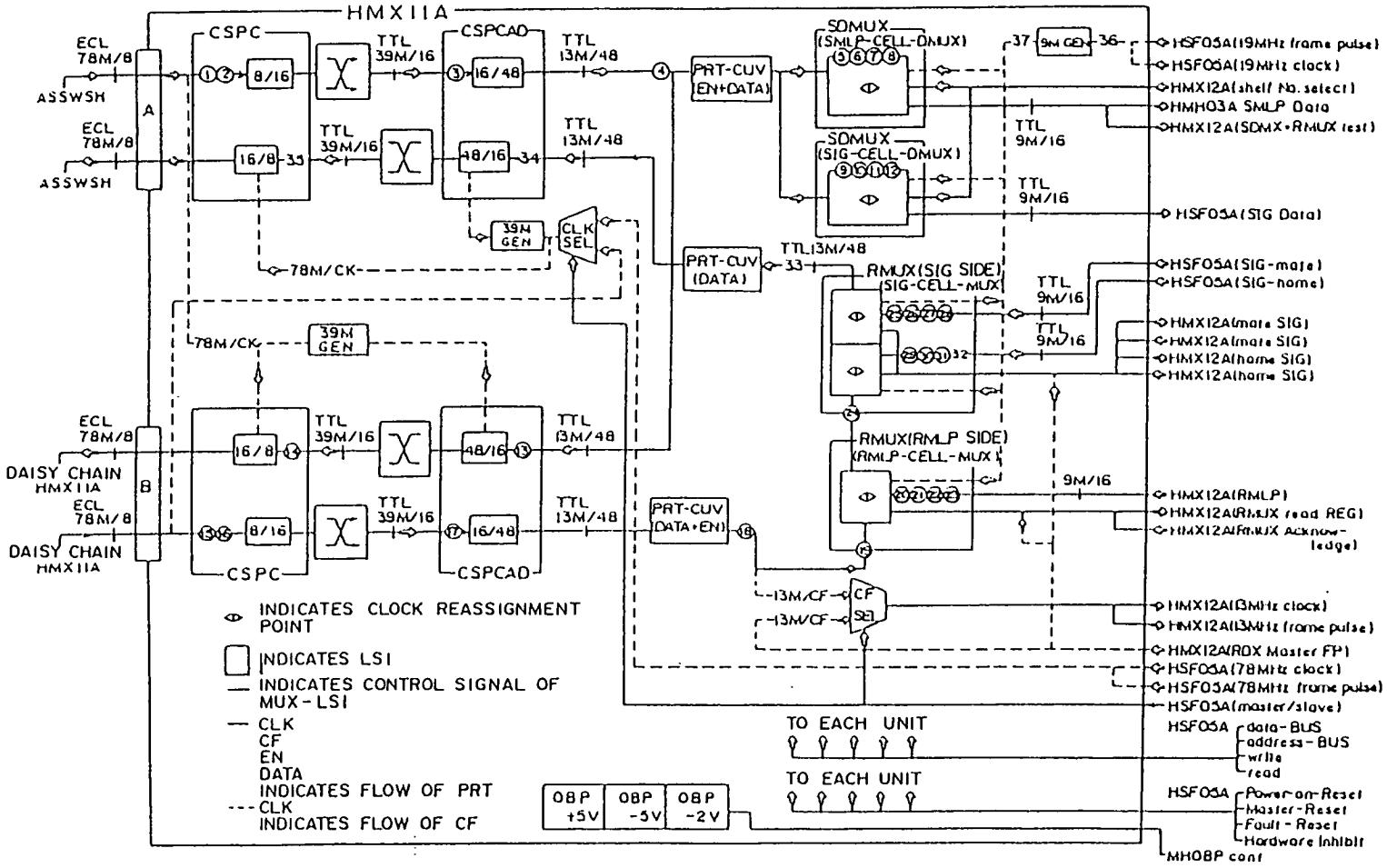

HMX11A
ECL 78M/8
ASSWSH
CSPC
8/16
16/8
TTL 39M/16
CSPCAD
16/48
48/16
TTL 13M/48
A
39M GEN
CLK SEL
78M/CK
PRT-CUV (EN+DATA)
PRT-CUV (DATA)
PRT-CUV DATA+EN)
SOMUX (SMLP-CELL-OMUX)
SOMUX (SIG-CELL-OMUX)
9M GEN
TTL 9M/16
RMUX(SIG SIDE) SIG-CELL-MUX
RMUX(RMLP SIDE) (RMLP-CELL-MUX)
B
DAISY CHAIN HMX11A
13M/CF
CF SEL
HSF05A(19MHz frame pulse)
HSF05A(19MHz clock)
HMX12A(shelf No. select)
HMH03A SMLP Data
HMX12A(SDMX+RMUX test)
HSF05A(SIG Data)
HSF05A(SIG-mate)
HSF05A(SIG-home)
HMX12A(mate SIG)
HMX12A(mate SIG)
HMX12A(home SIG)
HMX12A(home SIG)
HMX12A(RMLP)
HMX12A(RMUX read REG)
HMX12A(RMUX Acknowledge)
HMX12A(13MHz clock)
HMX12A(13MHz frame pulse)
HMX12A(ROX Master FP)
HSF05A(78MHz clock)
HSF05A(78MHz frame pulse)
HSF05A(master/slave)
TO EACH UNIT
HSF05A data-BUS address-BUS write read
HSF05A Power-on-Reset Master-Reset Fault-Reset Hardware Inhibit
MH08P cont
INDICATES CLOCK REASSIGNMENT POINT
INDICATES LSI
INDICATES CONTROL SIGNAL OF MUX-LSI
CLK
CF
EN
DATA
INDICATES FLOW OF PRT
CLK
INDICATES FLOW OF CF
08P +5V
08P -5V
08P -2V

FIG. 367

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
CSINPC	①	ASSW (UPWARD DAISY CHAIN) ⇨ INPUT HW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSINCK	②	ASSW (UPWARD DAISY CHAIN) ⇨ INPUT HW 78MHz CLOCK (78MHz CLOCK) CHECK	CSPC INTERNAL MONITOR
ADINPC	③	ASSW (UPWARD DAISY CHAIN) ⇨ INPUT HW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
DXINCK	④	DMUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PWC8 INTERNAL MONITOR
SDXINPC	⑤	SMLP-DMUX INPUT PARITY CHECK (SMLP-DMUX INPUT) DATA+EN ODD PARITY	SMLP-DMUX INTERNAL MONITOR
SDXFIPC	⑥	SMLP-DMUX INTERNAL PARITY CHECK (SMLP-DMUX INTERNAL FIFO) DATA+EN ODD PARITY	SMLP-DMUX INTERNAL MONITOR
SDXSLD 0	⑦	SMLP-DMUX CONGESTION STATE CHECK (P=0, CON=0) (SMLP-DMUX INTERNAL FIFO)	SMLP-DMUX INTERNAL MONITOR
SDXSLD 1		SMLP-DMUX CONGESTION STATE CHECK (P=0, CON=1) (SMLP-DMUX INTERNAL FIFO)	
SDXSLD 2		SMLP-DMUX CONGESTION STATE CHECK (P=1, CON=0) (SMLP-DMUX INTERNAL FIFO)	
SDXSLD 3		SMLP-DMUX CONGESTION STATE CHECK (P=1, CON=1) (SMLP-DMUX INTERNAL FIFO)	
SDXBFFL	⑧	SMLP-DMUX BUFFER-FULL CHECK (SMLP-DMUX INTERNAL FIFO)	SMLP-DMUX INTERNAL MONITOR
SGDXIPC	⑨	SIG-DMUX INPUT PARITY CHECK (SMLP-DMUX INPUT) DATA+EN ODD PARITY	SIG-DMUX INTERNAL MONITOR
SGDXFIPC	⑩	SIG-DMUX INTERNAL PARITY CHECK (SMLP-DMUX INTERNAL FIFO) DATA+EN ODD PARITY	SIG-DMUX INTERNAL MONITOR
SGDXSLD 0	⑪	SIG-DMUX CONGESTION STATE CHECK (P=0, CON=0) (SMLP-DMUX INTERNAL FIFO)	SIG-DMUX INTERNAL MONITOR
SGDXSLD 1		SIG-DMUX CONGESTION STATE CHECK (P=0, CON=1) (SMLP-DMUX INTERNAL FIFO)	
SGDXSLD 2		SIG-DMUX CONGESTION STATE CHECK (P=1, CON=0) (SMLP-DMUX INTERNAL FIFO)	
SGDXSLD 3		SIG-DMUX CONGESTION STATE CHECK (P=1, CON=1) (SMLP-DMUX INTERNAL FIFO)	

FIG. 368

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SGDXBFFL	⑫	SIG-DMUX BUFFER-FULL CHECK (SMLP-MUX INTERNAL FIFO)	SIG-DMUX INTERNAL MONITOR
ADIMOPC	⑬	ASSW ⇨ DOWNWARD DAISY CHAIN PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSIMOPC	⑭	ASSW ⇨ DOWNWARD DAISY CHAIN PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSIMIPC	⑮	DOWNWARD DAISY CHAIN ⇨ ASSW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
CSIMICK	⑯	DOWNWARD DAISY CHAIN ⇨ ASSW 78MHz CLOCK CHECK (78MHz CLOCK)	CSPC INTERNAL MONITOR
ADIMIPC	⑰	DOWNWARD DAISY CHAIN ⇨ ASSW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
RDXICK	⑱	RMUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PWC8 INTERNAL MONITOR
MXIMPC	⑲	DOWNWARD DAISY CHAIN ⇨ ASSW HIGH-SPEED DATA PARITY CHECK (RMLP-MUX HIGH-SPEED INPUT) DATA+EN ODD PARITY	RMLP-MUX INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
MXRPC	⑳	RMLP-MUX INPUT PARITY CHECK (RMLP-MUX INPUT) DATA+EN ODD PARITY	RMLP-DMUX INTERNAL MONITOR
MXFIPC	㉑	RMLP-MUX INTERNAL PARITY CHECK (RMLP-MUX INTERNAL FIFO) DATA+EN ODD PARITY	RMLP-DMUX INTERNAL MONITOR
MXSDL 0	㉒	RMLP-MUX CONGESTION STATE CHECK (P=0, CON=0) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	RMLP-MUX INTERNAL MONITOR
MXSDL 1		RMLP-MUX CONGESTION STATE CHECK (P=0, CON=1) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSDL 2		RMLP-MUX CONGESTION STATE CHECK (P=1, CON=0) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSDL 3		RMLP-MUX CONGESTION STATE CHECK (P=1, CON=1) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXBFFL	㉓	RMLP-MUX BUFFER-FULL CHECK (RMLP-MUX INTERNAL FIFO)	RMLP-MUX INTERNAL MONITOR
SGXXPC	㉔	RMLP-MUX ⇨ SIG-MUX HIGH-SPEED DATA PARITY CHECK (SIG-MUX HIGH-SPEED INPUT) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGXMPC	㉕	SIG(MATE)-MUX INPUT PARITY CHECK (SIG MATE-MUX INPUT) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR

FIG. 369

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SGXMFIPC	(26)	SIG(MATE)-MUX INTERNAL PARITY CHECK (SIG MATE-MUX INTERNAL FIFO) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGXMSL 0	(27)	SIG(MATE)-MUX CONGESTION STATE CHECK (P=0, CON=0) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
SGXMSL 1		SIG(MATE)-MUX CONGESTION STATE CHECK (P=0, CON=1) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXMSL 2		SIG(MATE)-MUX CONGESTION STATE CHECK (P=1, CON=0) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXMSL 3		SIG(MATE)-MUX CONGESTION STATE CHECK (P=1, CON=1) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXBFFL	(28)	SIG(MATE)-MUX BUFFER-FULL CHECK (SIG MATE-MUX INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
SGXHPC	(29)	SIG(HOME)-MUX INPUT PARITY CHECK (SIG HOME-MUX INPUT) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGXHFIPC	(30)	SIG(HOME)-MUX INTERNAL PARITY CHECK (SIG HOME-MUX INTERNAL FIFO) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGXHSL	(31)	SIG(HOME)-MUX CONGESTION STATE CHECK (P=0, CON=0) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
SGXHSL		SIG(HOME)-MUX CONGESTION STATE CHECK (P=0, CON=1) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXHSL		SIG(HOME)-MUX CONGESTION STATE CHECK (P=1, CON=0) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXHSL		SIG(HOME)-MUX CONGESTION STATE CHECK (P=1, CON=1) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXHBFFL	32	SIG(HOME)-MUX BUFFER-FULL CHECK (SIG HOME-MUX INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
MXCCK	33	SIG-MUX ⇨ ASSW(UPWARD DAISY CHAIN) 13MHz CLOCK CHECK (13MHz CLOCK)	PWC8 INTERNAL MONITOR
ADOPC	34	SIG-MUX ⇨ ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSOPC	35	SIG-MUX ⇨ ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
19MCK	36	HSF05A ⇨ MASTER 19MHz CLOCK CHECK (19MHz CLOCK)	PWC8 INTERNAL MONITOR
9MCK	37	PWC8 INTERNAL MASTER 9MHz CLOCK CHECK (19MHz CLOCK)	PWC8 INTERNAL MONITOR

FIG. 370

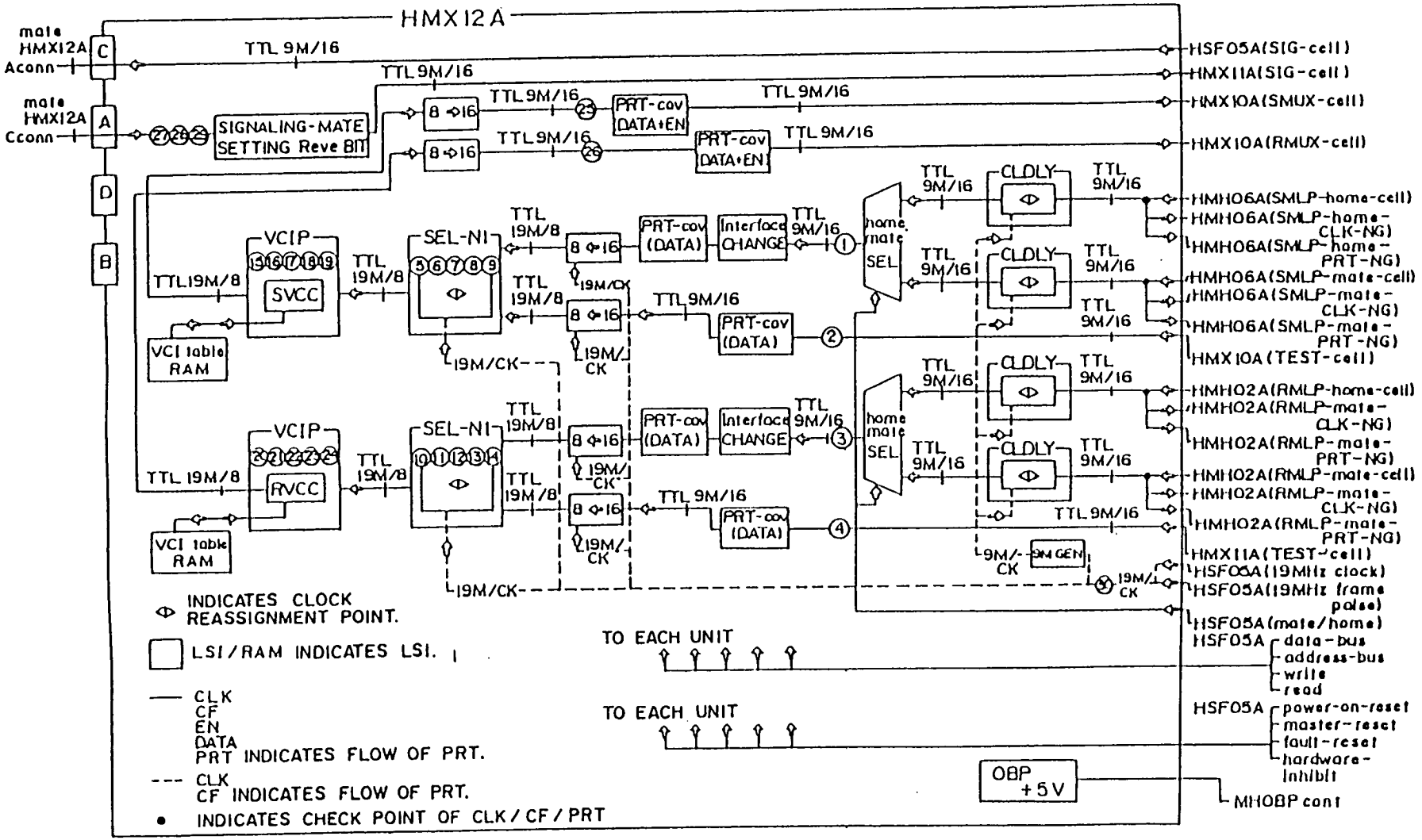

HMX12A
mate HMX12A Aconn
mate HMX12A Cconn
C
A
D
B
TTL 9M/16
SIGNALING-MATE SETTING Reve BIT
8 ⇔16
PRT-cov DATA+EN
HSF05A(SIG-cell)
HMX11A(SIG-cell)
HMX10A(SMUX-cell)
HMX10A(RMUX-cell)
VCIP
SVCC
RVCC
VCI table RAM
TTL19M/8
SEL-N1
PRT-cov (DATA)
Interface CHANGE
home mate SEL
CLDLY
HMH06A(SMLP-home-cell)
HMH06A(SMLP-home-CLK-NG)
HMH06A(SMLP-home-PRT-NG)
HMH06A(SMLP-mate-cell)
HMH06A(SMLP-mate-CLK-NG)
HMH06A(SMLP-mate-PRT-NG)
HMX10A(TEST-cell)
HMH02A(RMLP-home-cell)
HMH02A(RMLP-mate-CLK-NG)
HMH02A(RMLP-mate-PRT-NG)
HMH02A(RMLP-mate-cell)
HMH02A(RMLP-mate-CLK-NG)
HMH02A(RMLP-mate-PRT-NG)
HMX11A(TEST-cell)
19M/CK
9M GEN
HSF05A(19MHz clock)
HSF05A(19MHz frame pulse)
HSF05A(mate/home)
HSF05A data-bus address-bus write read
HSF05A power-on-reset master-reset fault-reset hardware-inhibit
TO EACH UNIT
TO EACH UNIT
OBP +5V
MHOBP cont
INDICATES CLOCK REASSIGNMENT POINT.
LSI/RAM INDICATES LSI.
CLK CF EN DATA PRT INDICATES FLOW OF PRT.
CLK CF INDICATES FLOW OF PRT.
INDICATES CHECK POINT OF CLK/CF/PRT

FIG. 371

6926E0 ET22E0

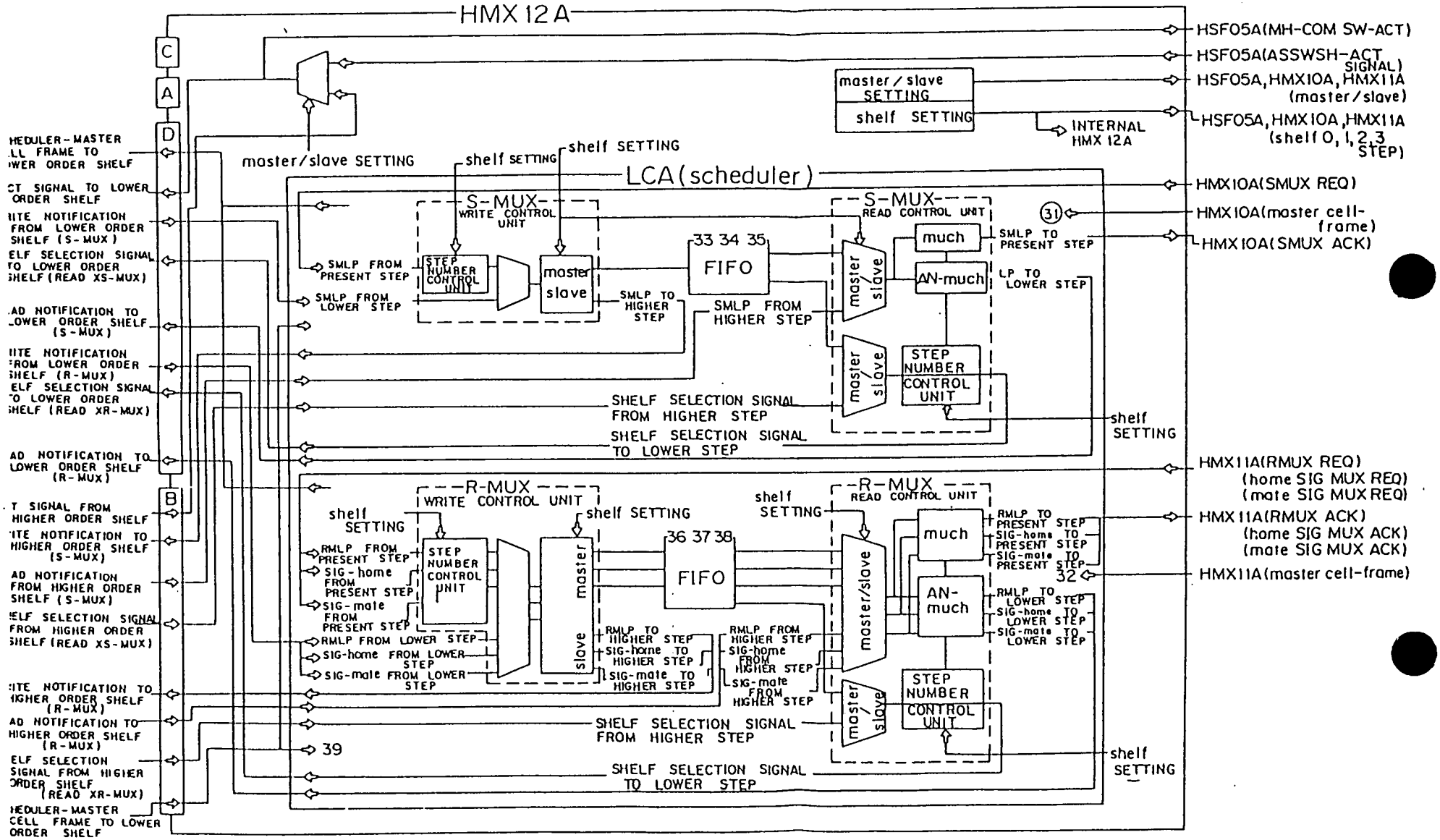


FIG. 372

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SN1PC	①	SMLP-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
STN1PC	②	STCG-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
RN1PC	③	RMLP-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
RTN1PC	④	RTCG-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
SN1MPC	⑤	SEL-N1 MEMORY PARITY CHECK (SMLP, STCG SEL-N1) DATA ODD PARITY	SEL-N1 INTERNAL MONITOR
SN1SL	⑥	SMLP SEL-N1 CONGESTION STATE CHECK (SMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
STN1SL	⑦	STCG SEL-N1 CONGESTION STATE CHECK (STCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
SN1BFFL	⑧	SMLP SEL-N1 BUFFER-FULL CHECK (SMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
STN1BFFL	⑨	STCG SEL-N1 BUFFER-FULL CHECK (STCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RN1MPC	⑩	SEL-N1 MEMORY PARITY CHECK (RMLP, RTCG SEL-N1) DATA ODD PARITY	SEL-N1 INTERNAL MONITOR
RN1SL	⑪	RMLP SEL-N1 CONGESTION STATE CHECK (RMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RTN1SL	⑫	RTCG SEL-N1 CONGESTION STATE CHECK (RTCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RN1BFFL	⑬	RMLP SEL-N1 BUFFER-FULL CHECK (RMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RTN1BFFL	⑭	RTCG SEL-N1 BUFFER-FULL CHECK (RTCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
SVCHDPC	⑮	SMLP VCIP INPUT DATA HEADER FIELD PARITY CHECK (SMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR

FIG. 373

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SVCDTPC		SMLP VCIP INPUT DATA PARITY CHECK (SMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR
SVCTBPC		SMLP VCIP VCC-TABLE PARITY CHECK	VCIP INTERNAL MONITOR
SVCMPC		SMLP VCIP VCC MEMORY CHECK	VCIP INTERNAL MONITOR
SVCALM		SMLP VCIP UNSET CELL ARRIVAL ALM	VCIP INTERNAL MONITOR
RVCHDPC		RMLP VCIP INPUT DATA HEADER FIELD PARITY CHECK (RMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR
RVCDTPC		RMLP VCIP INPUT DATA PARITY CHECK (RMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR
RVCTBPC		RMLP VCIP VCC-TABLE PARITY CHECK	VCIP INTERNAL MONITOR
RVCMPC		RMLP VCIP VCC MEMORY CHECK	VCIP INTERNAL MONITOR
RVCALM		RMLP VCIP UNSET ARRIVAL ALM	VCIP INTERNAL MONITOR
SVCOPC		SMLP-VCIP ⇨ SMLP-MUX OUTPUT PARITY CHECK DATA ODD PARITY	PWC8 INTERNAL MONITOR
RVCOPV		RMLP-VCIP ⇨ RMLP-MUX OUTPUT PARITY CHECK DATA ODD PARITY	PWC8 INTERNAL MONITOR
LAPCK		LAP MATE SYSTEM CROSS-CONNECTION MASTER 9MHz CLOCK CHECK (SIGNALING-9M CLOCK)	PWC8 INTERNAL MONITOR
LAPPC		LAP MATE SYSTEM CROSS-CONNECTION PARITY CHECK (SIGNALING-DATA) DATA+EN ODD PARITY	PWC8 INTERNAL MONITOR
SYFP		INTRA-SYSTEM PHASE MONITOR FRAME CHECK	PWC8 INTERNAL MONITOR HIGHEST ORDER CH
19MCK		HSF05A ⇨ MASTER 19MHz CLOC CHECK (19MHz CLOCK)	PWC8 INTERNAL MONITOR

FIG. 374

MONITOR POINT NAME	POINT-NO	DITAILED FAULT MONITOR	REMARKS
SHFP	(31)	SMLP MUX SCHEDULER MASTER FRAME CHECK (HMX 10A ⇨ HMX12A)	PWCB INTERNAL MONITOR
SHSGFP	32	RMLP, SIG MUX SCHEDULER MASTER FRAME CHECK (HMX11A ⇨ HMX12A)	PWCB INTERNAL MONITOR
SSHFIPC	33	SMLP MUX SCHEDULER FIFO PARITY CHECK	SMLP-SCHEDULER-LCA INTERNAL MONITOR
SSHCLT	34	SMLP MUX SCHEDULER CONTROL FAULT CHECK	SMLP-SCHEDULER-LCA INTERNAL MONITOR
SSHBFFL	35	SMLP MUX SCHEDULER FIFO FULL CHECK	SMLP-SCHEDULER-LCA INTERNAL MONITOR
RSHFIPC	36	RMLP, SIG MUX SCHEDULER FIFO PARITY CHECK	RMLP, SIG SCHEDULER LCA INTERNAL MONITOR
RSHCLT	37	RMLP SIG MUX SCHEDULER CONTROL FAULT CHECK	RMLP, SIG SCHEDULER LCA INTERNAL MONITOR
RSHBFFL	38	RMLP, SIG MUX SCHEDULER FIFO FULL CHECK	RMLP, SIG SCHEDULER LCA INTERNAL MONITOR
IMSYFP	39	INTER-DAISY-CHAIN PHASE SYNCHRONIZING MASTER FRAME CHECK	PWCB INTERNAL MONITOR

FIG. 375

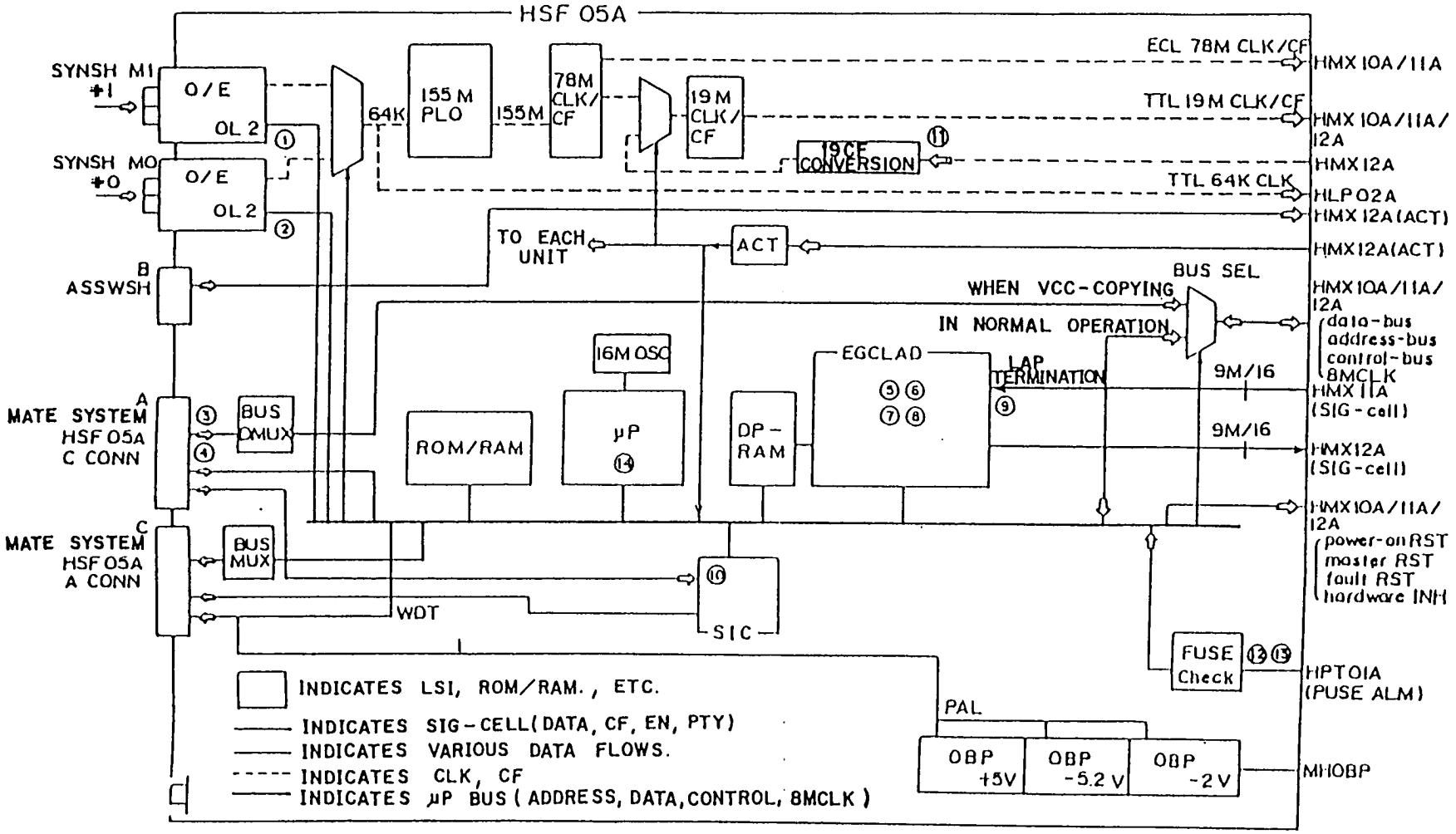

HSF 05A
SYNSH MI +1
SYNSH MO +0
O/E
OL 2
64K
155 M PLO
155M
78M CLK/CF
19 M CLK/CF
19CE CONVERSION
ECL 78M CLK/CF
TTL 19M CLK/CF
TTL 64K CLK
HMX 10A/11A
HMX 10A/11A/12A
HMX 12A
HLP 02A
HMX 12A(ACT)
TO EACH UNIT
ACT
B ASSWSH
BUS SEL
WHEN VCC-COPYING
IN NORMAL OPERATION
16M OSC
EGCLAD
LAP TERMINATION
9M/16
A MATE SYSTEM HSF 05A C CONN
BUS DMUX
ROM/RAM
μP
DP-RAM
HMX 11A (SIG-cell)
HMX 12A (SIG-cell)
C MATE SYSTEM HSF 05A A CONN
BUS MUX
WDT
SIC
power-on RST
master RST
fault RST
hardware INH
FUSE Check
HPTOIA (PUSE ALM)
INDICATES LSI, ROM/RAM., ETC.
INDICATES SIG-CELL(DATA, CF, EN, PTY)
INDICATES VARIOUS DATA FLOWS.
INDICATES CLK, CF
INDICATES μP BUS (ADDRESS, DATA, CONTROL, 8MCLK)
PAL
OBP +5V
OBP -5.2 V
OBP -2V
MHOBP

FIG. 376

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
OPTOCK		SYSTEM 0 OPTICAL 8MHz CLOCK CHECK (0# OL2)	PWC8 INTERNAL MONITOR
OPTICK		SYSTEM 1 OPTICAL 8MHz CLOCK CHECK (1# OL2)	PWC8 INTERNAL MONITOR
CR8MCK		MATE SYSTEM μP 8MHz CLOCK CHECK	PWC8 INTERNAL MONITOR
OBPALM		MATE SYSTEM OBP FAULT CHECK	PWC8 INTERNAL MONITOR
EGINPC		EGCLAD SIGNALING-DATA INPUT PARITY CHECK (HMX11A ⇨ HSF05A) DATA+EN ODD PARITY	EGCLAD INTERNAL MONITOR
EGINMPC		EGCLAD INTERNAL MEMORY PARITY CHECK	EGCLAD INTERNAL MONITOR
EGEXMPC		EGCLAD EXTERNAL MEMORY PARITY CHECK	EGCLAD INTERNAL MONITOR
EGBFFL		EGCLAD BUFFER-FULL CHECK	EGCLAD INTERNAL MONITOR
EGEXPC		SIGNALING-DATA PWC8 INPUT PARITY CHECK (HMX11A ⇨ HSF05A) DATA+EN ODD PARITY	PWC8 INTERNAL MONITOR
SIPTC		INTER-SYSTEM COMMUNICATIONS PARITY, TIME-OUT CHECK	SIC INTERNAL MONITOR
SYFP		INTER-SYSTEM PHASE SYNCHRONIZATION FRAME CHECK (HLP02A ⇨ HSF05A)	PWC8 INTERNAL MONITOR
FALM0		FUSE DISCONNECTION CHECK (HPT01A ⇨ HSF05A)	PWC8 INTERNAL MONITOR
FALM1			
WDTOF		MATE SYSTEM WATCHDOG TIMER CHECK	μP INTERNAL MONITOR

FIG. 377

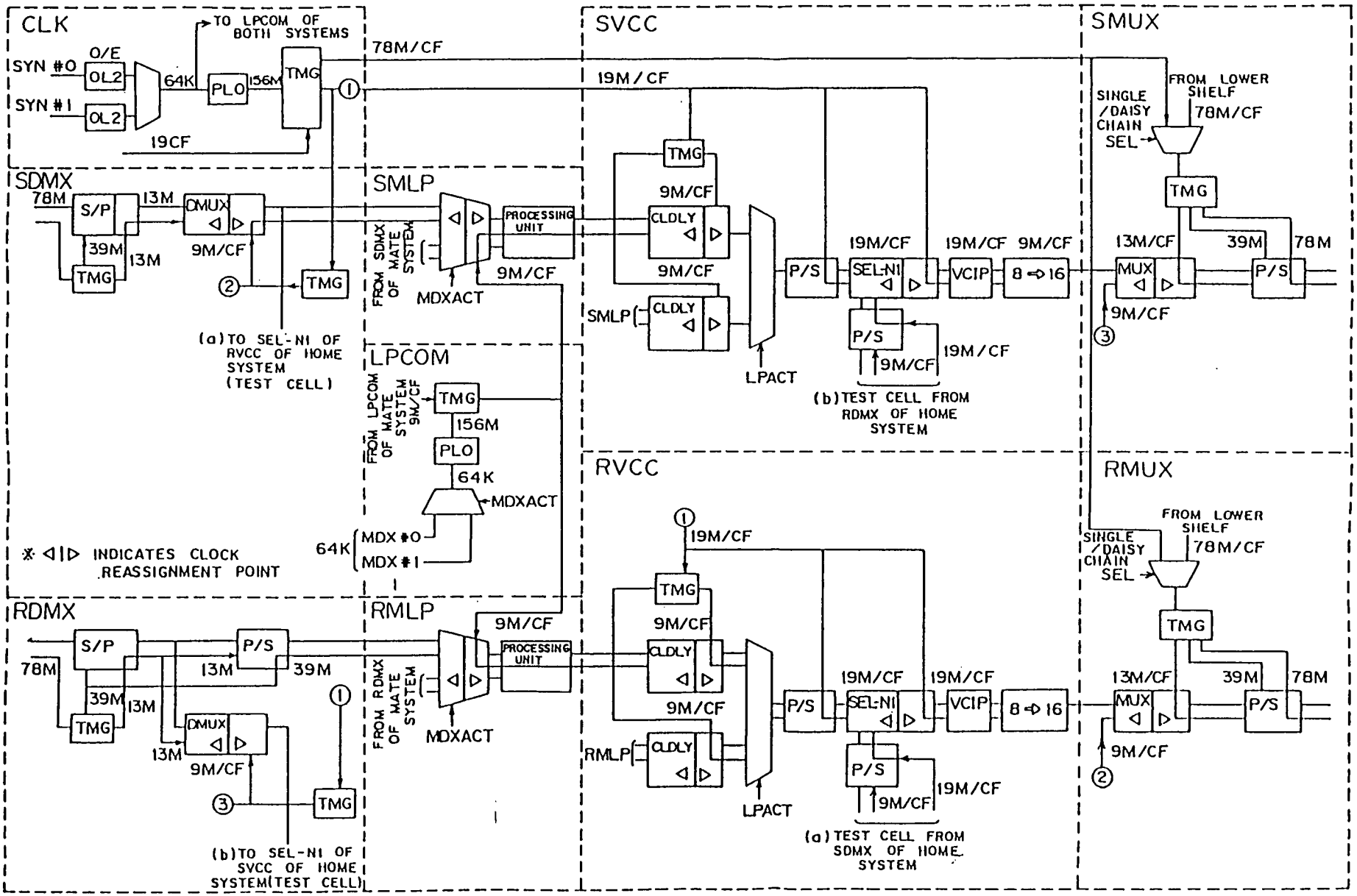

CLK
TO LPCOM OF BOTH SYSTEMS
O/E
SYN #0
SYN #1
OL2
OL2
64K
PLO
156M
TMG
78M/CF
19M/CF
19CF
SDMX
78M
S/P
13M
DMUX
39M
13M
TMG
9M/CF
TMG
(a) TO SEL-NI OF RVCC OF HOME SYSTEM (TEST CELL)
SMLP
FROM SDMX OF MATE SYSTEM
PROCESSING UNIT
9M/CF
MDXACT
LPCOM
FROM LPCOM OF MATE SYSTEM 9M/CF
TMG
156M
PLO
64K
MDXACT
64K
MDX #0
MDX #1
※ ◁|▷ INDICATES CLOCK REASSIGNMENT POINT
RDMX
78M
S/P
P/S
13M
39M
39M
13M
TMG
DMUX
13M
9M/CF
TMG
(b) TO SEL-NI OF SVCC OF HOME SYSTEM (TEST CELL)
RMLP
FROM RDMX OF MATE SYSTEM
9M/CF
PROCESSING UNIT
MDXACT
SVCC
19M/CF
TMG
9M/CF
CLDLY
9M/CF
CLDLY
SMLP
LPACT
P/S
19M/CF
SEL-NI
19M/CF
VCIP
8 ⇨ 16
P/S
9M/CF
19M/CF
(b) TEST CELL FROM RDMX OF HOME SYSTEM
RVCC
19M/CF
TMG
9M/CF
CLDLY
9M/CF
CLDLY
RMLP
LPACT
P/S
19M/CF
SEL-NI
19M/CF
VCIP
8 ⇨ 16
P/S
9M/CF
19M/CF
(a) TEST CELL FROM SDMX OF HOME SYSTEM
SMUX
SINGLE /DAISY CHAIN SEL
FROM LOWER SHELF
78M/CF
TMG
13M/CF
39M
78M
MUX
P/S
9M/CF
RMUX
SINGLE /DAISY CHAIN SEL
FROM LOWER SHELF
78M/CF
TMG
13M/CF
39M
78M
MUX
P/S
9M/CF

FIG. 378

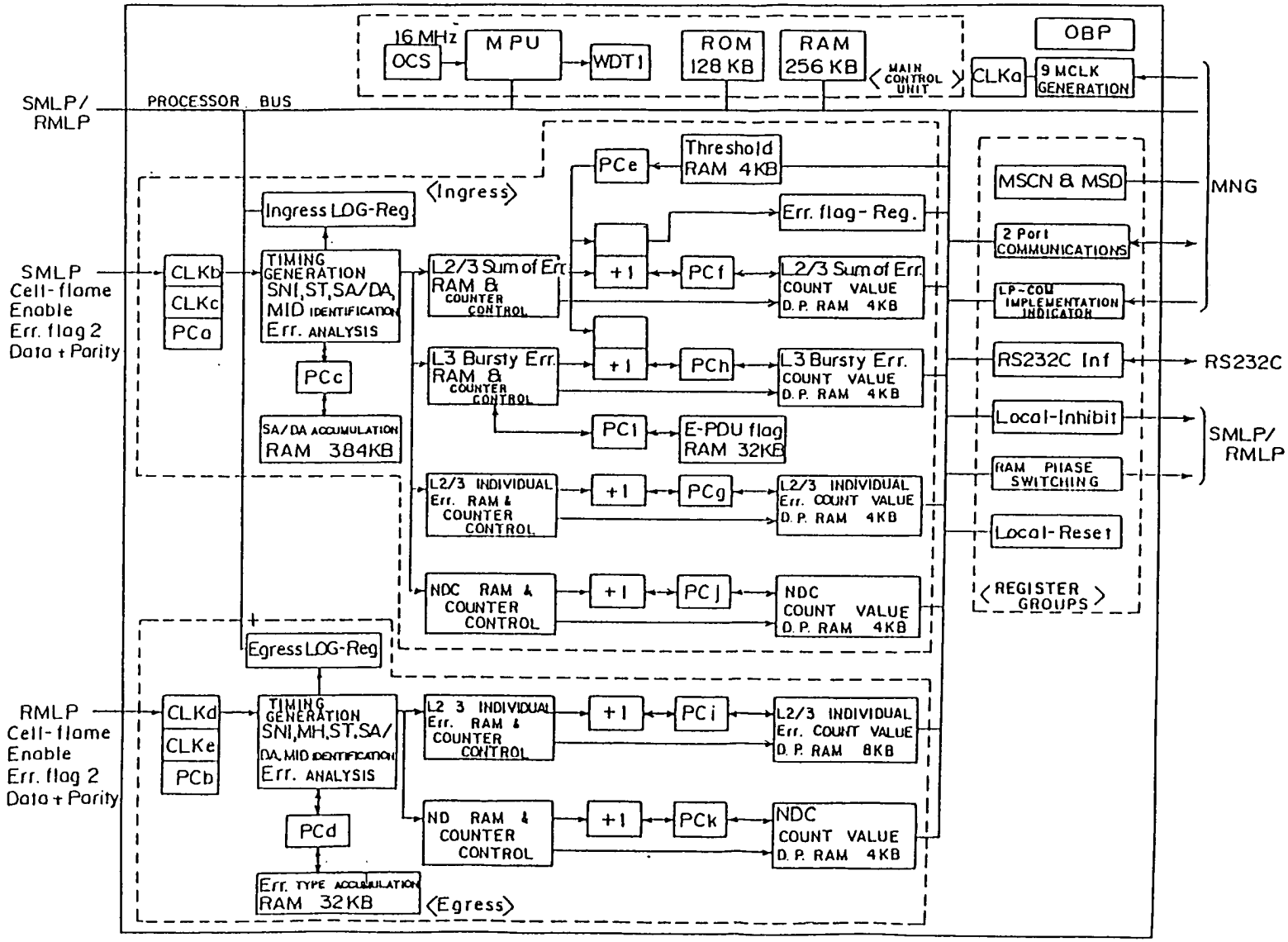

16 MHz
OCS
M PU
WDT1
ROM 128 KB
RAM 256 KB
MAIN CONTROL UNIT
OBP
CLKa
9 MCLK GENERATION
SMLP/ RMLP
PROCESSOR BUS
MNG
RS232C
SMLP/ RMLP
Threshold RAM 4KB
PCe
MSCN & MSD
2 Port COMMUNICATIONS
LP-COU IMPLEMENTATION INDICATOR
RS232C Inf
Local-Inhibit
RAM PHASE SWITCHING
Local-Reset
REGISTER GROUPS
Err. flag-Reg.
Ingress
Ingress LOG-Reg
SMLP Cell-flame Enable Err. flag 2 Data + Parity
CLKb
CLKc
PCa
TIMING GENERATION SNI,ST,SA/DA, MID IDENTIFICATION Err. ANALYSIS
PCc
SA/DA ACCUMULATION RAM 384KB
L2/3 Sum of Err RAM & COUNTER CONTROL
+1
PCf
L2/3 Sum of Err. COUNT VALUE D. P. RAM 4KB
L3 Bursty Err. RAM & COUNTER CONTROL
PCh
L3 Bursty Err. COUNT VALUE D. P. RAM 4KB
PCi
E-PDU flag RAM 32KB
L2/3 INDIVIDUAL Err. RAM & COUNTER CONTROL
PCg
L2/3 INDIVIDUAL Err. COUNT VALUE D. P. RAM 4KB
NDC RAM & COUNTER CONTROL
PCJ
NDC COUNT VALUE D. P. RAM 4KB
Egress LOG-Reg
RMLP Cell-flame Enable Err. flag 2 Data + Parity
CLKd
CLKe
PCb
TIMING GENERATION SNI,MH,ST,SA/ DA, MID IDENTIFICATION Err. ANALYSIS
PCd
Err. TYPE ACCUMULATION RAM 32KB
L2 3 INDIVIDUAL Err. RAM & COUNTER CONTROL
PCi
L2/3 INDIVIDUAL Err. COUNT VALUE D. P. RAM 8KB
ND RAM & COUNTER CONTROL
PCk
NDC COUNT VALUE D. P. RAM 4KB
Egress

FIG. 379

BLOCK	FUNCTION	
MAIN CONTROL UNIT	MPU	16BIT MICROPROCESSOR (80C186-10)
	RAM	128K X 16 BIT SRAM FOR FIRMWARE WORK
	ROM	64K X 16 BIT EPROM FOR FIRMWARE STORAGE
	OCS	16 MHz OSCILLATOR
REGISTER GROUPS	MSCN & MSD	MSCN: AREA FOR USE IN REPORTING EACH CHECK NG (LISTED IN FIGURE 6.1.2) TO HLP02A
		MSD : AREA FOR USE IN SETTING PSEUDO-FAULT FROM HLP02A
	2PORT COMMUNICATIONS	ACTIVATING/RELEASING INTERRUPTION DURING COMMUNICATIONS WITH HLP02A
	LP-COM IMPLEMENTATION INDICATOR	INDICATING IMPLEMENTATION OF LP-COM AND OTHER PWCB (HLP02A AND HLM00A)
	RS232C INF	INTERFACE WITH WORK STATION FOR DEBUGGING
	LOCAL-INHIBIT	INITIAL STATE INDICATOR OF PM/TM COUNT VALUE STORAGE RAM
	RAM PHASE SWITCHING	INDICATOR OF HARDWARE ACCESS PHASE OF PM/TM COUNT VALUE STORAGE 2-PHASE RAM
	LOCAL-RESET	INTERNAL RESET
CLK GENERATION		GENERATING 9MCLK USING 19MCLK AND 19MFP FROM HLP02A
OBP		CONVERTING ON BOARD POWER -48V INTO +5V

FIG. 380

0000000-0000000

BLOCK	FUNCTION
INGRESS	COUNTING INGRESS L2/3 SUM OF ERROR, L2/3 INDIVIDUAL ERROR, L3 BURSTY ERROR, NETWORK DATA COLLECTION DERINED ACCORDING TO TR774.
TIMING GENERATION	GENERATING EACH TIMING ACCORDING TO 9MCLK, CELL FRAME (CF), AND ENABLE (EN) SIGNAL.
SNI, ST, SA/DA, MID IDENTIFICATION	IDENTIFYING SOURCE SNI, SEGMENT TYPE, SA/DA/, MID AND MID FROM CELL DATA
ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (FF) SIGNAL
INGRESS LOG-REG.	AREA FOR USE IN REPORTING ERROR TYPE, SOURCE SNI, SA, AND DA WHEN LOG OBJECT ERROR ARISES
SA/DA TYPE ACCUMULATION RAM	RAM FOR ACCUMULATING SA AND DA TO COLLECT LOG.
THRESHOLD RAM	FIRMWARE SETS THRESHOLD OF L2/3 SUM OF ERROR, AND NI AND NB OF L3 BURSTY ERROR AT INITIALIZATION
L2/3 SUM OF ERR. COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF L2/3 SUM OF ERROR
ERR. FLAG-REG.	AREA FOR USE IN REPORTING TO FIRMWARE WHEN SUM OF ERROR COUNT VALUE EXCEEDS THRESHOLD
L3 BURSTY ERR. COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING L3 BURSTY ERROR PDU COUNT VALUE, ERRORED-PDU COUNT VALUE, INTERVAL COUNT VALUE, AND BAD INTERVAL COUNT VALUE
E-PDU FLAG RAM	RAM FOR USE IN COUNTING NUMBER OF ERRORED PDU OF L3 BURSTY ERROR
L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR
NDC COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF NETWORK DATA COLLECTION
EGRESS	COUNTING EGRESS L2/3 INDIVIDUAL ERROR AND NETWORK DATA COLLECTION DEFINED ACCORDING TO TR774.
TIMING GENERATION	GENERATING EACH TIMING ACCORDING TO 9MCLK, CELL FRAME (CF), AND ENABLE (EN) SIGNAL.
SNI, MH, ST, SA/DA, MID IDENTIFICATION	IDENTIFYING DESTINATION SNI, SOURCE MH, SEGMENT TYPE, SA/DA, AND MID FROM CELL DATA
ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (FF) SIGNAL
EGRESS LOG-REG.	AREA FOR USE INREPORTING ERROR TYPE, SOURCE SNI, SA, AND DA WHEN LOG OBJECT ERROR ARISES
ERR. TYPE ACCUMULATION RAM	ACCUMULATING ERROR TYPE FOR LOG COLLECTION
L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR
NDC COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF NETWORK DATA COLLECTION

FIG. 381

CHECK NAME	OBJECT OF CHECK
CLKa	DISCONNECTION CHECK OF 19M CLOCK AND FRAME PULSE FROM HLP02A
CLKb	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND CELL FRAME FROM SMLP
CLKc	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND ERROR FLAG 2 FROM SMLP
CLKd	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND CELL FRAME FROM RMLP
CLKe	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND ERROR FLAG 2 FROM RMLP
WDTI	TIMEOUT OF WATCHDOG TIMER, AND DICONNECTION OF MPU OUTPUT 8M CLOCK
PCa	PARITY CHECK OF DATA AND ENABLE FROM SMLP
PCb	PARITY CHECK OF DATA AND ENABLE FROM RMLP
PCc	PARITY CHECK OF SA/DA ACCUMULATION RAM
PCd	PARITY CHECK OF ERROR TYPE ACCUMULATION RAM
PCe	PARITY CHECK OF THRESHOLD RAM
PCf	PARITY CHECK OF L2/3 SUM OF ERR. COUNT VALUE D.P. RAM
PCg	PARITY CHECK OF INGRESS L2/3 INDIVIDUAL ERR. COUNT VALUE D.P. RAM
PCh	PARITY CHECK OF L3 BURSTY ERR. COUNT VALUE D.P. RAM
PCi	PARITY CHECK OF EGRESS L2/3 INDIVIDUAL ERR. COUNT VALUE D.P. RAM
PCj	PARITY CHECK OF INGRESS NDC COUNT VALUE D.P. RAM
PCk	PARITY CHECK OF EGRESS NDC COUNT VALUE D.P. RAM
PCl	PARITY CHECK OF E-PDU FLAG RAM

FIG. 382

US 6,636,509 B1

CHECK NAME	CHECK CONDITION
PCc	RECEIVING ERROR NOTIFICATION OF LOG REQUIRED ERROR FROM SMLP
PCd	CELL RECEIVED FROM RMLP IS SIP-BOM OR SIP-SSM
PCe	RECEIVING ERROR NOTIFICATION OF L2/3 SUM OF ERROR FROM SMLP
PCf	RECEIVING ERROR NOTIFICATION OF L2/3 SUM OF ERROR FROM SMLP
PCg	RECEIVING ERROR NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM SMLP
PCh	CELL RECEIVED FROM SMLP IS INTER-BOM (SIP-BOM OR SIP-SSM UNLESS ENCAPSULATED).
	RECEIVING ERROR NOTIFICATION OF L3 BURSTY ERROR THAT ERRORED-PDU SHOULD BE COUNTED
	NI=PDU COUNT AS RESULT OF NI COMPARISON IN L3 BURSTY ERROR PROCESS
	NI≦ERRORED-PDU COUNT AS RESULT OF NB COMPARISON IN L3 BURSTY ERROR PROCESS
	CHECKING UNDER ANY OF FOUR ABOVE LISTED CONDITIONS
PCi	RECEIVING ERROR NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM RMLP
PCj	CELL RECEIVED FROM SMLP IS CELL OTHER THAN INTER-BOM.
	CELL RECEIVED FROM SMLP IS INTER-BOM (SIP-BOM OR SIP-SSM UNLESS ENCAPSULATED).
	RECEIVING ERROR NOTIFICATION OF NDC INDIVIDUAL COUNT ERROR FROM SMLP
	CHECKING UNDER ANY OF THREE ABOVE LISTED CONDITIONS
PCk	CELL RECEIVED FROM RMLP IS CELL OTHER THAN INTER-BOM
	CELL RECEIVED FROM RMLP IS SIP-BOM OR SIP-SSM.
	RECEIVING ERROR NOTIFICATION OF NDC INDIVIDUAL COUNT ERROR FROM RMLP
	CHECKING UNDER ANY OF THREE ABOVE LISTED CONDITIONS
PCl	CELL RECEIVED FROM SMLP IS EOM.

FIG. 383

GROUP	ITEMS	Source	LEVEL	Check	Action	No
A	1	Maintenance	L3	MRI time out	Count Log	1
B	1	TR-772	L2	Busy Bit = 0	Stop	—
C	1	Maintenance	L2	HCS Violation	Stop Count	—
D	1	TR-772	L2	NCI ≠ 規定pattern	Stop	—
E	1	Maintenance	L2	Payload CRC Violation	Stop Count	2
F	1	Maintenance	L2	Payload Length Error	Stop Count	3
	2	Maintenance	L2	BOMs/SSMs with Invalid MIDs	Stop Count	4
G	1	Maintenance	L2	MID Currently Active	Stop Count	5
	2	Maintenance	L2	Unappreved MID	Stop Count	5
H	1	Maintenance	L2	Invalid Sequence Number	Stop Count	6
I	1	Maintenance	L3	Invalid SA Type	Stop Count	7
	2	Maintenance	L3	Invalid DA Type	Stop Count	8
J	1	Maintenance	L3	Invalid SMDS Address Type	Stop Count	9
K	1	Maintenance	L3	Individual DA Assign to Org. SNI	Stop Count	10
	2	Maintenance	L3	DA Field Format Error	Stop Count Log	11
	3	Maintenance	L3	SA Field Format Error	Stop Count Log	12
L	1	Maintenance	L3	Invalid BAsize Field Value	Stop Count Log	13
	2	NDC	L3	Access Class Violation	Stop Count Log	14
M	1	Maintenance	L3	Invalid HEL Field Value	Stop Count Log	15
	2	Maintenance	L3	Invalid HE- Carrier Selection	Stop Count Log	16
	3	Maintenance	L3	Invalid HE- Version	Stop Count Log	17
	4	NDC	L3	Exceed Max. Number of CDU —	Stop Count Log	18
	5	NDC	L3	SA not Assigned to Org. SNI	Stop Count Log	19
	6	NDC	L3	DA Screening Violation	Stop Count Log	20
N	1	Maintenance	L3	BEtag Mismatch	Stop Count Log	21
	2	Maintenance	L3	Incorrect Length	Stop Count Log	22
	3	Maintenance	L3	BAsize Field≠Length Field	Stop Count Log	23
O	1	UNIQUE SPECIFICATION	--	MID Assigned Error	Stop Count	24
	2	UNIQUE SPECIFICATION	L3	End User Blocking	Stop Count	25

FIG. 384

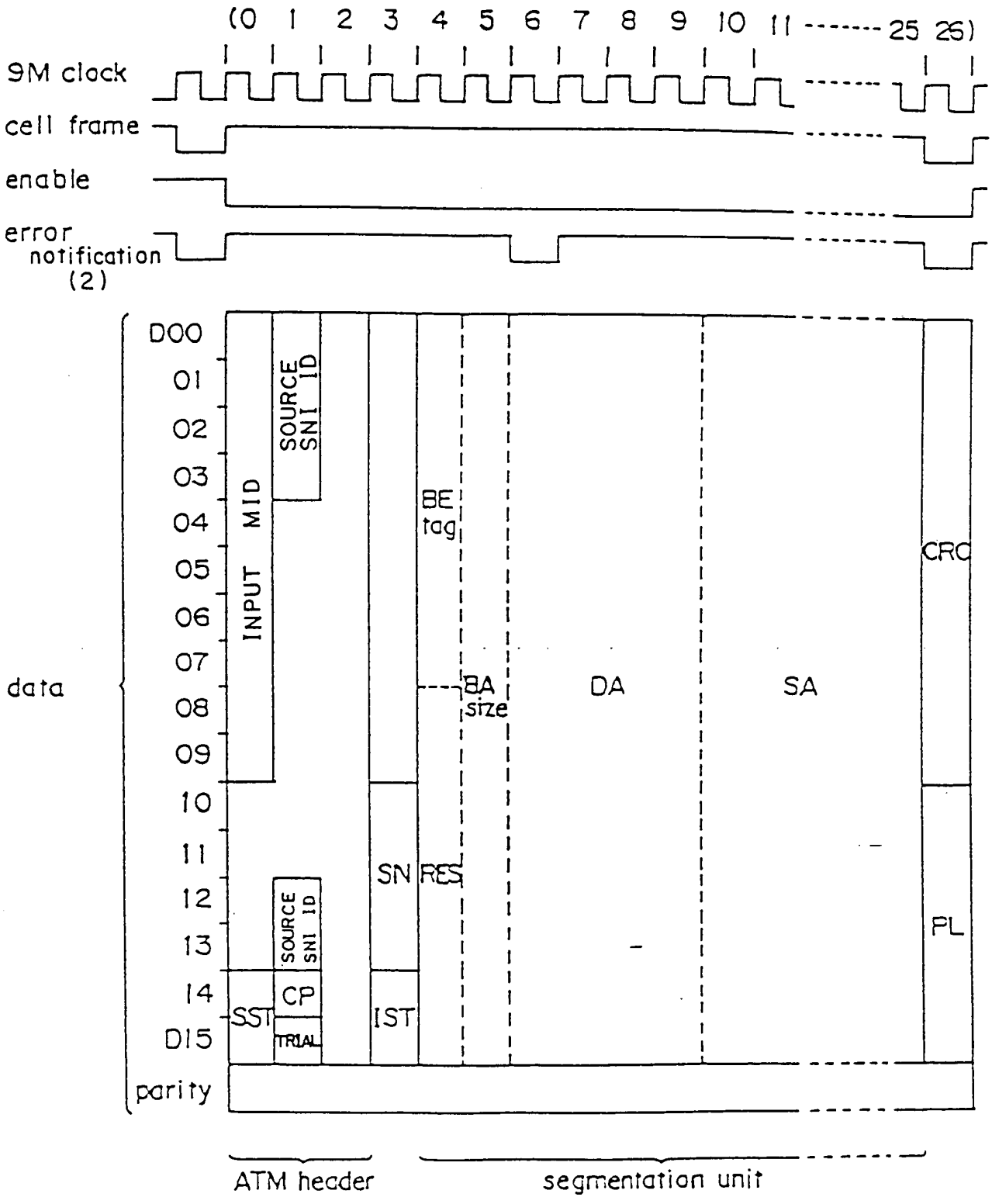

(0 1 2 3 4 5 6 7 8 9 10 11 ------- 25 26)
9M clock
cell frame
enable
error notification (2)
data
D00
01
02
03
04
05
06
07
08
09
10
11
12
13
14
D15
parity
INPUT MID
SOURCE SNI ID
BE tag
BA size
DA
SA
CRC
SN
RES
SOURCE SNI ID
PL
SST
CP
TRIAL
IST
ATM header
segmentation unit

FIG. 385

SIGNAL NAME	POLARITY	EXPLANATION
9M CLOCK	——	ALL SIGNALS OTHER THAN BASIC CLOCK CHANGE AT RISE OF THIS CLOCK
CELL FRAME	⇨	LAST 1 τ OF SIGNAL CELL INDICATING BOUNDARY OF CELL ONLY INDICATES L
ENABLE	⇨	SIGNAL INDICATING VALID/INVALID OF CELL ENTIRE CELL AREA INDICATES L WHEN VALID
ERROR NOTIFICATION (2)	⇨	SIGNAL INDICATING ERROR TYPE DESCRIBED LATER IN DETAIL L INDICATES ERROR
DATA	POSITIVE	16 PARALLEL DATA + PARITY PARITY IS ODD PARITY IN TOTAL 17 BITS OF 16 BIT PARALLEL DATA + ENABLE

FIG. 386

	SST	IST
Inter-BOM	1 0	1 0
SIP-BOM	1 0	(0 0)
COM	0 0	0 0
EOM	0 1	0 1
SIP-SSM	1 1	(0 1)

FIG. 387

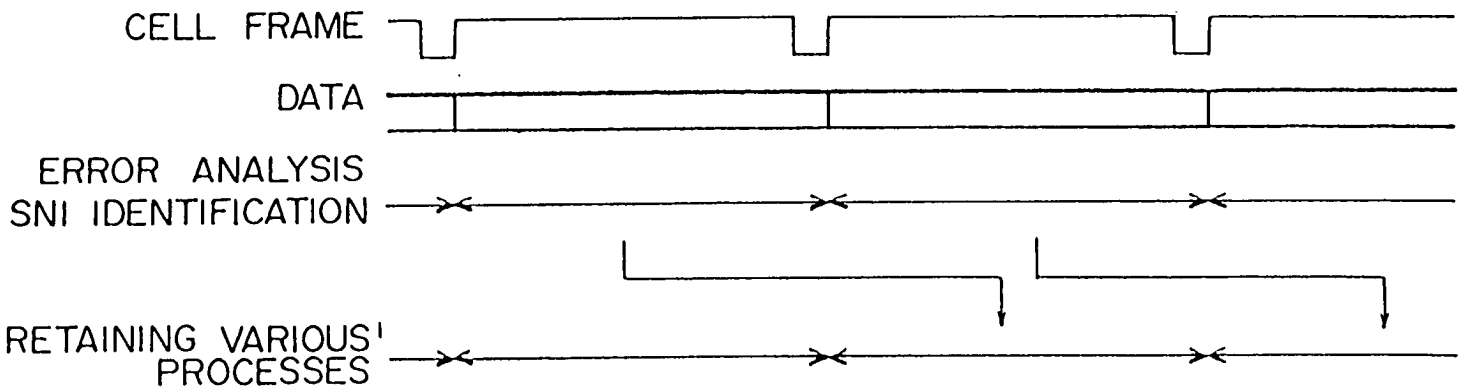

CELL FRAME
DATA
ERROR ANALYSIS
SNI IDENTIFICATION
RETAINING VARIOUS
PROCESSES

FIG. 388

6692E0 ET2Z260

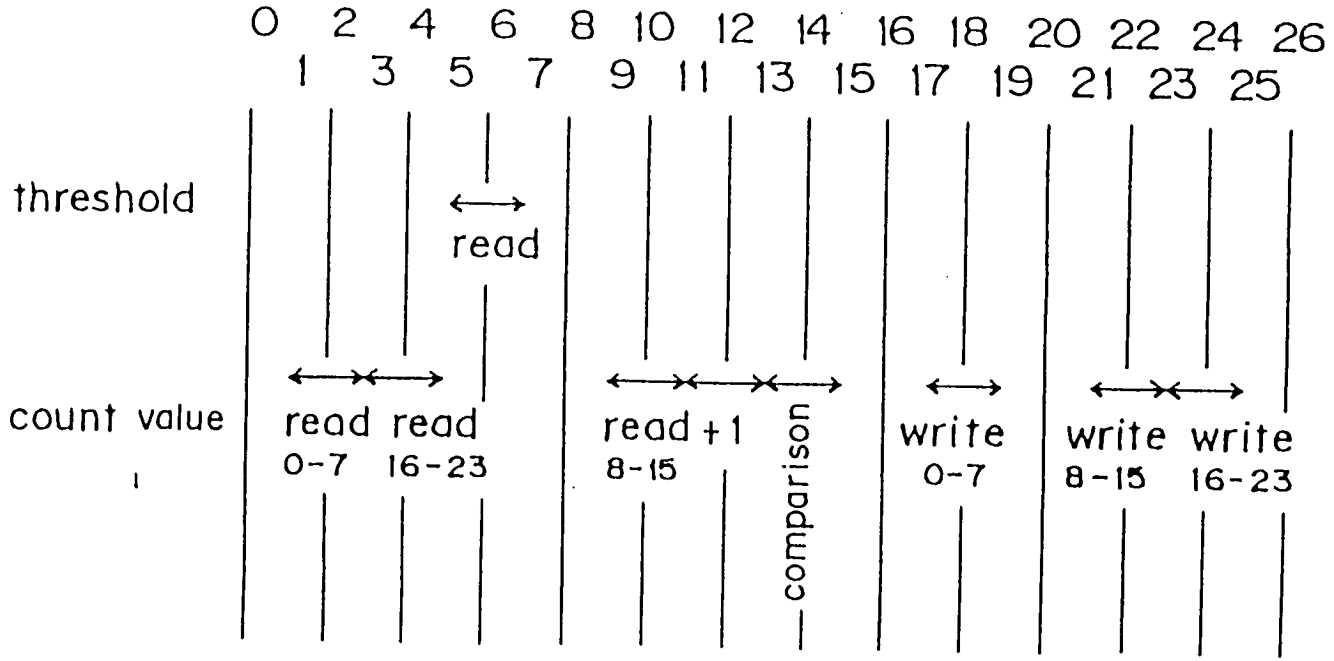


FIG. 389

0692E0 EP2772E0

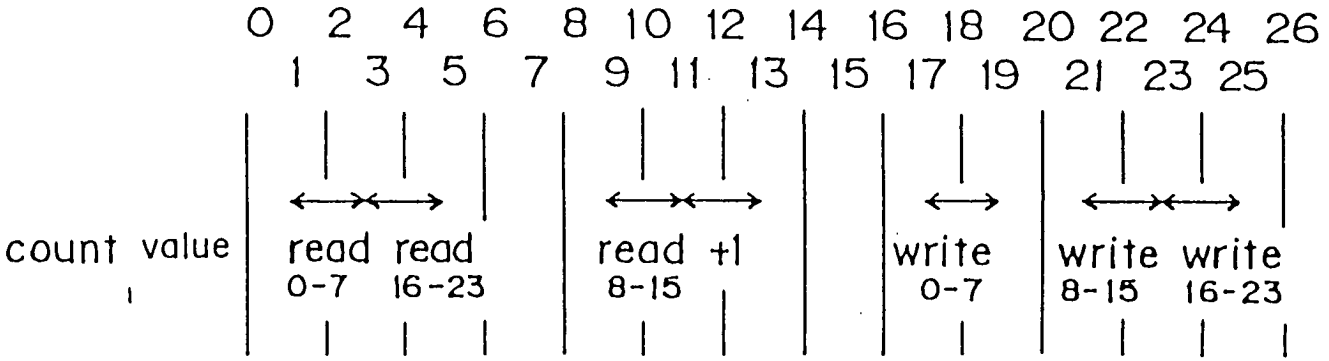


FIG. 390

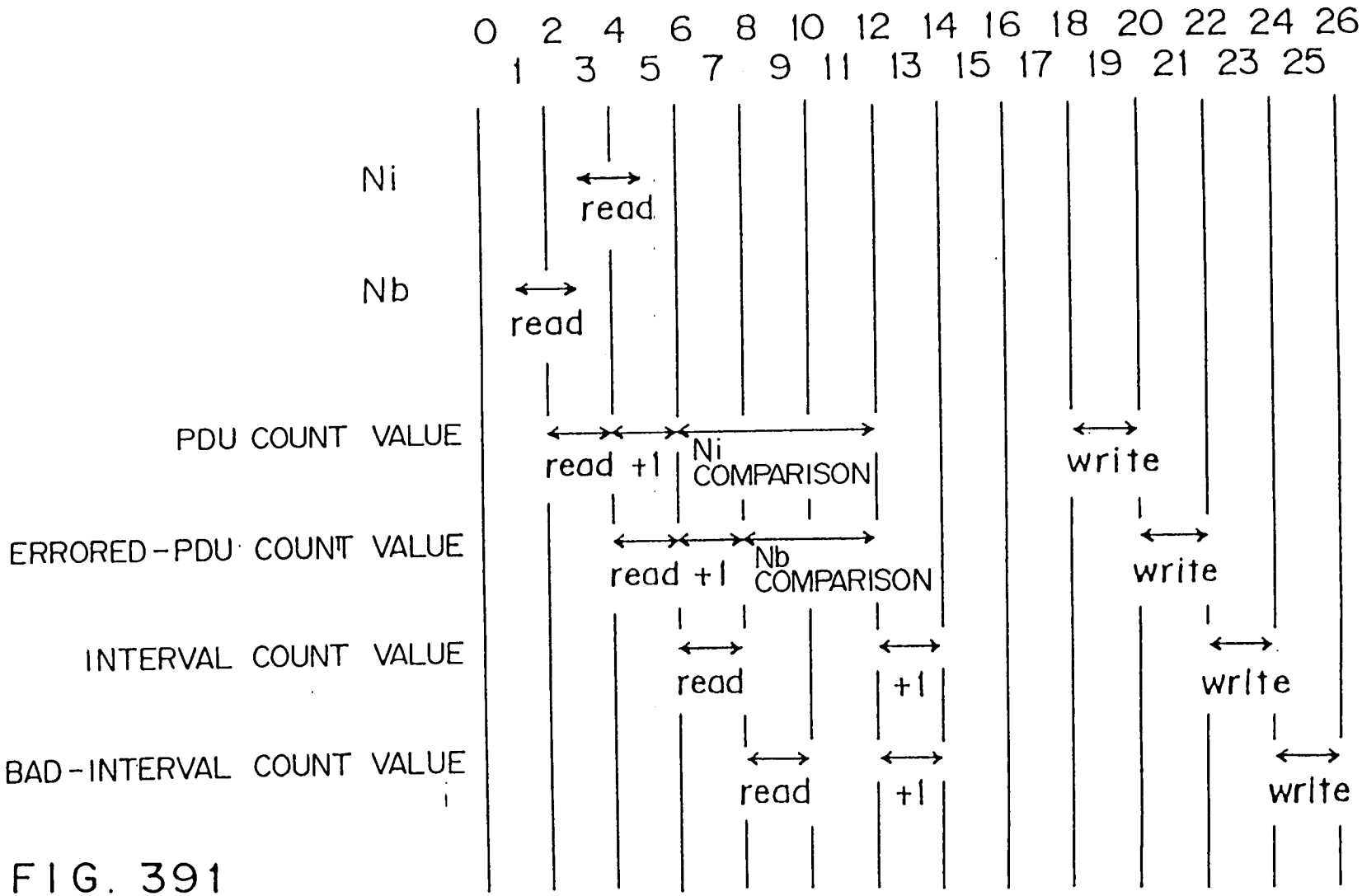

0 2 4 6 8 10 12 14 16 18 20 22 24 26
1 3 5 7 9 11 13 15 17 19 21 23 25
Ni
read
Nb
read
PDU COUNT VALUE
read +1
Ni
COMPARISON
write
ERRORED-PDU COUNT VALUE
read +1
Nb
COMPARISON
write
INTERVAL COUNT VALUE
read
+1
write
BAD-INTERVAL COUNT VALUE
read
+1
write

FIG. 391

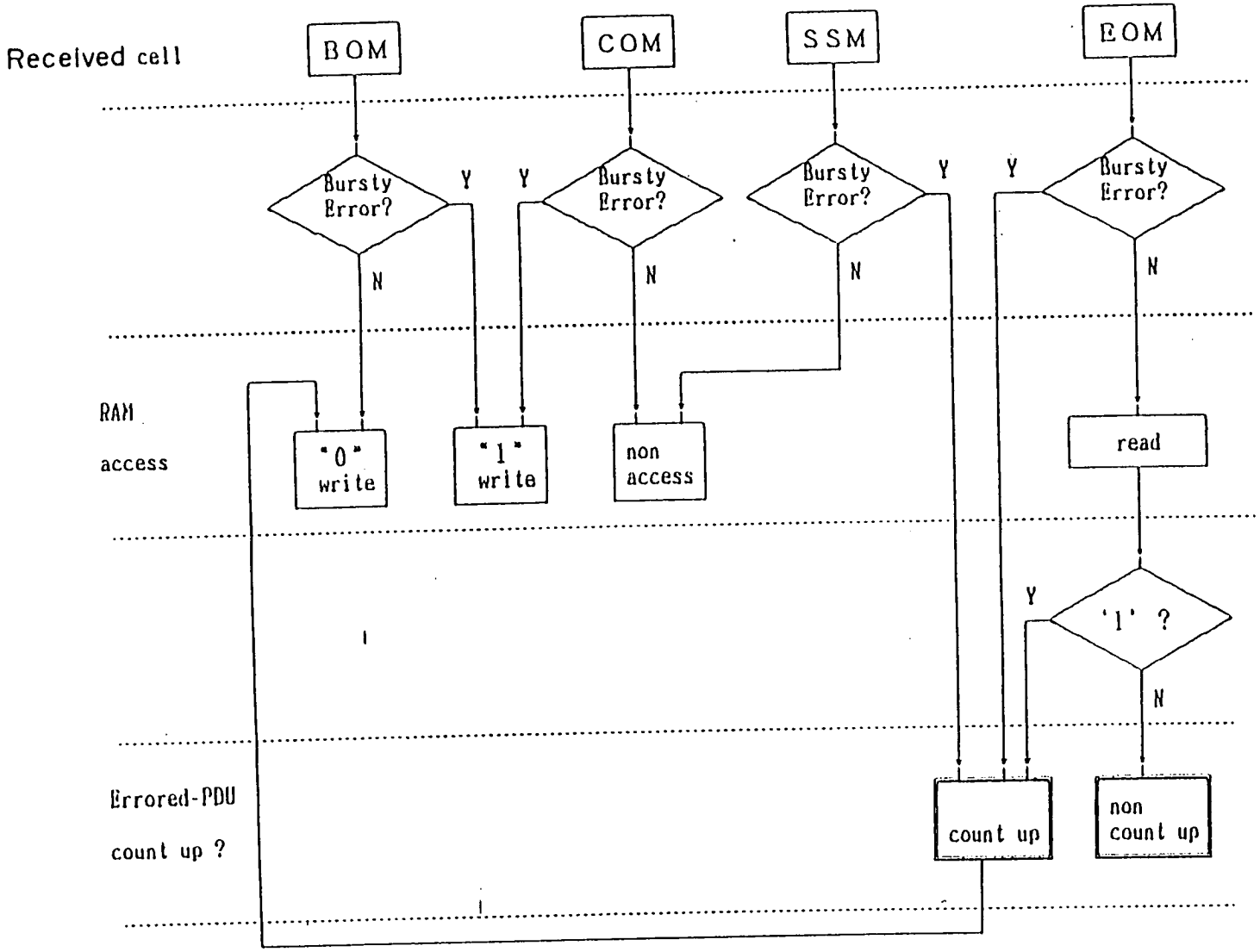

Received cell
BOM
COM
SSM
EOM
Bursty Error?
Y
N
RAM access
"0" write
"1" write
non access
read
'1' ?
Errored-PDU count up ?
count up
non count up

FIG. 392

GROUP	ITEM	SOURCE	LEVEL	CHECK	ACTION	NO
A	1	UNIQUE SPECIFICATION	L3	MRI TIME OUT	COUNT	1
	2	UNIQUE SPECIFICATION	.....	DEST. EQUAL TO ORG. SNI	————	2
B	1	UNIQUE SPECIFICATION	L2	PAYLOAD CRC VIOLATION	STOP COUNT	3
C	1	UNIQUE SPECIFICATION	L2	MID CURRENTLY ACTIVE	STOP COUNT	4
D	1	UNIQUE SPECIFICATION	L2	INVALID SEQUENCE NUMBER	STOP COUNT	5
E	1	NDC	L3	SA SCREENING VIOLATION	STOP COUNT LOG	6
	2	NDC	L3	DEST. SNI NOT AVAILABLE	STOP COUNT LOG	7
F	1	NDC	L3	EXCEED MAX. NUMBER OF CDU	STOP COUNT LOG	8
G	1	UNIQUE SPECIFICATION	L3	BETAG MISMATCH	STOP COUNT	9
H	1	UNIQUE SPECIFICATION	.....	MID ASSIGNED ERROR	COUNT	10
I	1	UNIQUE SPECIFICATION	.....	ENCAPSULATION ERROR	COUNT	11

FIG. 393

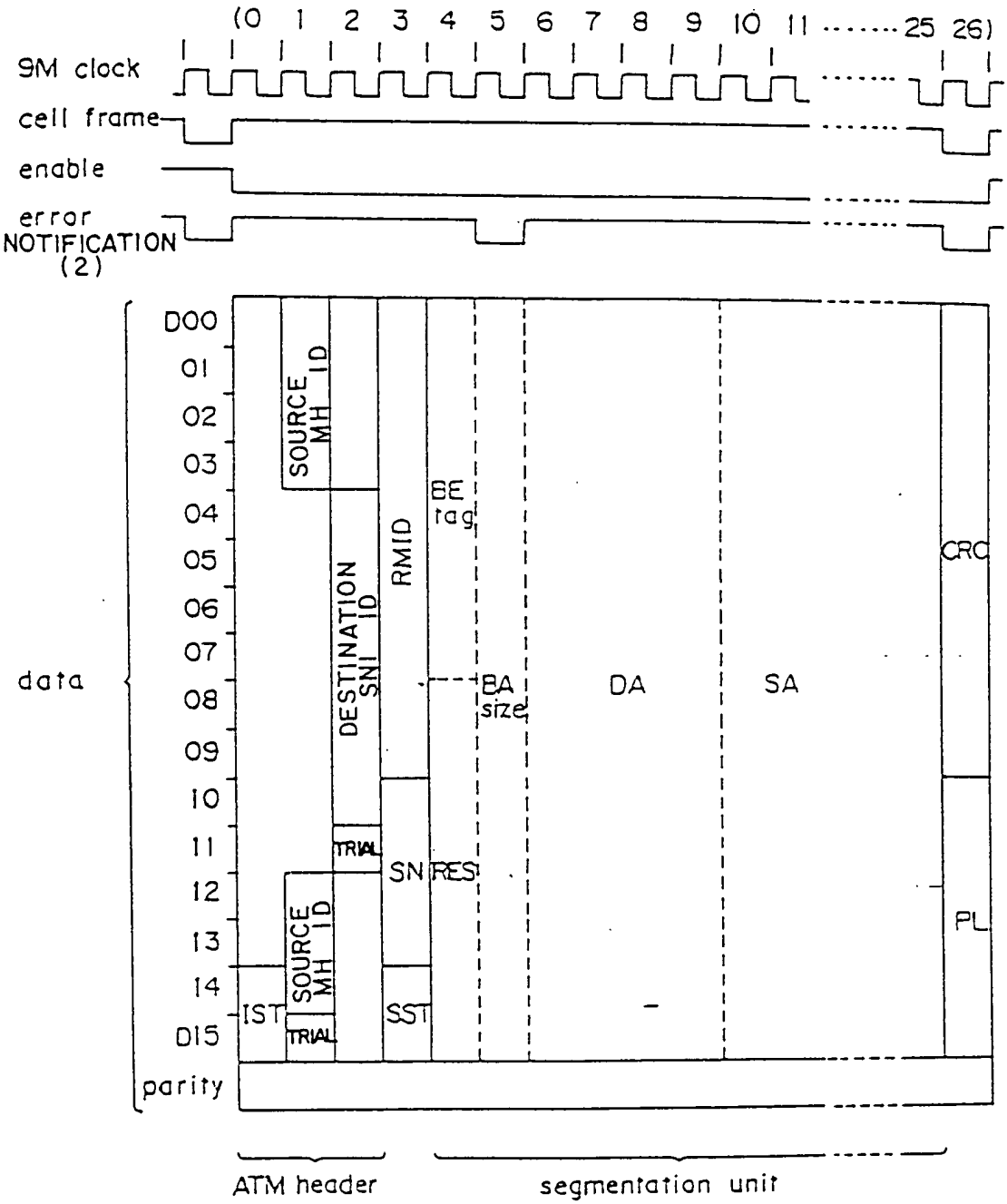

(0 1 2 3 4 5 6 7 8 9 10 11 ..... 25 26)
9M clock
cell frame
enable
error NOTIFICATION (2)
data
D00
01
02
03
04
05
06
07
08
09
10
11
12
13
14
D15
parity
SOURCE MH ID
DESTINATION SNI ID
RMID
BE tag
BA size
DA
SA
CRC
TRIAL
SN
RES
PL
IST
SOURCE MH ID
TRIAL
SST
ATM header
segmentation unit

FIG. 394

SIGNAL NAME	POLARITY	EXPLANATION
9M CLOCK	——	ALL SIGNALS OTHER THAN BASIC CLOCK CHANGE AT RISE OF THIS CLOCK
CELL FRAME	⇨	LAST 1τ OF SIGNAL CELL INDICATING BOUNDARY OF CELL ONLY INDICATES L.
ENABLE	⇨	SIGNAL INDICATING VALID/INVALID OF CELL ENTIRE CELL AREA INDICATES L WHEN VALID.
ERROR NOTIFICATION	⇨	SIGNAL INDICATING ERROR TYPE DESCRIBED LATER IN DETAIL.
DATA	+	16 PARALLEL DATA + PARITY ODD PARITY IN TOTAL 17 BITS OF 16 BIT PARALLEL DATA + ENABLE.

FIG. 395

	IST	SST
Inter-BOM	1 0	1 0
SIP-BOM	0 0	1 0
COM	0 0	0 0
EOM	0 1	0 1
SIP-SSM	0 1	1 1

FIG. 396

6652E0 E7E7E60

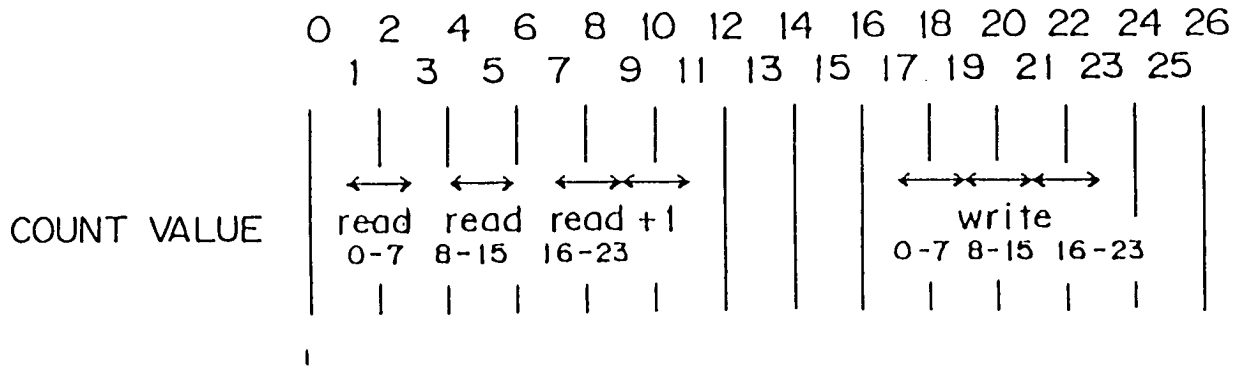


FIG. 397

6,592,629 B2

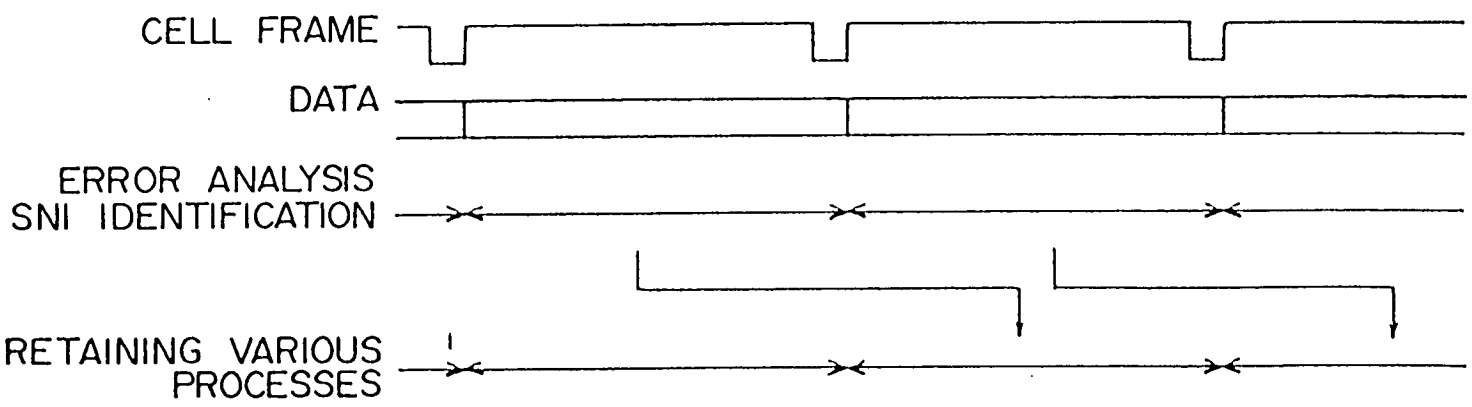


FIG. 398

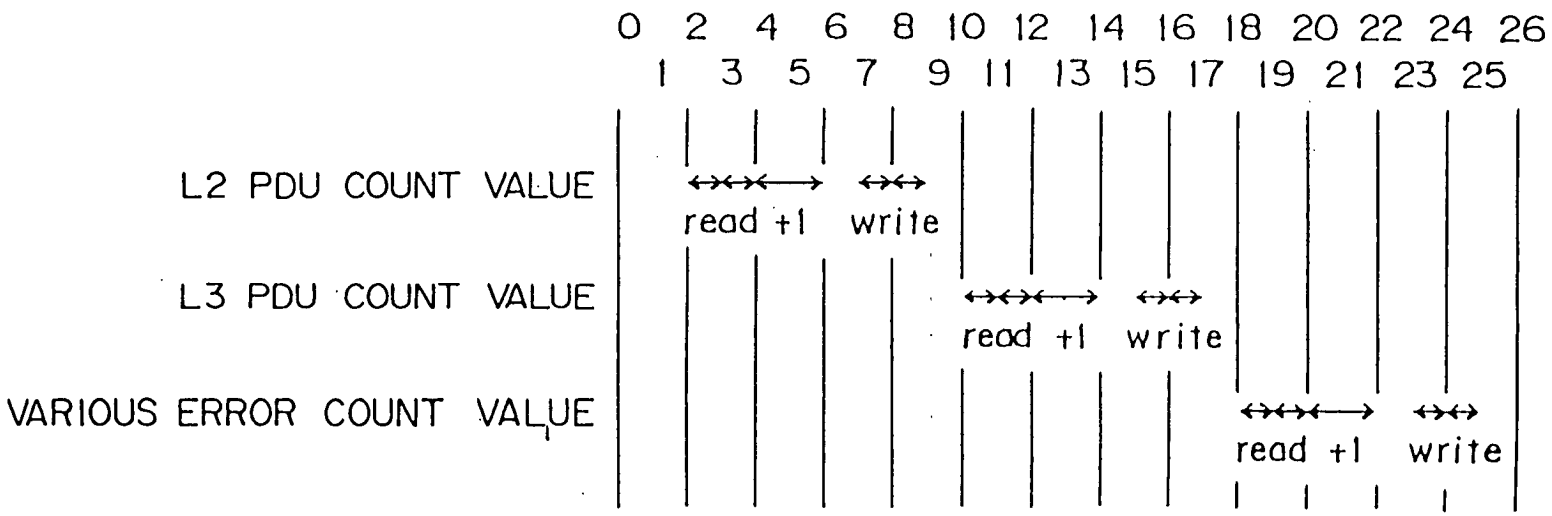

0 2 4 6 8 10 12 14 16 18 20 22 24 26
1 3 5 7 9 11 13 15 17 19 21 23 25
L2 PDU COUNT VALUE
read +1
write
L3 PDU COUNT VALUE
read +1
write
VARIOUS ERROR COUNT VALUE
read +1
write

FIG. 399

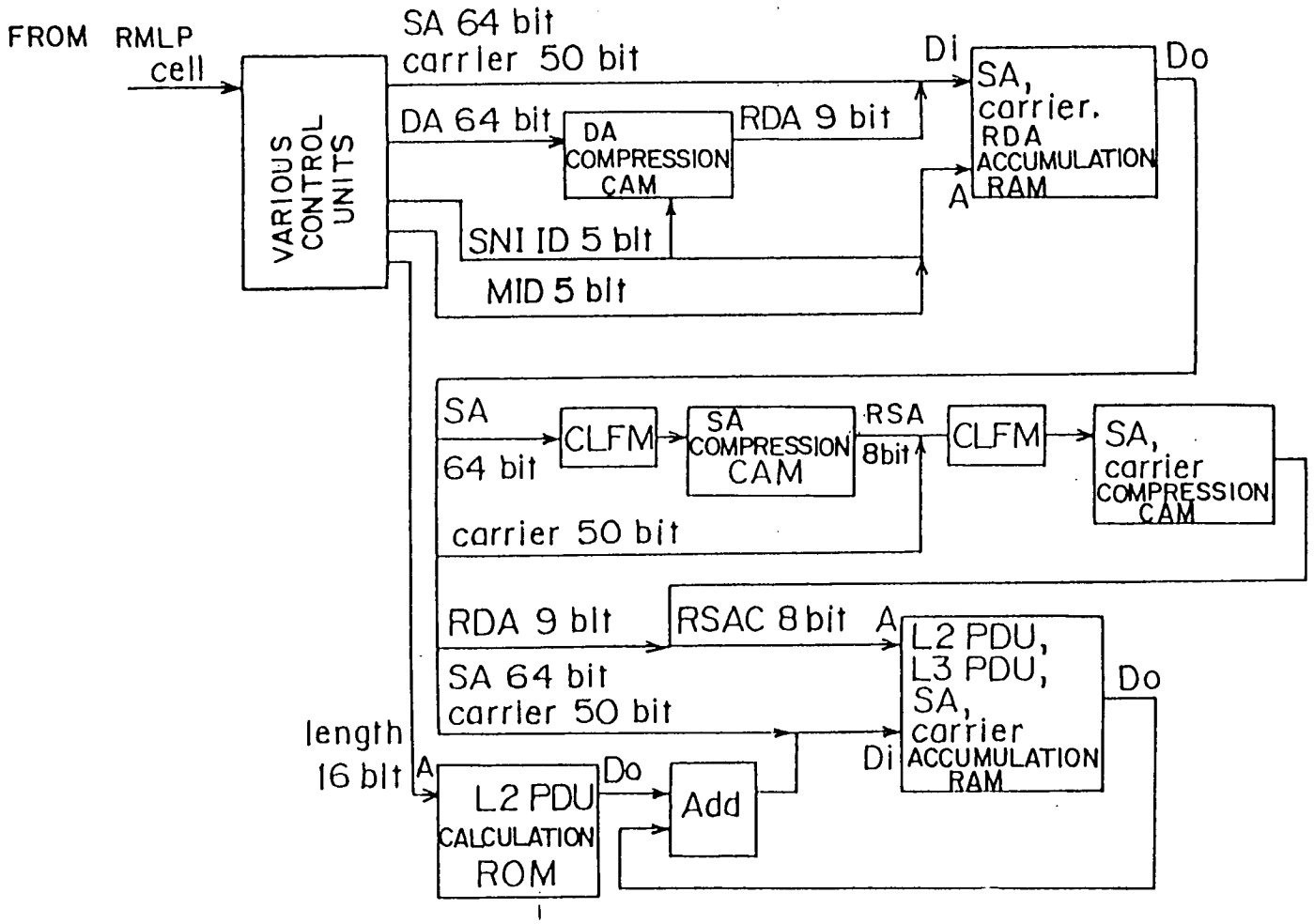

FROM RMLP
cell
VARIOUS CONTROL UNITS
SA 64 bit
carrier 50 bit
DA 64 bit
DA COMPRESSION CAM
RDA 9 bit
Di
SA, carrier. RDA ACCUMULATION RAM
Do
A
SNI ID 5 bit
MID 5 bit
SA
64 bit
CLFM
SA COMPRESSION CAM
RSA
8bit
CLFM
SA, carrier COMPRESSION CAM
carrier 50 bit
RDA 9 bit
RSAC 8 bit
A
SA 64 bit
carrier 50 bit
L2 PDU, L3 PDU, SA, carrier ACCUMULATION RAM
Do
Di
length
16 bit
A
L2 PDU CALCULATION ROM
Do
Add

FIG. 400

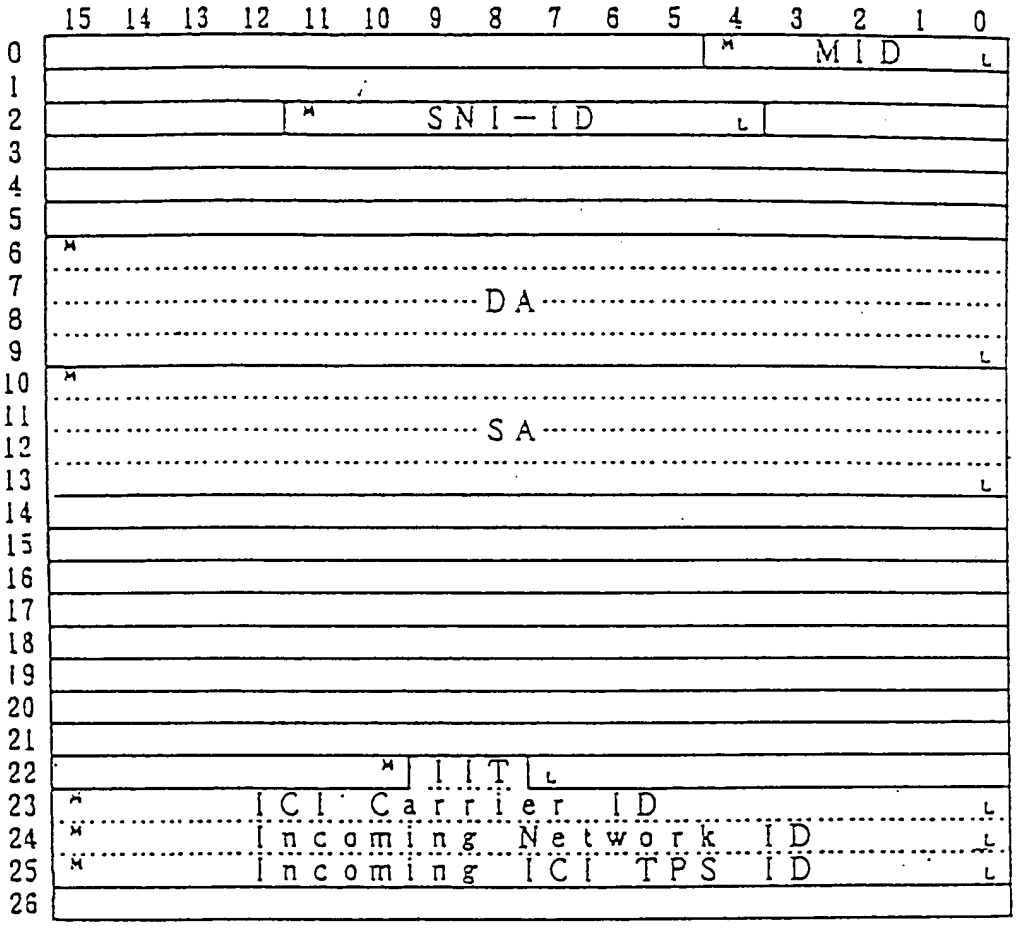

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
MID
SNI-ID
DA
SA
IIT
ICI Carrier ID
Incoming Network ID
Incoming ICI TPS ID

FIG. 401

6692E0 "E7E7260

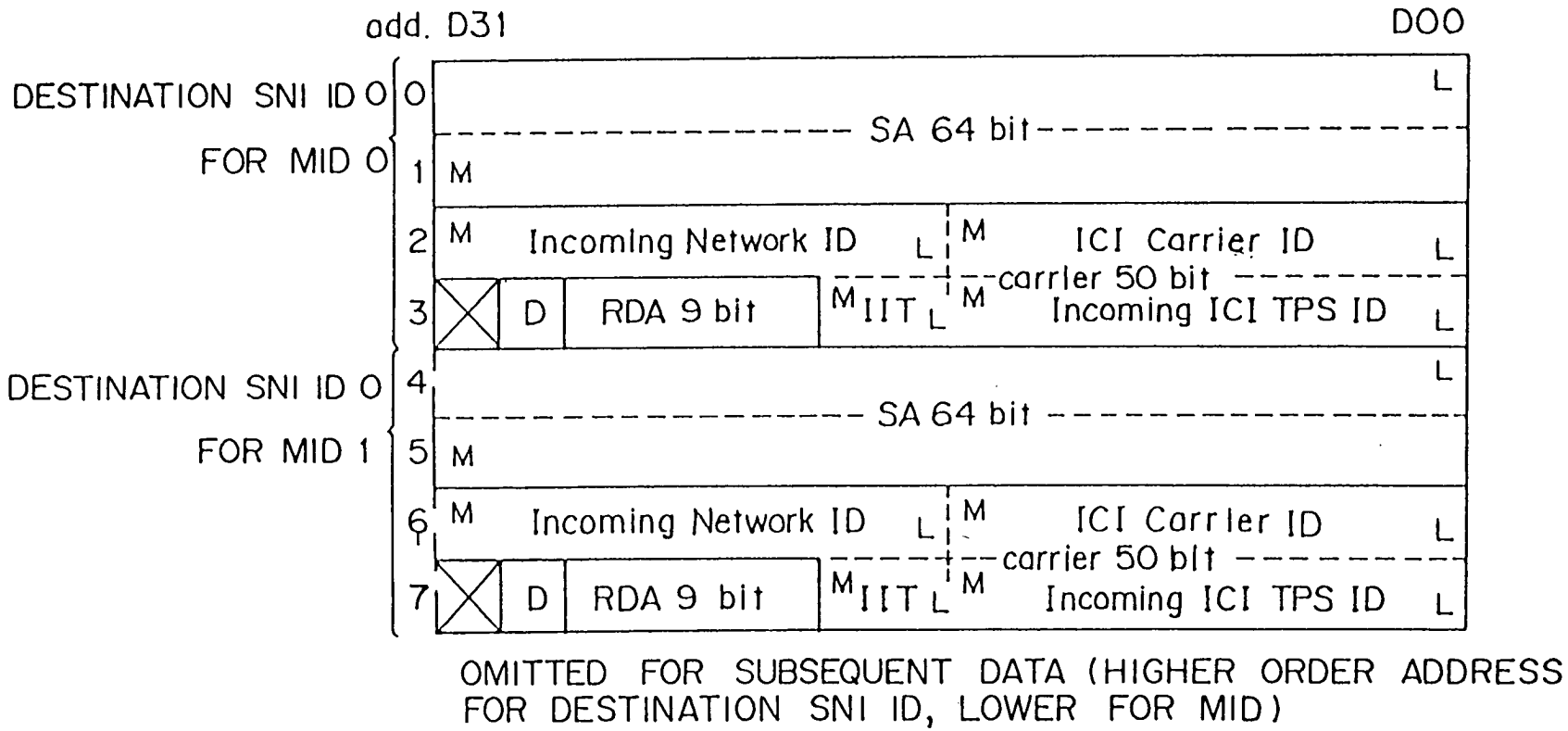


FIG. 402

6653:2742660

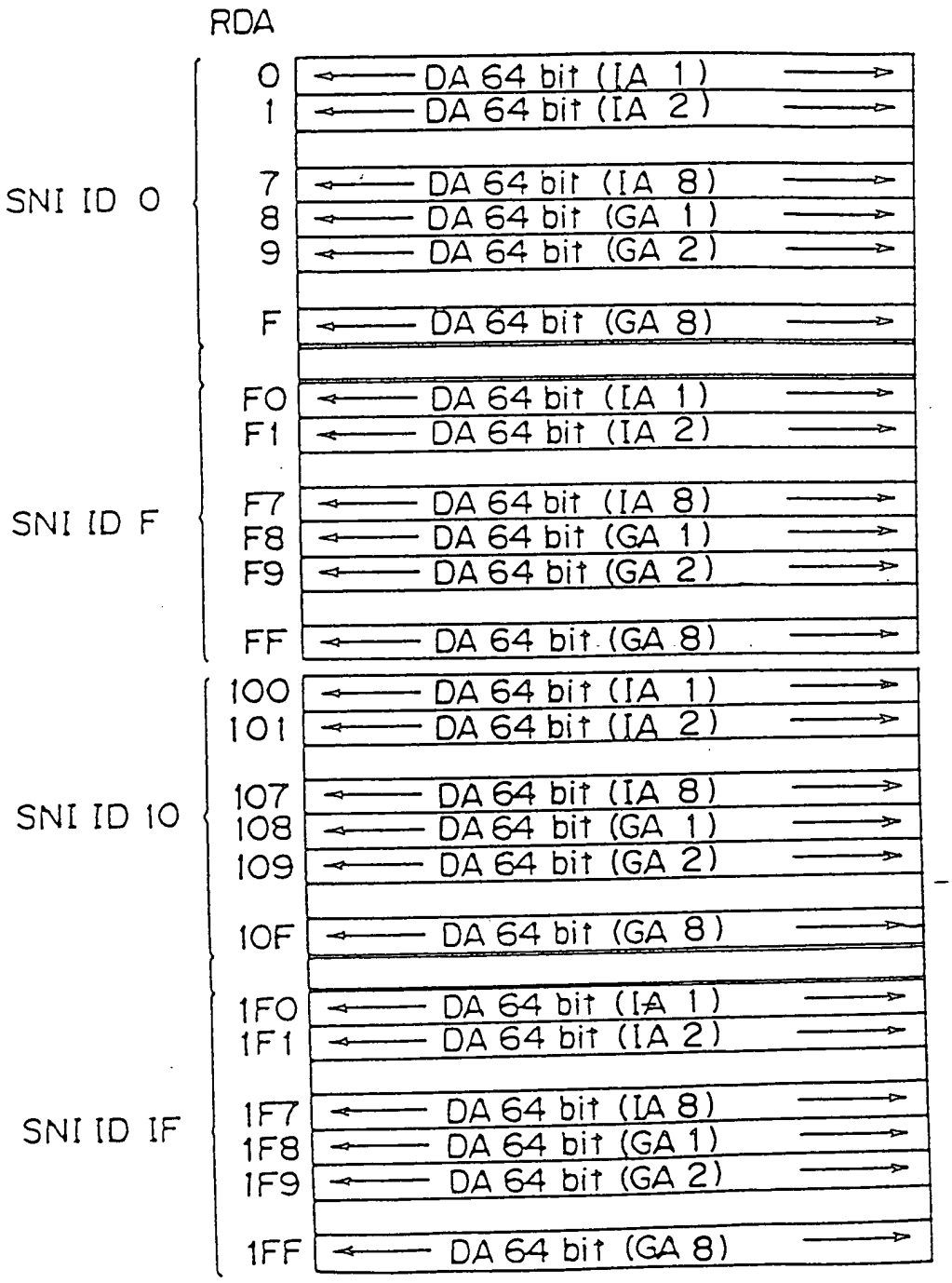


FIG. 403

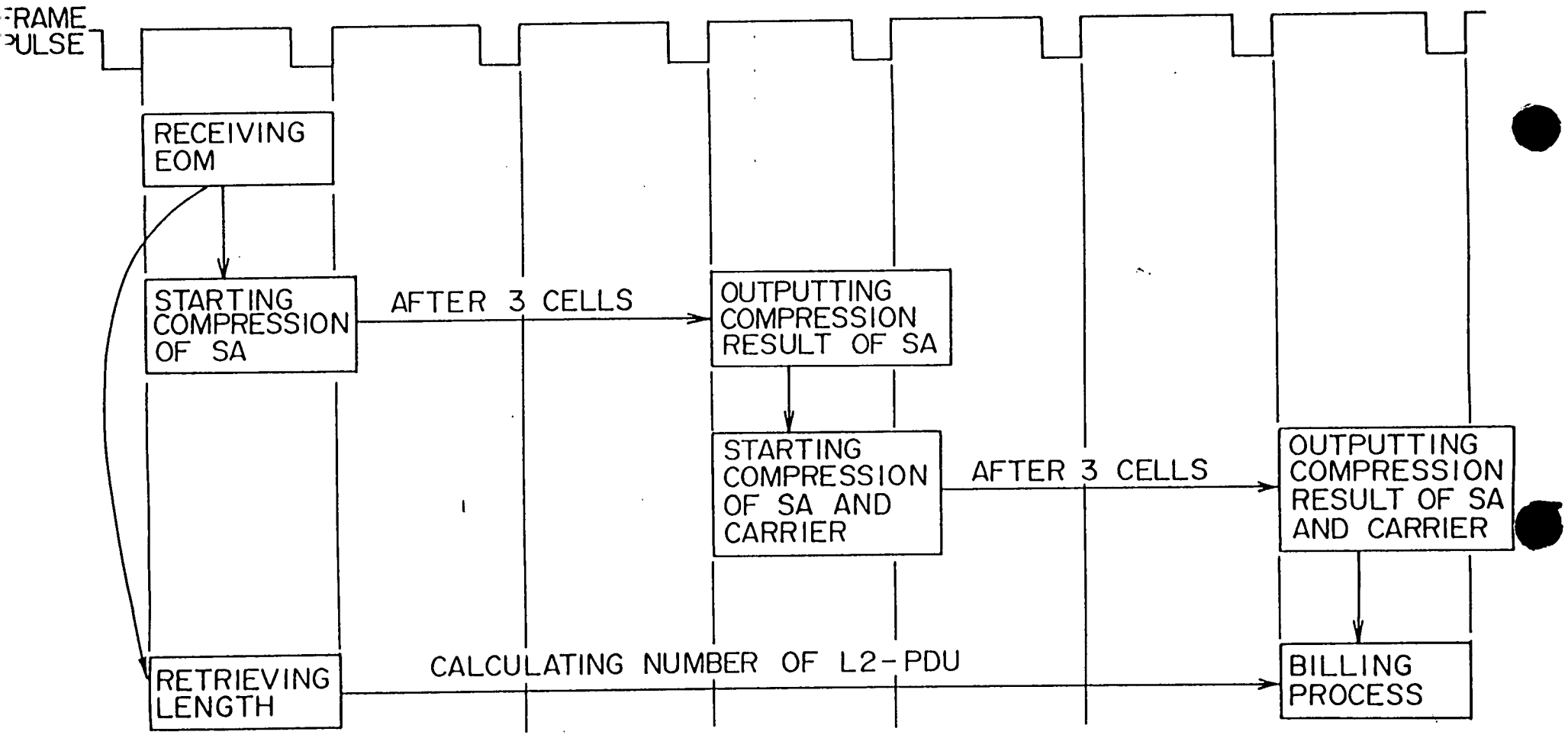

FRAME PULSE
RECEIVING EOM
STARTING COMPRESSION OF SA
AFTER 3 CELLS
OUTPUTTING COMPRESSION RESULT OF SA
STARTING COMPRESSION OF SA AND CARRIER
AFTER 3 CELLS
OUTPUTTING COMPRESSION RESULT OF SA AND CARRIER
RETRIEVING LENGTH
CALCULATING NUMBER OF L2-PDU
BILLING PROCESS

FIG. 404

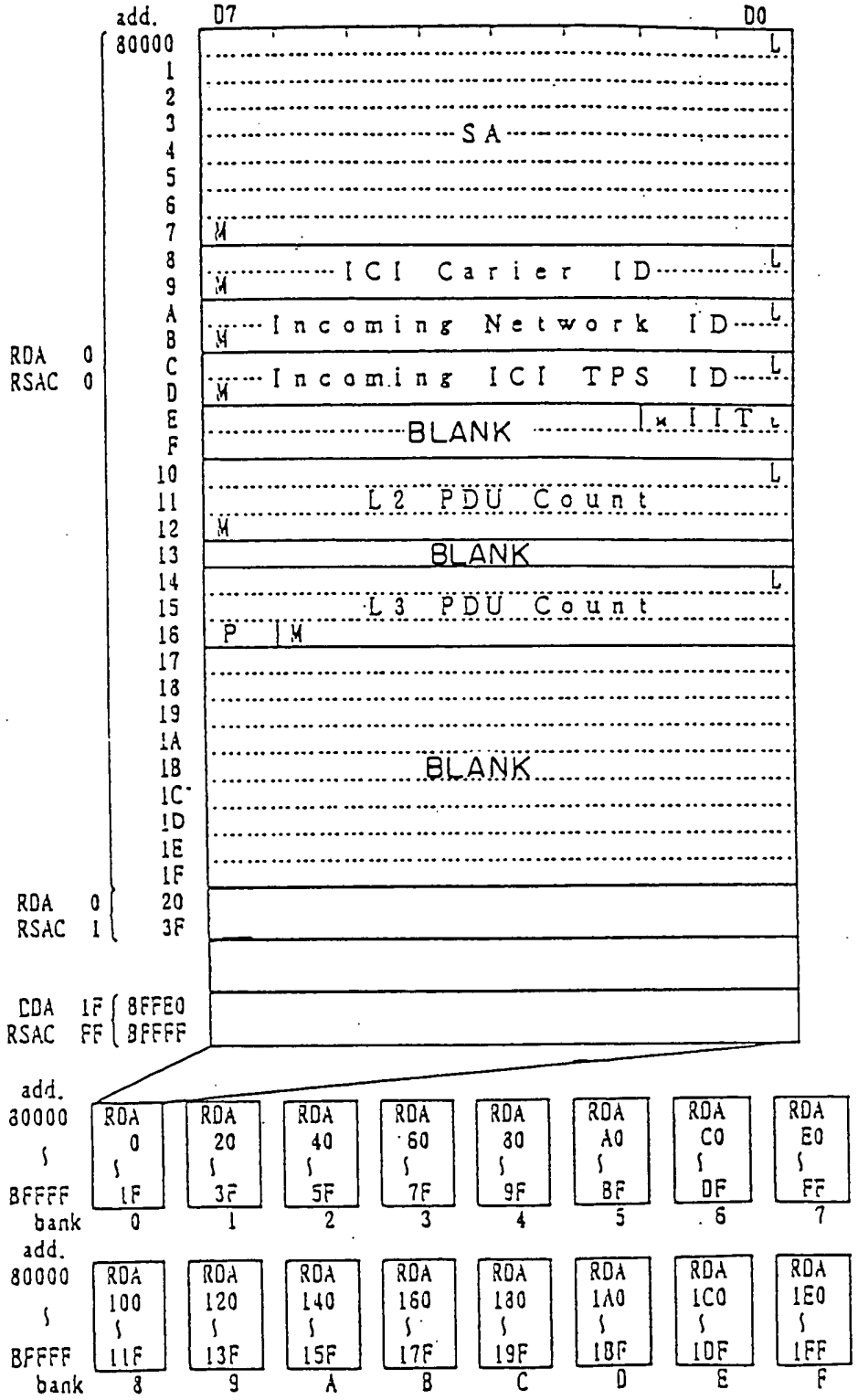

add.
D7
D0
80000
SA
ICI Carier ID
Incoming Network ID
Incoming ICI TPS ID
BLANK
L2 PDU Count
BLANK
L3 PDU Count
BLANK
RDA 0
RSAC 0
RDA 0
RSAC 1
CDA 1F
RSAC FF
8FFE0
8FFFF
BFFFF
bank
RDA 0
RDA 20
RDA 40
RDA 60
RDA 80
RDA A0
RDA C0
RDA E0
RDA 100
RDA 120
RDA 140
RDA 160
RDA 180
RDA 1A0
RDA 1C0
RDA 1E0

FIG. 405

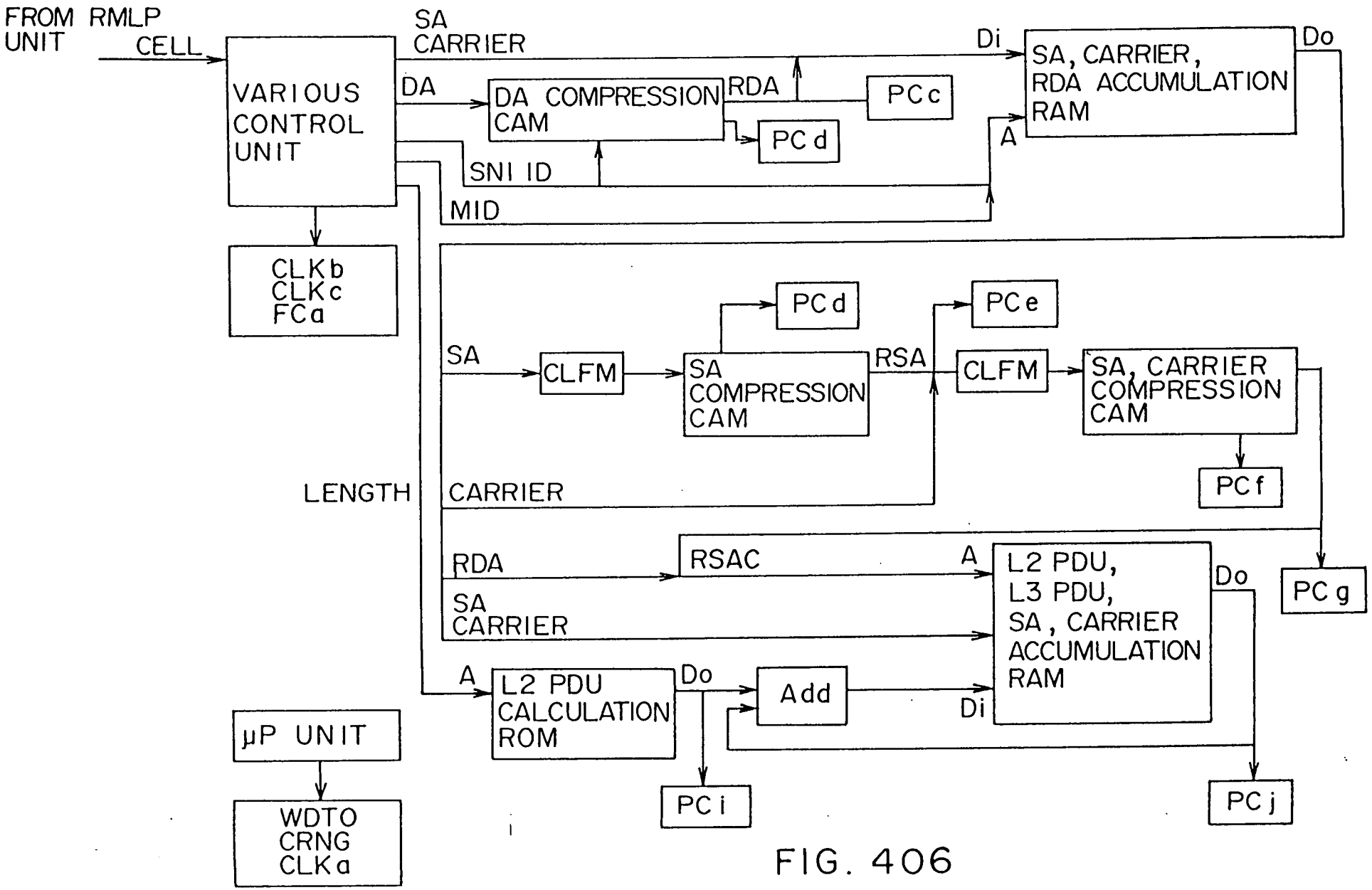

FROM RMLP UNIT
CELL
VARIOUS CONTROL UNIT
SA CARRIER
DA
DA COMPRESSION CAM
RDA
PCc
PCd
SNI ID
MID
Di
SA, CARRIER, RDA ACCUMULATION RAM
Do
A
CLKb
CLKc
FCa
SA
CLFM
SA COMPRESSION CAM
PCd
RSA
PCe
CLFM
SA, CARRIER COMPRESSION CAM
PCf
LENGTH
CARRIER
RDA
RSAC
A
L2 PDU, L3 PDU, SA, CARRIER ACCUMULATION RAM
Do
PCg
SA
CARRIER
A
L2 PDU CALCULATION ROM
Do
Add
Di
μP UNIT
WDTO
CRNG
CLKa
PCi
PCj

FIG. 406

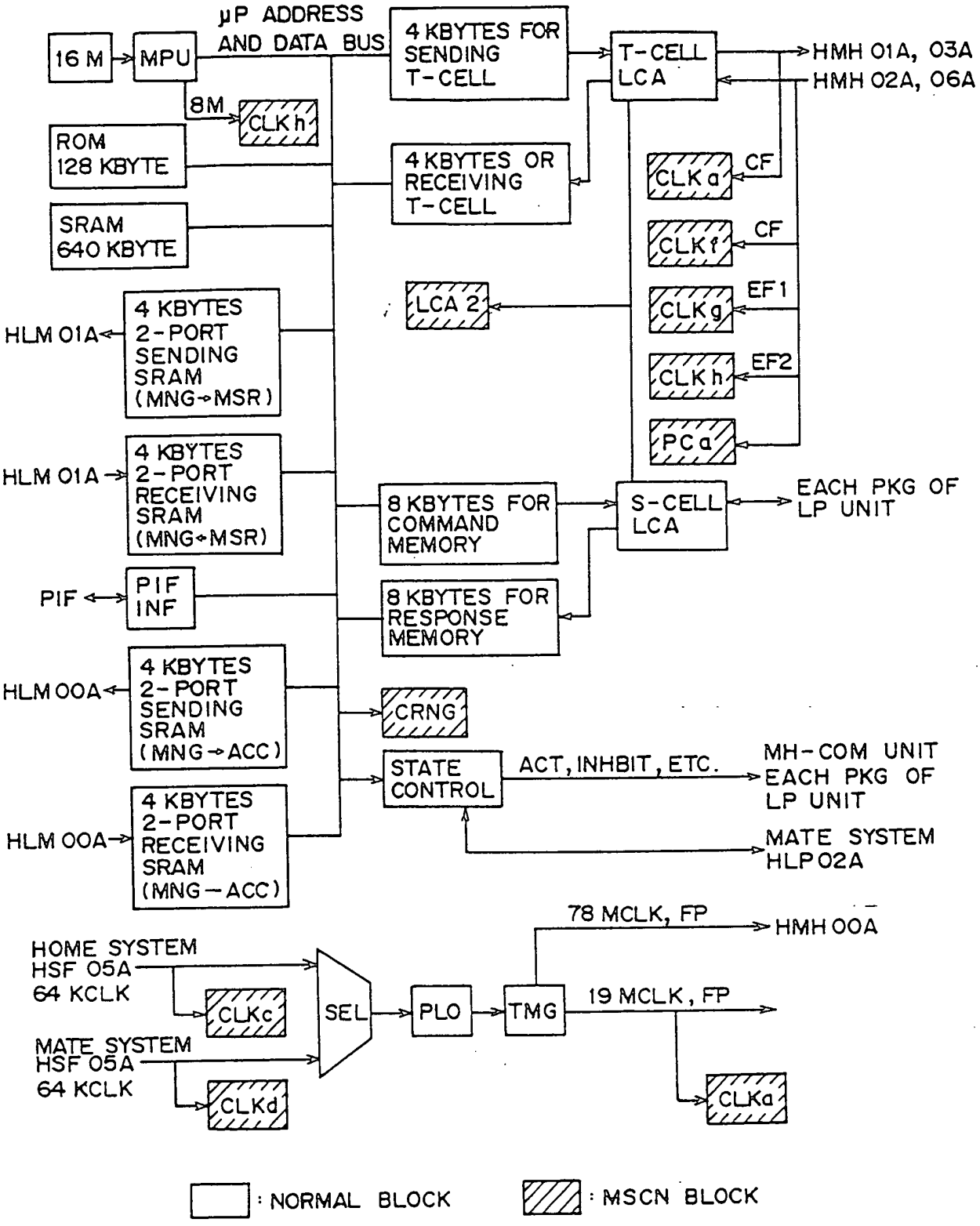

16 M
MPU
μP ADDRESS AND DATA BUS
8M
CLK h
ROM 128 KBYTE
SRAM 640 KBYTE
4 KBYTES FOR SENDING T-CELL
4 KBYTES OR RECEIVING T-CELL
T-CELL LCA
HMH 01A, 03A
HMH 02A, 06A
CLK a
CF
CLK f
CF
LCA 2
CLK g
EF1
CLK h
EF2
PC a
HLM 01A
4 KBYTES 2-PORT SENDING SRAM (MNG→MSR)
HLM 01A
4 KBYTES 2-PORT RECEIVING SRAM (MNG→MSR)
8 KBYTES FOR COMMAND MEMORY
S-CELL LCA
EACH PKG OF LP UNIT
PIF
PIF INF
8 KBYTES FOR RESPONSE MEMORY
HLM 00A
4 KBYTES 2-PORT SENDING SRAM (MNG→ACC)
CRNG
STATE CONTROL
ACT, INHBIT, ETC.
MH-COM UNIT EACH PKG OF LP UNIT
MATE SYSTEM HLP 02A
HLM 00A
4 KBYTES 2-PORT RECEIVING SRAM (MNG—ACC)
78 MCLK, FP
HMH 00A
HOME SYSTEM HSF 05A 64 KCLK
CLKc
SEL
PLO
TMG
19 MCLK, FP
MATE SYSTEM HSF 05A 64 KCLK
CLKd
CLKa
: NORMAL BLOCK
: MSCN BLOCK

FIG. 407

BLOCK NAME	FUNCTION
16M	GENERATING 16 MHZ CLOCK FOR MICROPROCESSOR
MPU	μP (80C186)
ROM	STORING FIRMWARE FOR MPU
FOR SENDING T-CELL	TEST CELL SENDING MEMORY
FOR RECEIVING T-CELL	TEST CELL RECEIVING MEMORY
T-CELL LCA	SENDING TEST CELL FOR HMH01A AND 03A (ASSIGNING ODD PARITY AND ADJUSTING TIMIGN), RECEIVING TEST CELL, MAKING PARITY CHECK, ETC.
SRAM	WORK MEMORY FOR MPU
2-PORT SENDING SRAM MNG → MSR	DATA SENDING MEMORY FOR MSR-FIRM
2-PORT RECEIVING SRAM MNG← MSR	DATA RECEIVING MEMORY FROM MSR-FIRM
2-PORT SENDING SRAM MNG → ACC	DATA SENDING MEMORY FOR ACC-FIRM
2-PORT RECEIVING SRAM MNG← ACC	DATA RECEIVING MEMORY FROM ACC-FIRM
PIF inf	CONTROLLING INTERFACE WITH PIF (SBIF-LSI)
FOR COMMAND MEMORY	SRAM FOR SENDING COMMAND
FOR RESPONSE MEMORY	SRAM FOR RECEIVING RESPONSE
S-CTL LCA	COMMAND AND RESPONSE CONTROL FOR LP
STATE CONTROL	CONTROLLING ACT, INHBIT, ETC. OUS CONTROL TO MATE SYSTEM
SEL	SELECTING 64 KHZ CLOCK FROM MH-COM OF HOME AND MATE SYSTEMS
PLO	GENERATING 155 MHZ CLOCK IN SYNCHRONISM WITH 64 KHZ CLOCK
TMG	GENERATING 78 MHZ AND 19 MHZ CLOCKS FROM 155 MHZ CLOCK

FIG. 408

BLOCK NAME	F U N C T I O N
C L K b	DISCONNECTING 8 M CLOCK FOR μP OPERATION
C L K e	DISCONNECTING SENDING CELL FRAME (COMMON TO SMLP AND RMLP)
C L K f	DISCONNECTING RECEIVING CELL FRAME(COMMON TO SMLP AND RMLP)
C L K g	DISCONNECTING ERROR FLAG-1(COMMON TO SMLP AND RMLP)
C L K h	DISCONNECTING ERROR FLAG-2(COMMON TO SMLP AND RMLP)
P C a	RECEIVING CELL DATA PARITY NG(COMMON TO SMLP AND RMLP)
L C A 2	HLP02A LCA CONFIGURATION NG
C R N G	ABNORMAL COMMAND AND RESPONSE IN S-CTL1
C L K c	DISCONNECTING 64 K HOME SYSTEM CLOCK
C L K d	DISCONNECTING 64 K MATE SYSTEM CLOCK
C L K a	DISCONNECTING 19 M CLOCK/FRAME PULSE

F I G. 4 0 9

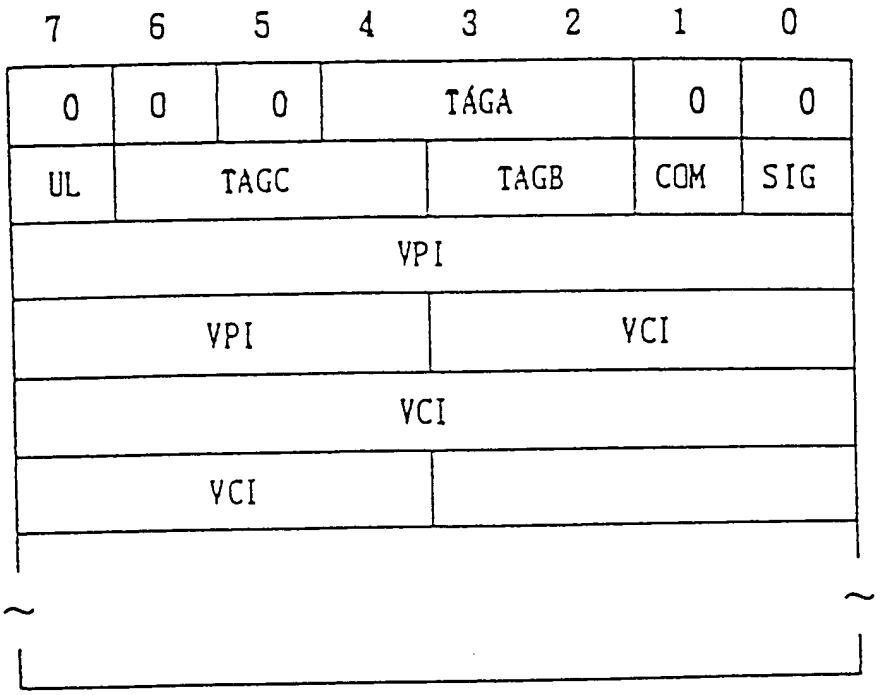


FIG. 410

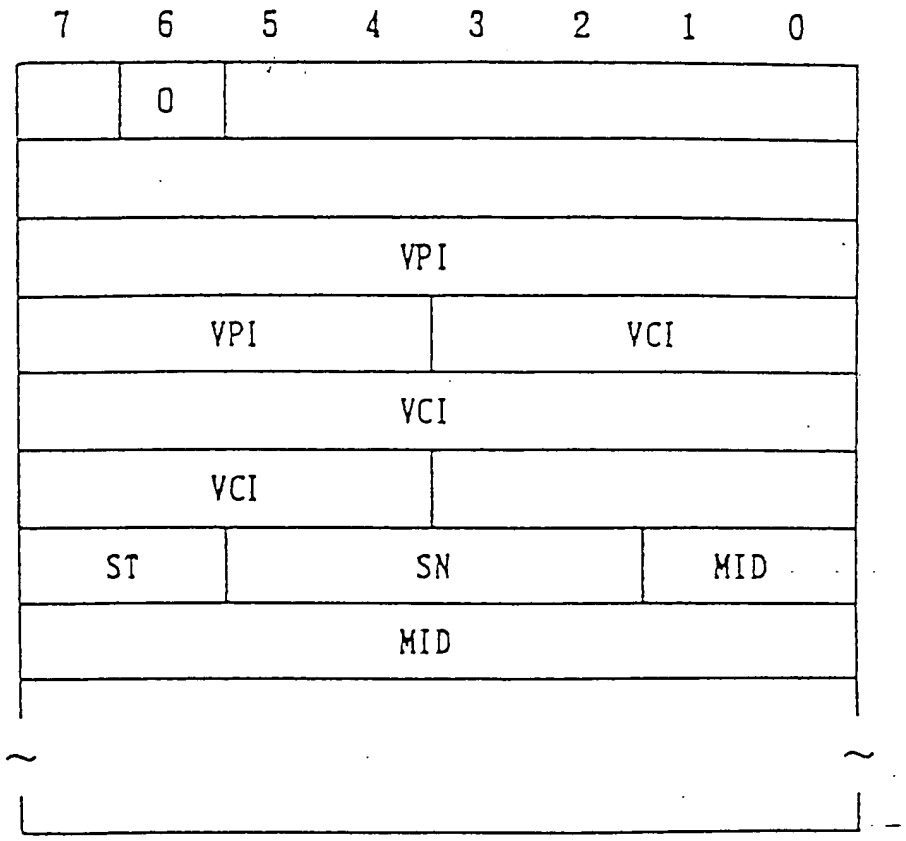


FIG. 411

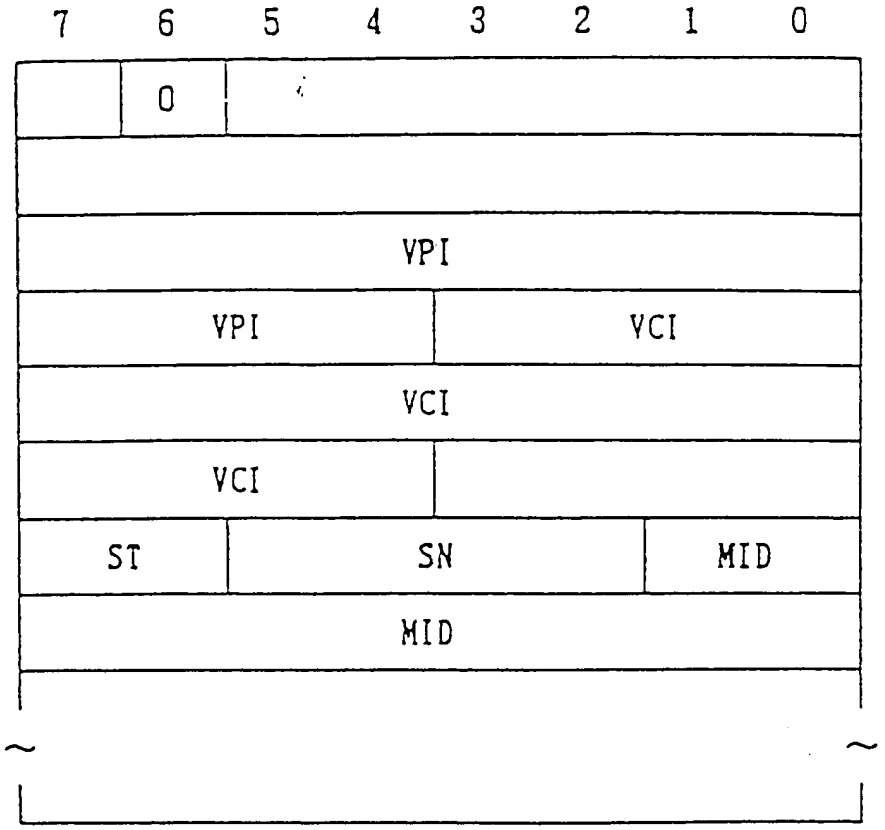


FIG. 412

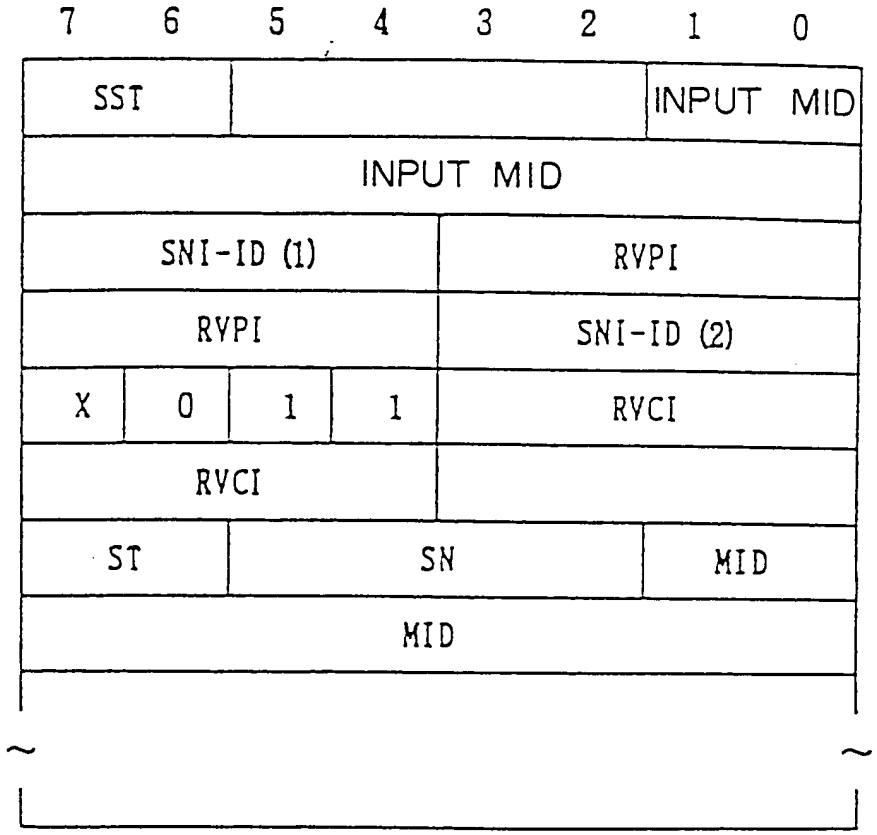

7 6 5 4 3 2 1 0
SST
INPUT MID
INPUT MID
SNI-ID (1)
RVPI
RVPI
SNI-ID (2)
X
0
1
1
RVCI
RVCI
ST
SN
MID
MID

FIG. 413

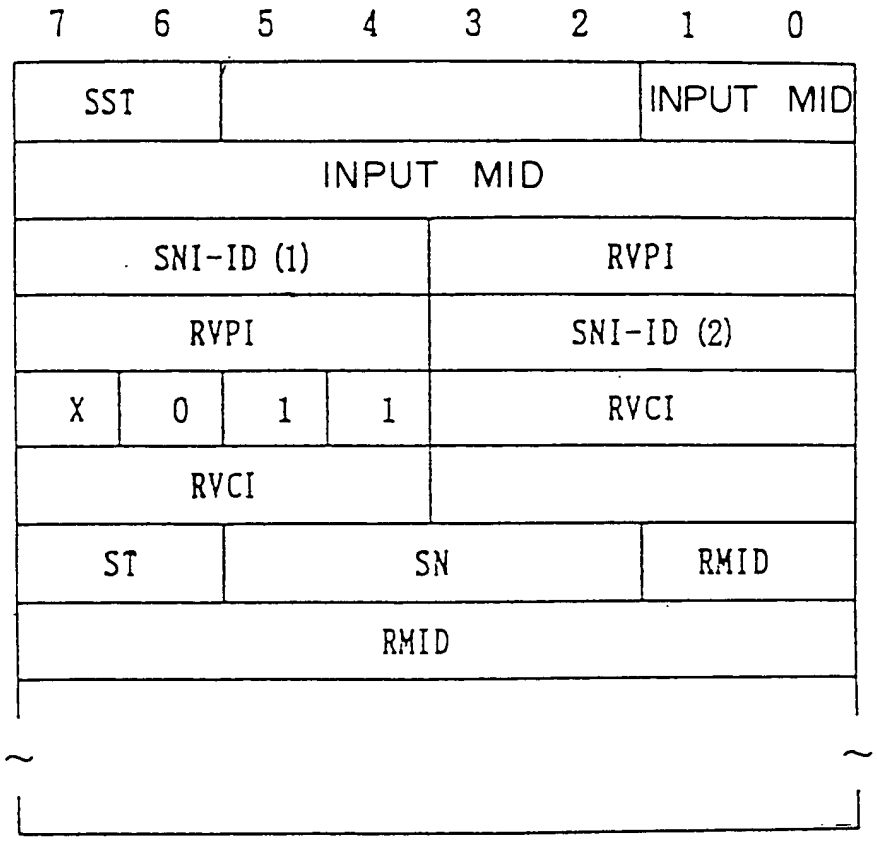

7 6 5 4 3 2 1 0
SST
INPUT MID
INPUT MID
SNI-ID (1)
RVPI
RVPI
SNI-ID (2)
X
0
1
1
RVCI
RVCI
ST
SN
RMID
RMID

FIG. 414

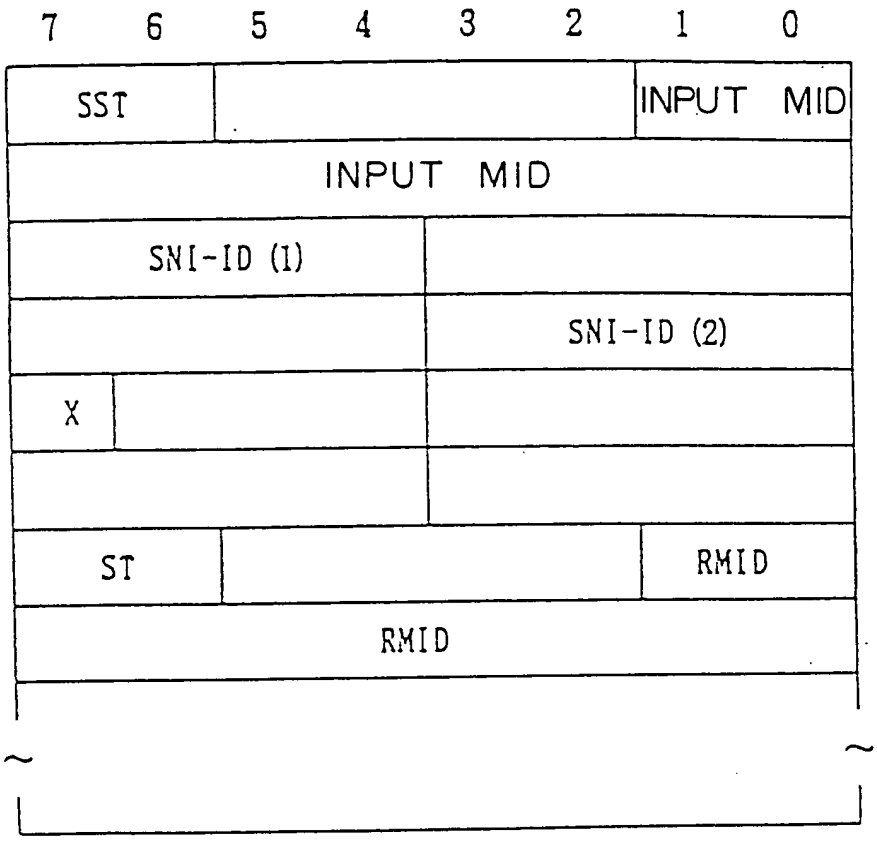

7 6 5 4 3 2 1 0
SST
INPUT MID
INPUT MID
SNI-ID (1)
SNI-ID (2)
X
ST
RMID
RMID

FIG. 415-

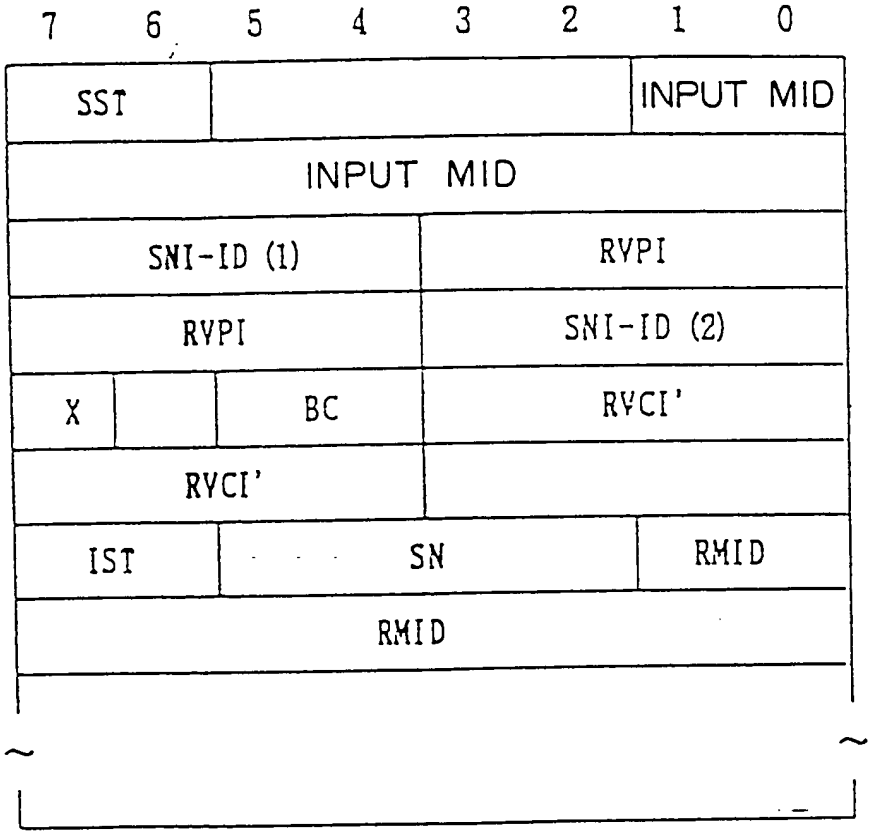

7 6 5 4 3 2 1 0
SST
INPUT MID
INPUT MID
SNI-ID (1)
RVPI
RVPI
SNI-ID (2)
X
BC
RVCI'
RVCI'
IST
SN
RMID
RMID

FIG. 416

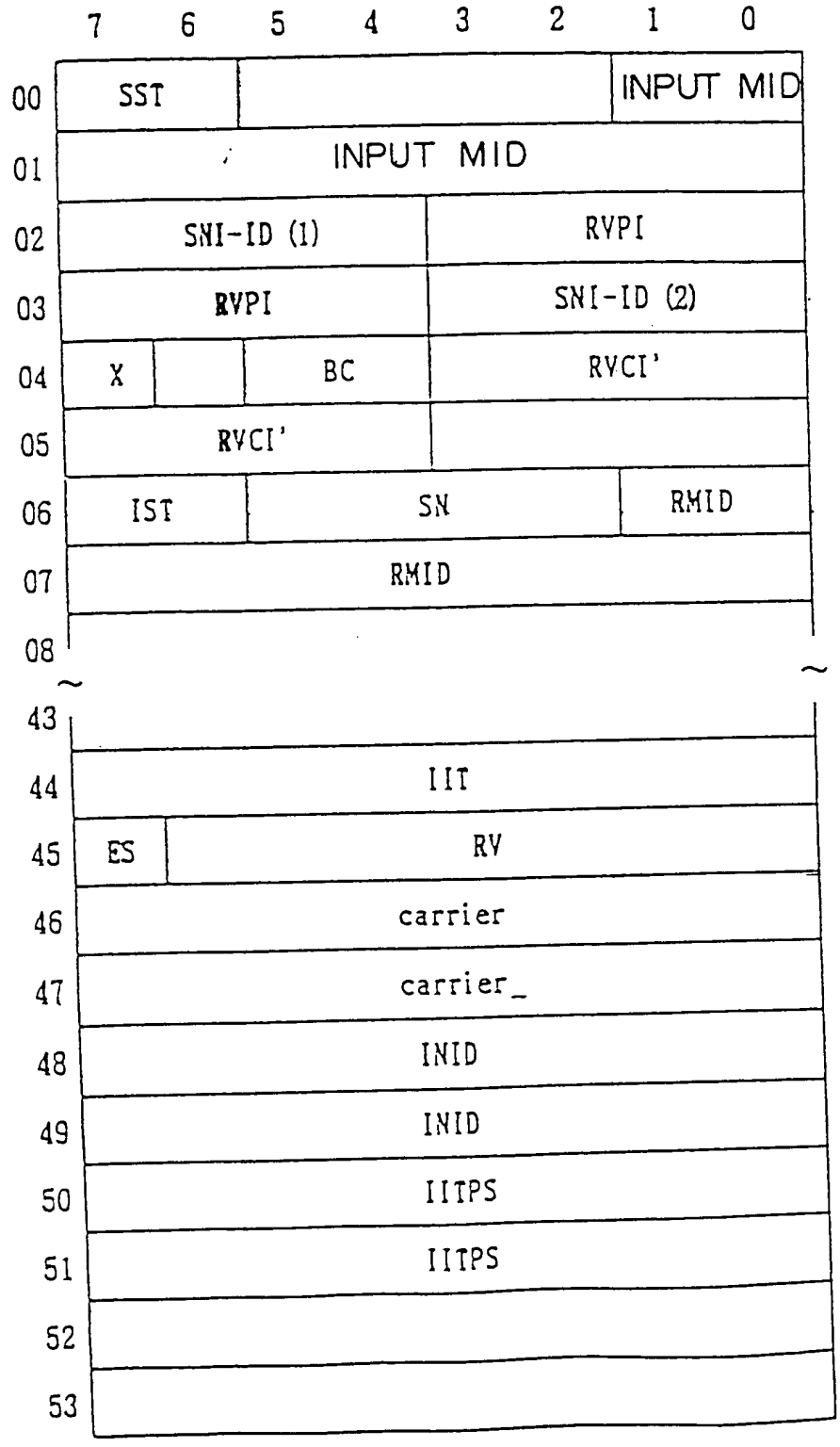

7 6 5 4 3 2 1 0
00 SST INPUT MID
01 INPUT MID
02 SNI-ID (1) RVPI
03 RVPI SNI-ID (2)
04 X BC RVCI'
05 RVCI'
06 IST SN RMID
07 RMID
08
43
44 IIT
45 ES RV
46 carrier
47 carrier_
48 INID
49 INID
50 IITPS
51 IITPS
52
53

FIG. 417

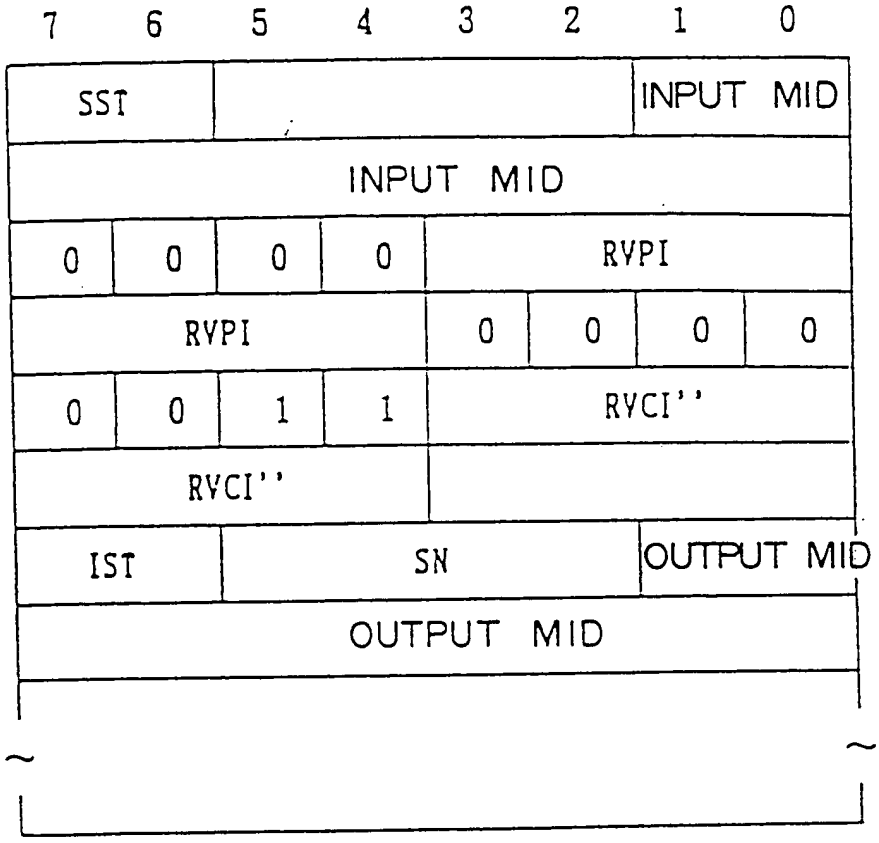

7 6 5 4 3 2 1 0
SST
INPUT MID
INPUT MID
0 0 0 0 RVPI
RVPI 0 0 0 0
0 0 1 1 RVCI''
RVCI''
IST SN OUTPUT MID
OUTPUT MID

FIG. 418

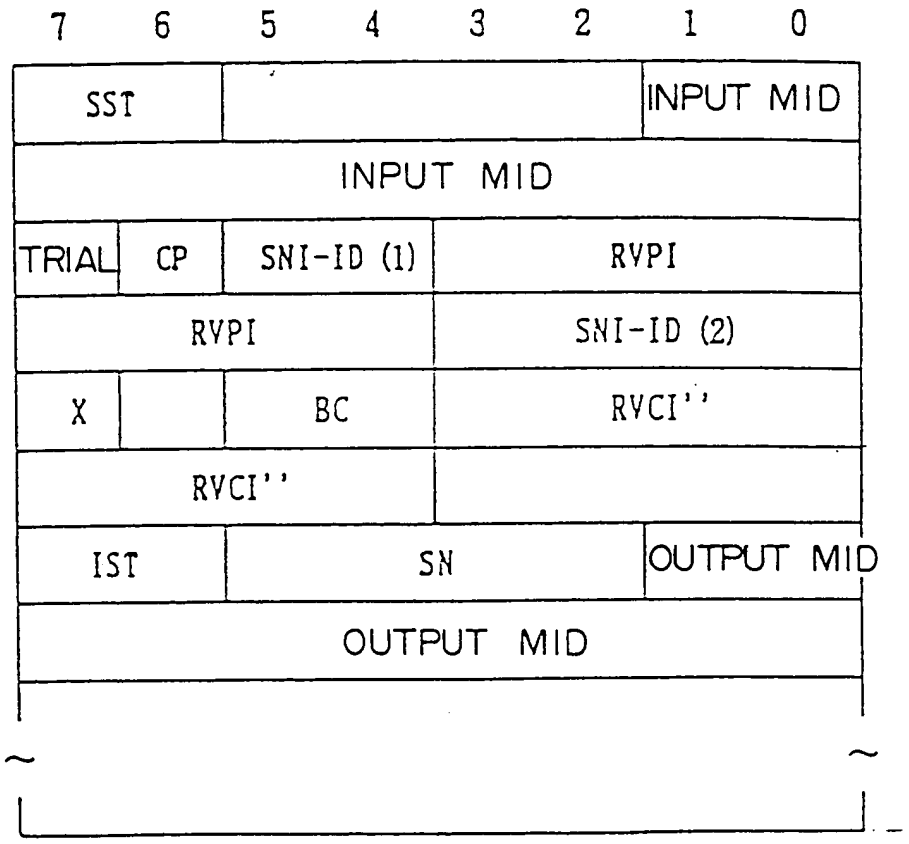

7 6 5 4 3 2 1 0
SST
INPUT MID
INPUT MID
TRIAL
CP
SNI-ID (1)
RVPI
RVPI
SNI-ID (2)
X
BC
RVCI''
RVCI''
IST
SN
OUTPUT MID
OUTPUT MID

FIG. 419

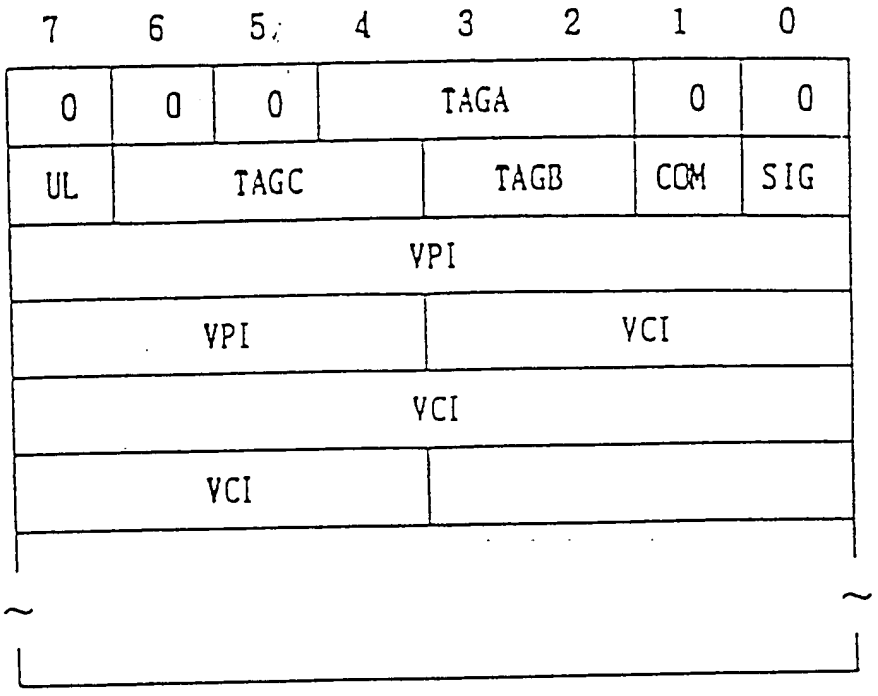


FIG. 420

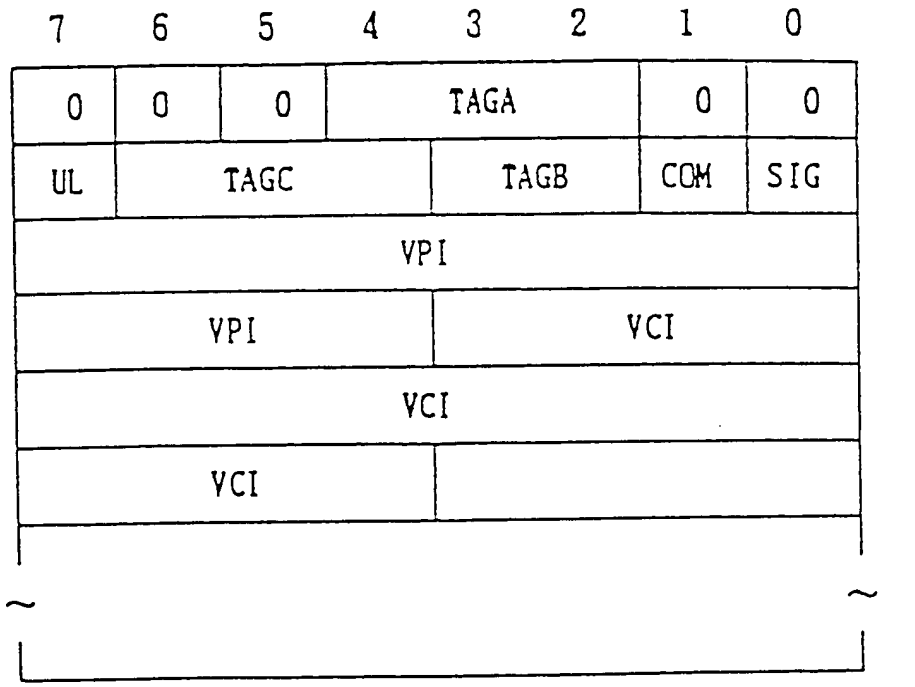


FIG. 421

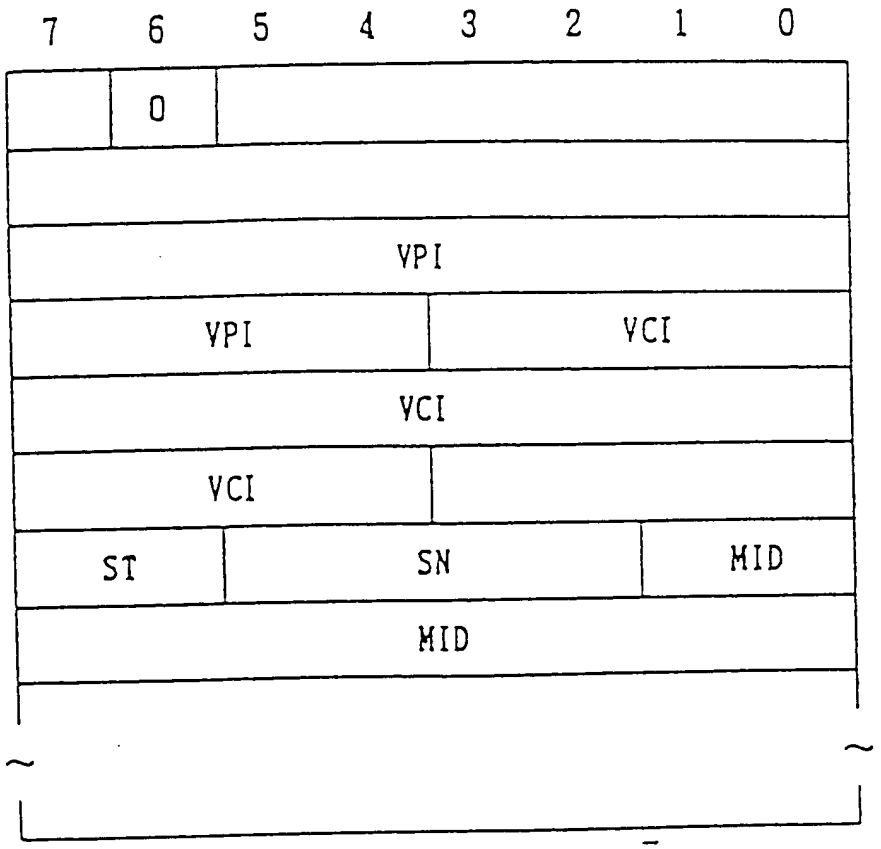


FIG. 422

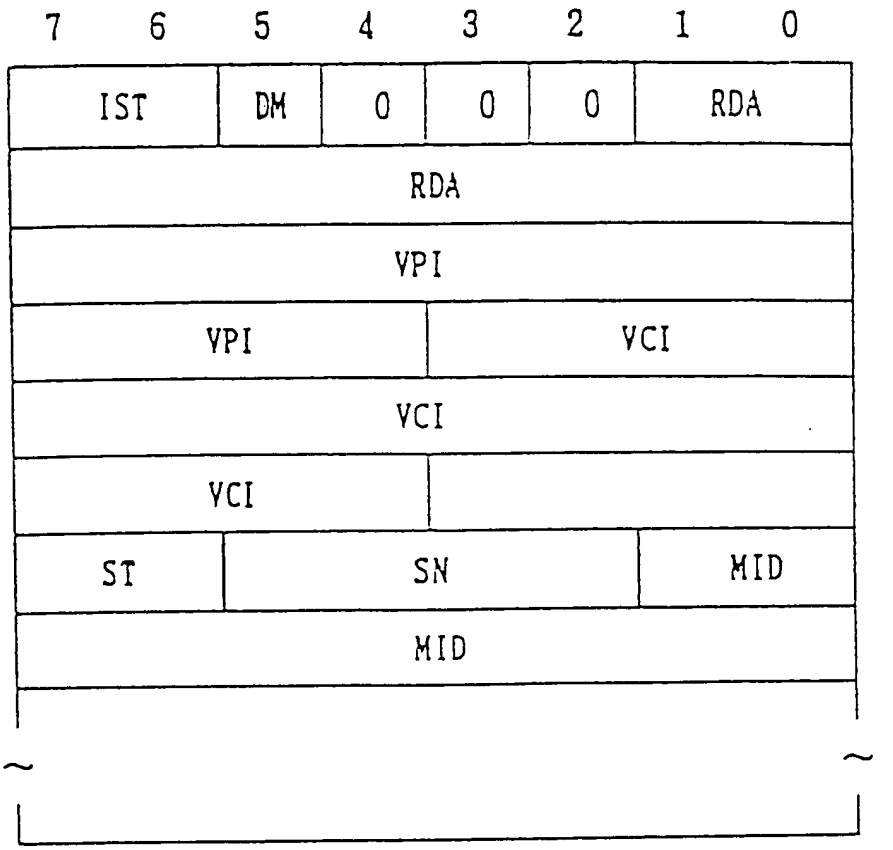


FIG. 423

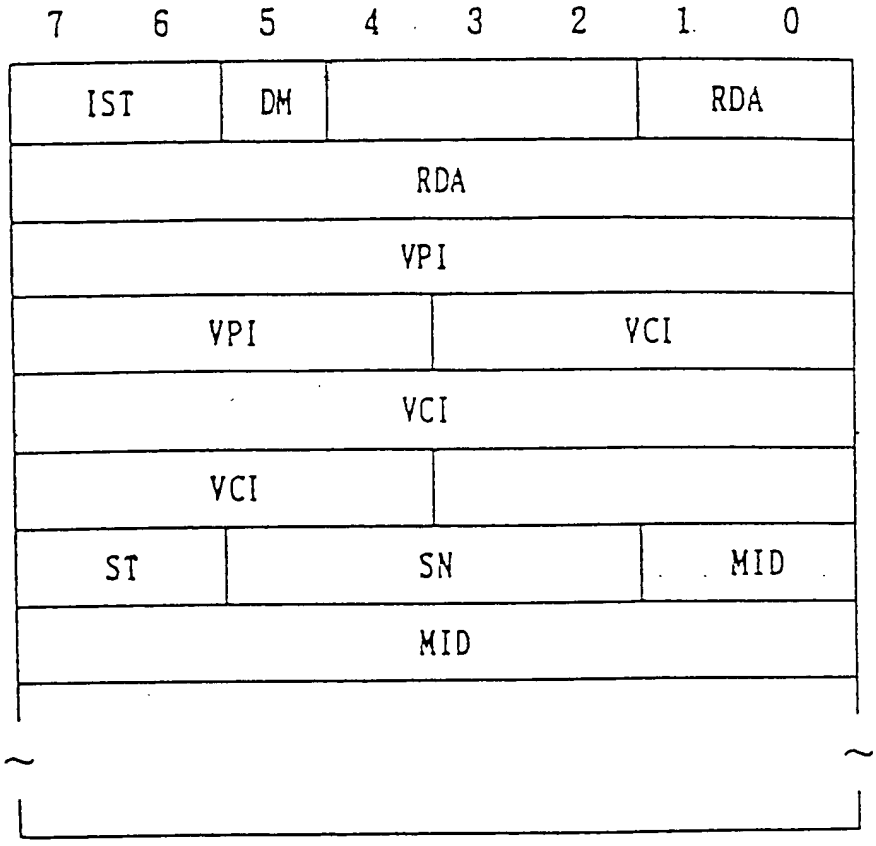


FIG. 424

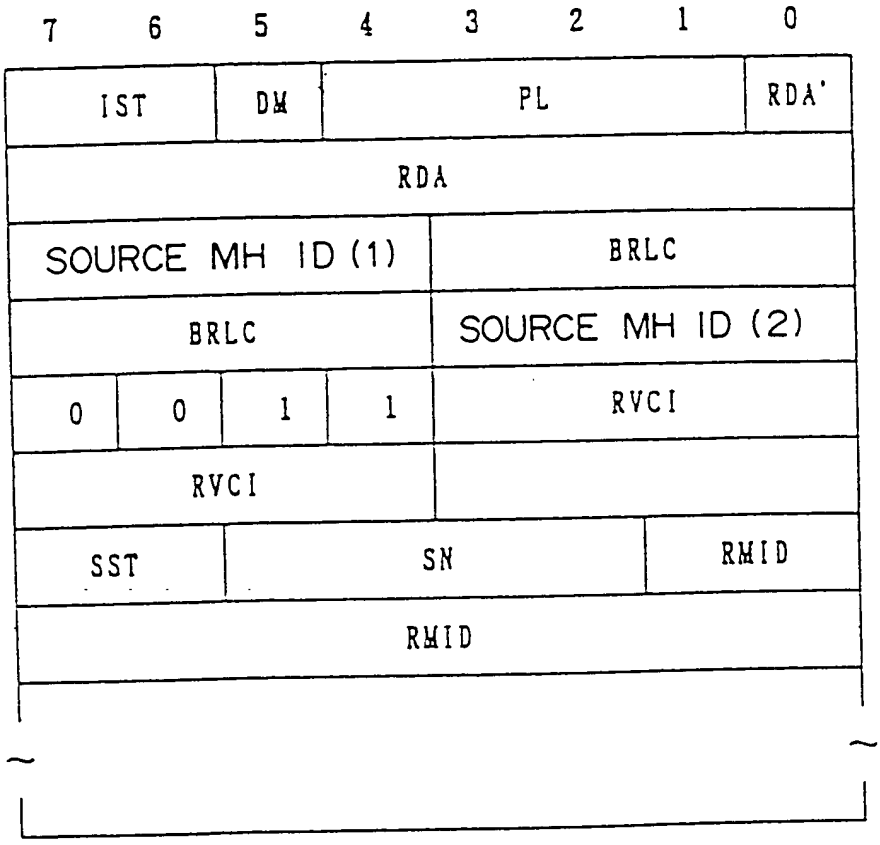

7 6 5 4 3 2 1 0
IST
DM
PL
RDA'
RDA
SOURCE MH ID (1)
BRLC
BRLC
SOURCE MH ID (2)
0 0 1 1
RVCI
RVCI
SST
SN
RMID
RMID

FIG. 425

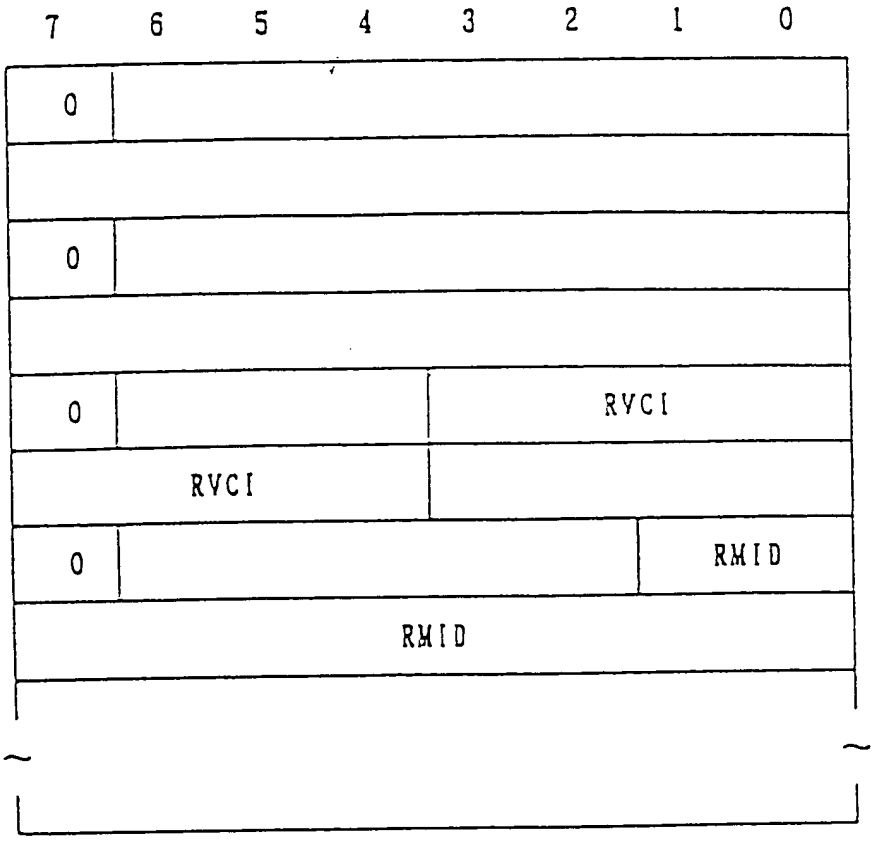


FIG. 426

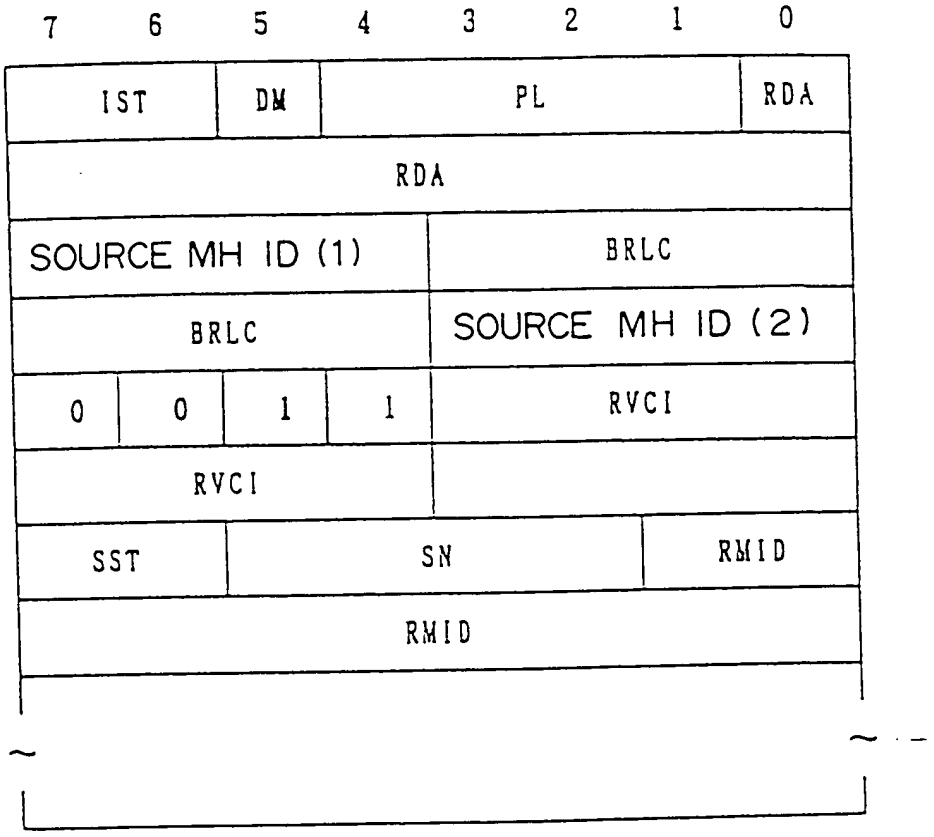

7 6 5 4 3 2 1 0
IST
DM
PL
RDA
RDA
SOURCE MH ID (1)
BRLC
BRLC
SOURCE MH ID (2)
0 0 1 1
RVCI
RVCI
SST
SN
RMID
RMID

FIG. 427

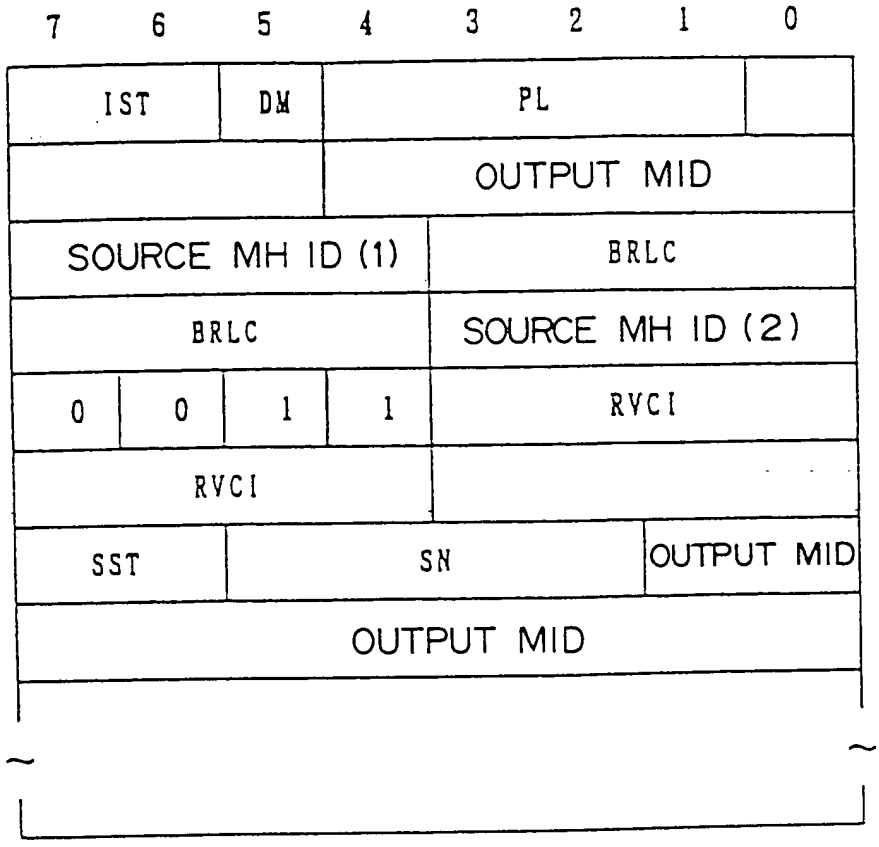

7 6 5 4 3 2 1 0
IST
DM
PL
OUTPUT MID
SOURCE MH ID (1)
BRLC
BRLC
SOURCE MH ID (2)
0 0 1 1
RVCI
RVCI
SST
SN
OUTPUT MID
OUTPUT MID

FIG. 428

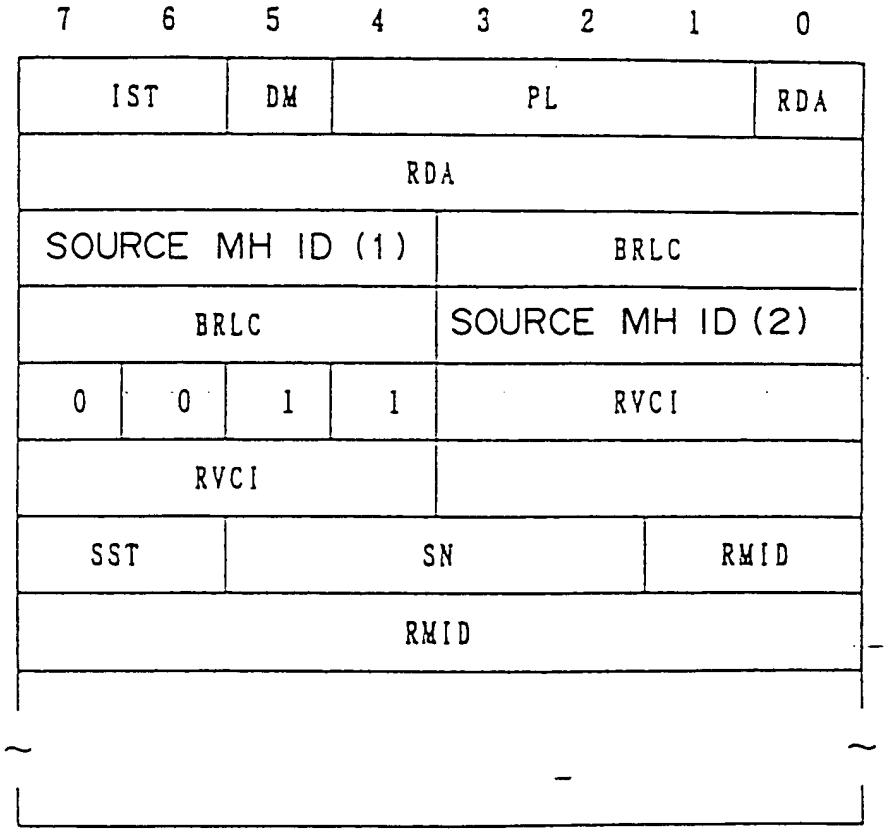

7 6 5 4 3 2 1 0
IST
DM
PL
RDA
RDA
SOURCE MH ID (1)
BRLC
BRLC
SOURCE MH ID (2)
0
0
1
1
RVCI
RVCI
SST
SN
RMID
RMID

FIG. 429

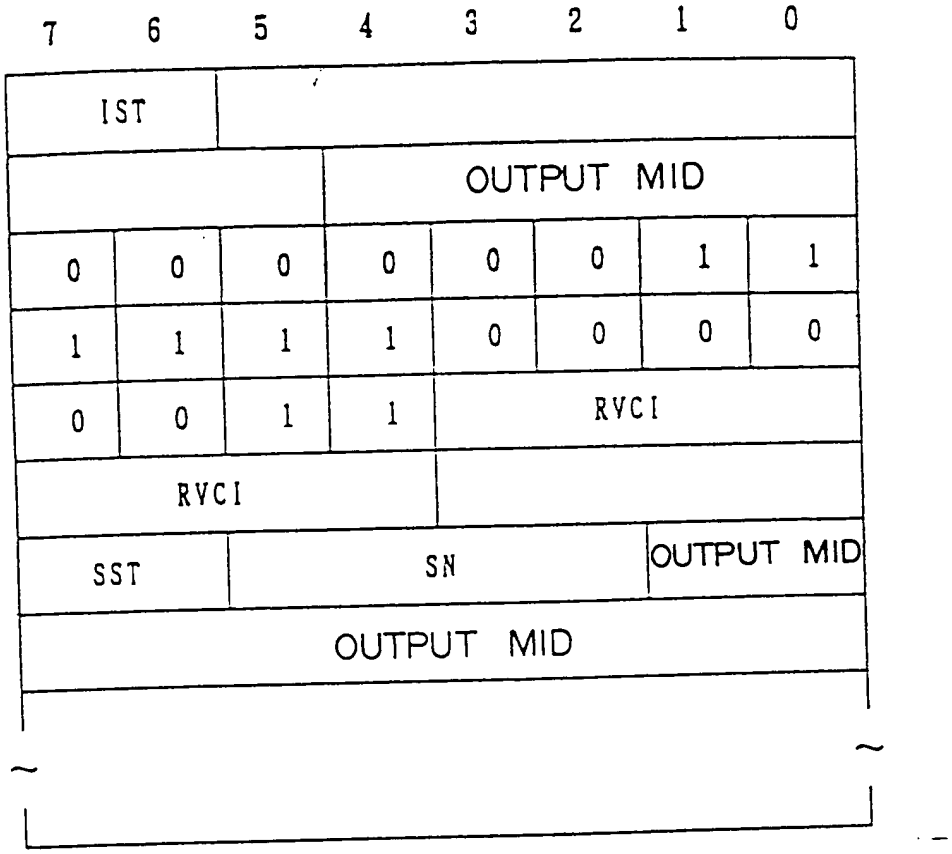

7 6 5 4 3 2 1 0
IST
OUTPUT MID
0 0 0 0 0 0 1 1
1 1 1 1 0 0 0 0
0 0 1 1 RVCI
RVCI
SST SN OUTPUT MID
OUTPUT MID

FIG. 430

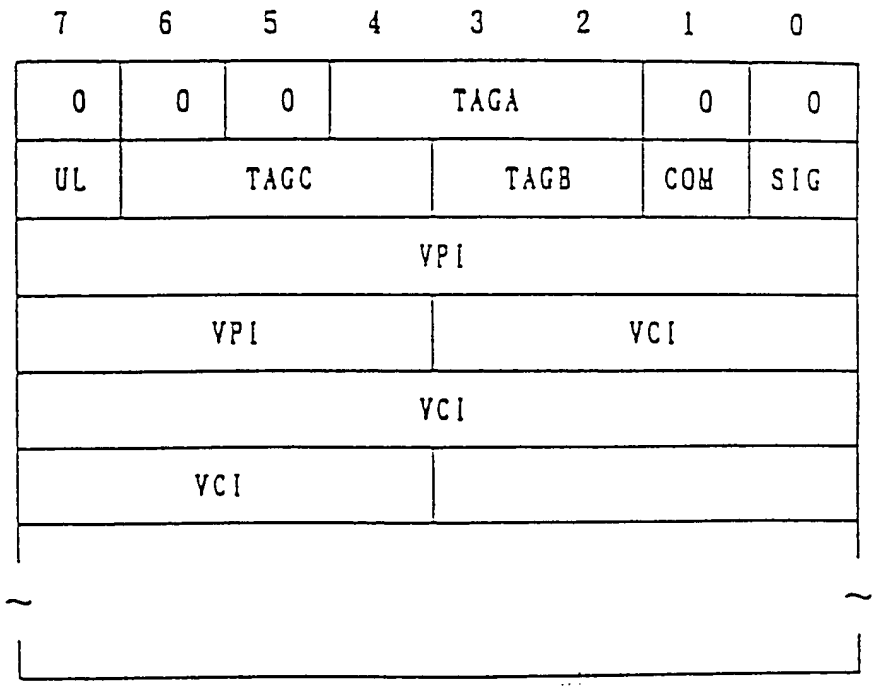
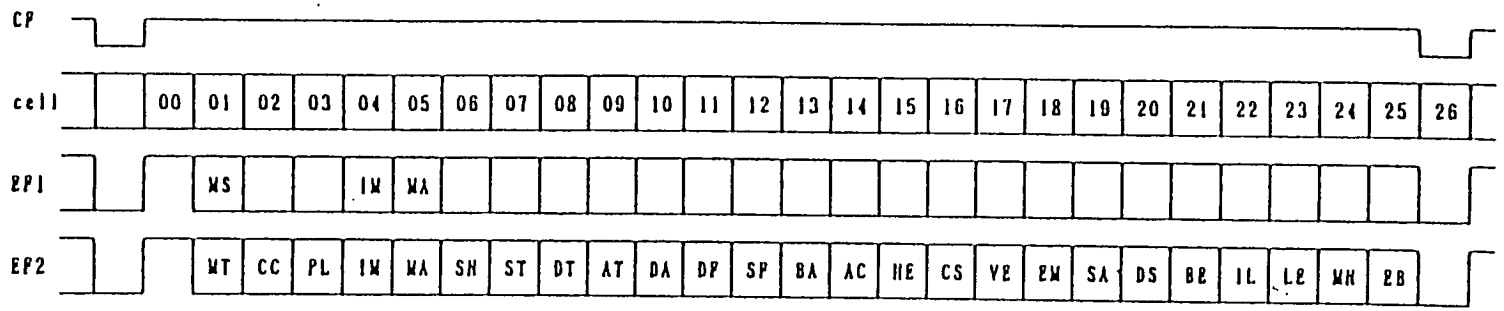


FIG. 431

10.24 ERROR FLAG (IN SMLP)



[EP1]

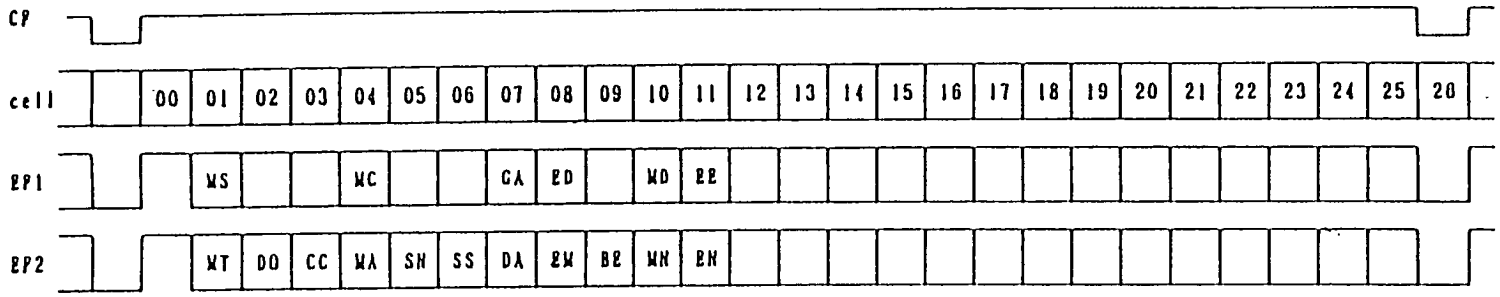
MS : master
IM : COM with MID=0
MA : MID not active (COM)

[EP2]

MT : MRI time out
CC : Payload CRC violation
PL : Payload length error
IM : BOM/SSM with invalid MID
MA : MID currently active or BOM with unapproved MID
SN : Invalid sequence number
ST : Invalid SA type
DT : Invalid DA type
AT : Invalid SMDS address type
DA : Individual DA assigned to originating SNI
DF : DA field format error
SP : SA field format error
BA : Invalid BAsize field value
AC : Access class violation
HE : Invalid HE length field value
CS : Invalid HB carrier selection
VE : Invalid HB version
EM : Exceed maximum number of CDU
SA : SA not assigned to originating SNI
DS : DA screening violation
BE : BEtag mismatch
IL : Incorrect length
LE : BAsize field not equal to length field
MN : MID assigned error
EB : End-user blocking

FIG. 432

10.25 ERROR FLAG (IN RMLP)



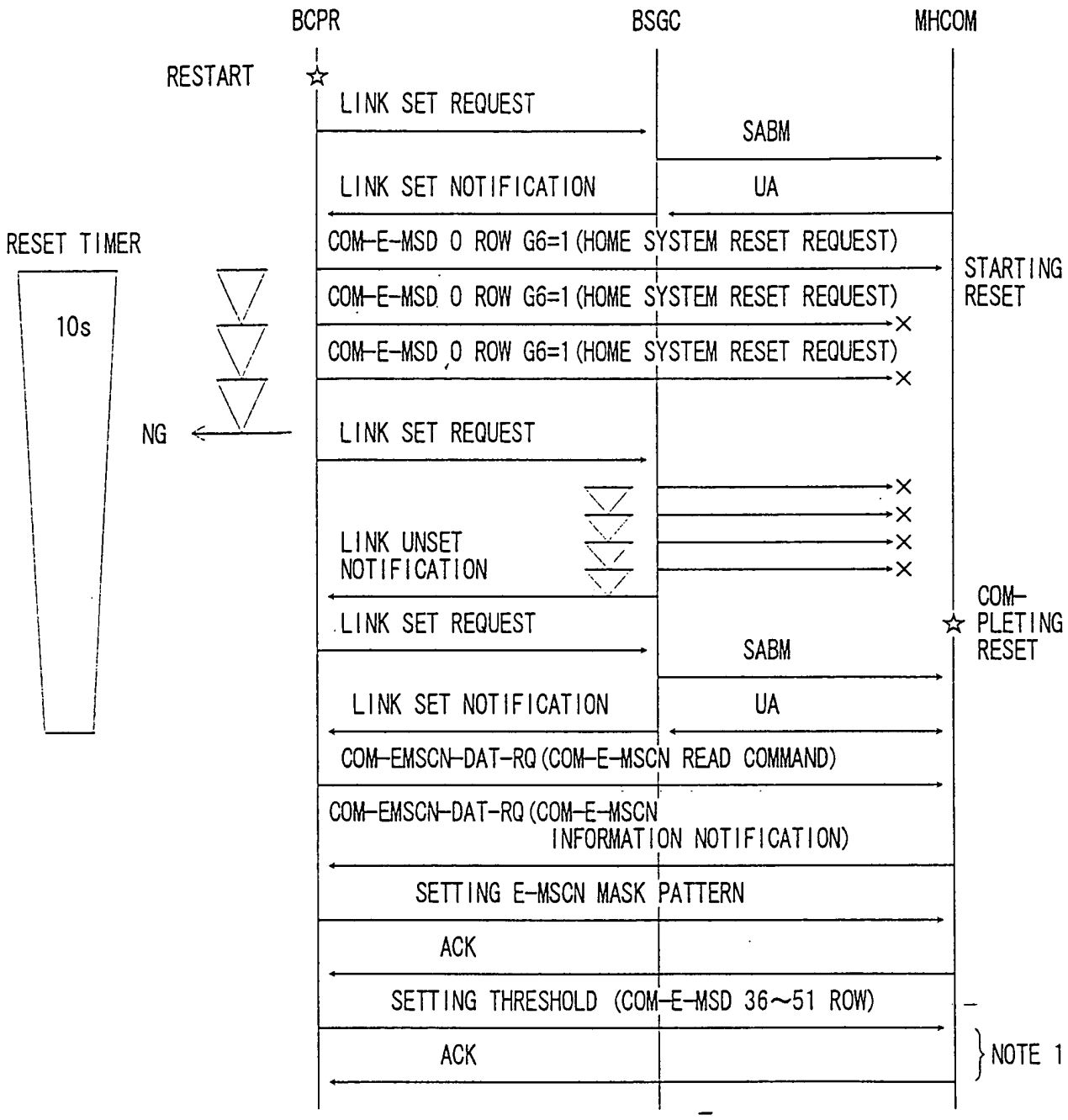
[EF1]

MS : master
MC : COM MID active error
GA : GA active error
ED : CDU active error
MD : RMID active error
BE : Encapsulation D.C.

[EF2]

MT : MRI time out
DO : Destination equal to originating SNI
CC : Payload CRC violation
MA : MID active error
SN : Invalid sequence number
SS : SA screening violation
DA : Destination SNI not available
EM : Exceed maximum number of CDU
BE : BEtag mismatch
MN : RMID assigned error
EN : Encapsulation error

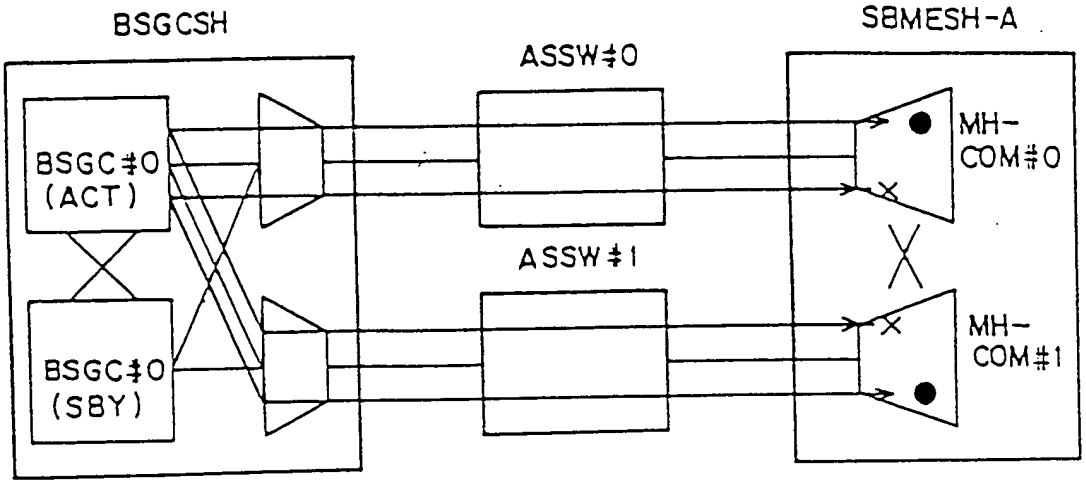
FIG. 433



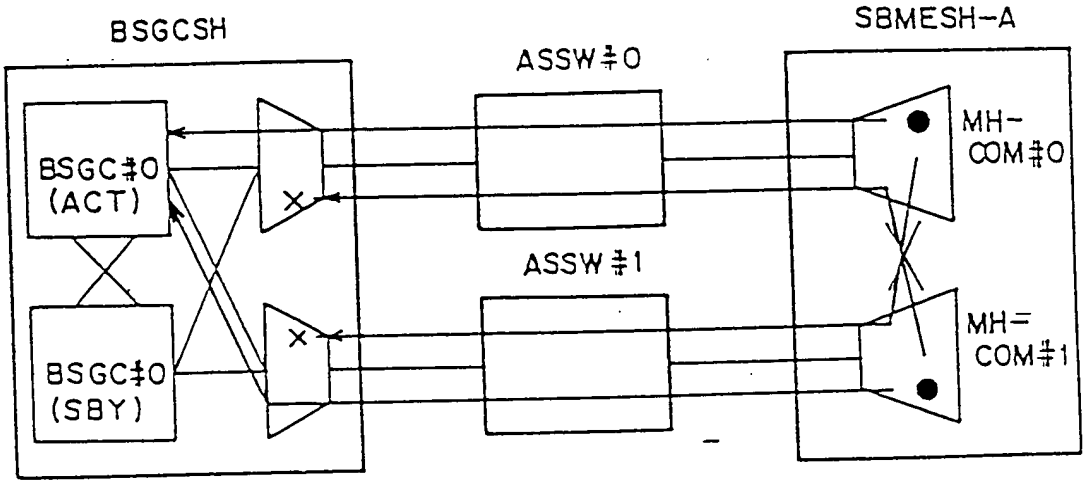
NOTE 1 : NOT NECESSARY TO SET THRESHOLD WHEN HARDWARE DEFAULT VALUE IS USED. SINGLE COMMAND CAN SET THRESHOLD OF 1MUX OR 1DMUX ONLY.

FIG. 434

(BSGC → MH-COM DIRECTION)



(MH-COM → BSGC DIRECTION)



●... ENDING POINT

×... DISCARDING POINT

FIG. 435

RECEIVING VPI/VCI VALUE		USE	SENDING VPI/VCI VALUE		USE
VPI(H)	VCI(H)		VPI(H)	VCI(H)	
000	03FC	INTRA-SYSTEM-#0 COMMUNICATIONS	0AA	0000 ~ 03FF	AA : BSGC CARD NO. VCI: BSGC PORT NO. 03FA AND 03FB FOR TEST USE(TCG)
000	03FD	INTRA-SYSTEM-#1 COMMUNICATIONS			

FIG. 436

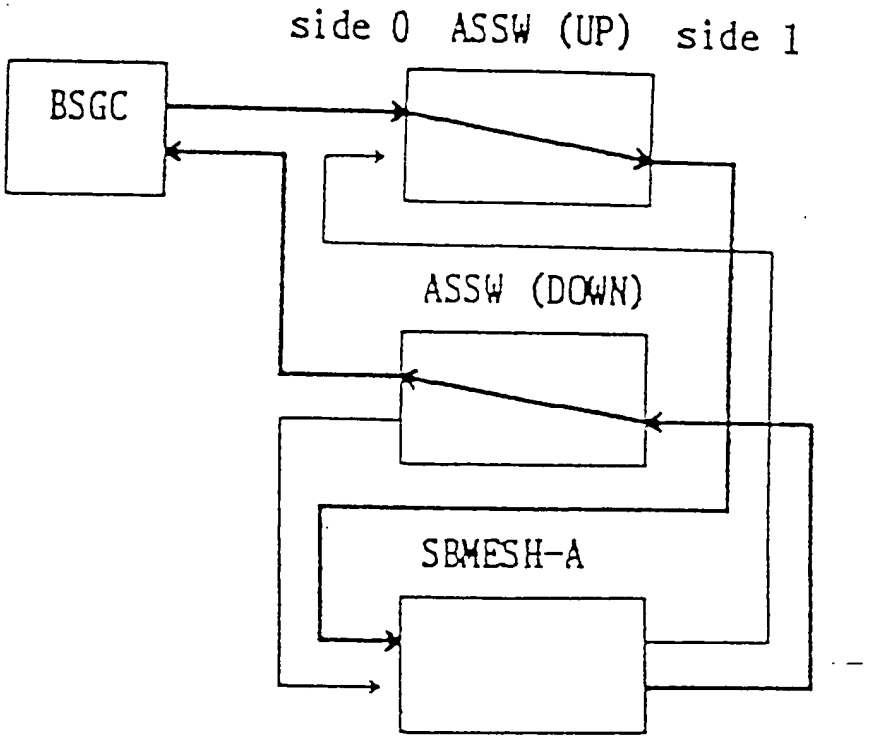


FIG. 437

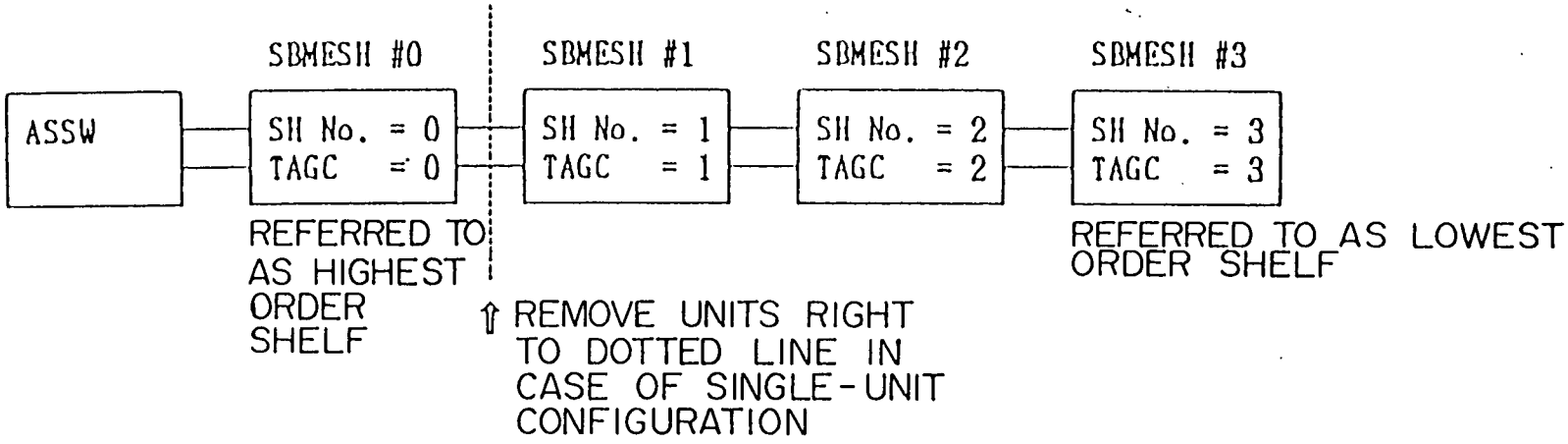

SBMESH #0
SBMESH #1
SBMESH #2
SBMESH #3
ASSW
SH No. = 0
TAGC = 0
SH No. = 1
TAGC = 1
SH No. = 2
TAGC = 2
SH No. = 3
TAGC = 3
REFERRED TO AS HIGHEST ORDER SHELF
REFERRED TO AS LOWEST ORDER SHELF
⇧ REMOVE UNITS RIGHT TO DOTTED LINE IN CASE OF SINGLE-UNIT CONFIGURATION

FIG. 438

shelf No.	UL	TAGC	COM	SIG	0
0	0	0	0	0	0
1	0	1	0	0	0
2	0	2	0	0	0
3	0	3	0	0	0

FIG. 439

shelf No.	UL	TAGC	COM	SIG	0
0	0	0	0	0	0
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	0

FIG. 440

5,502,482

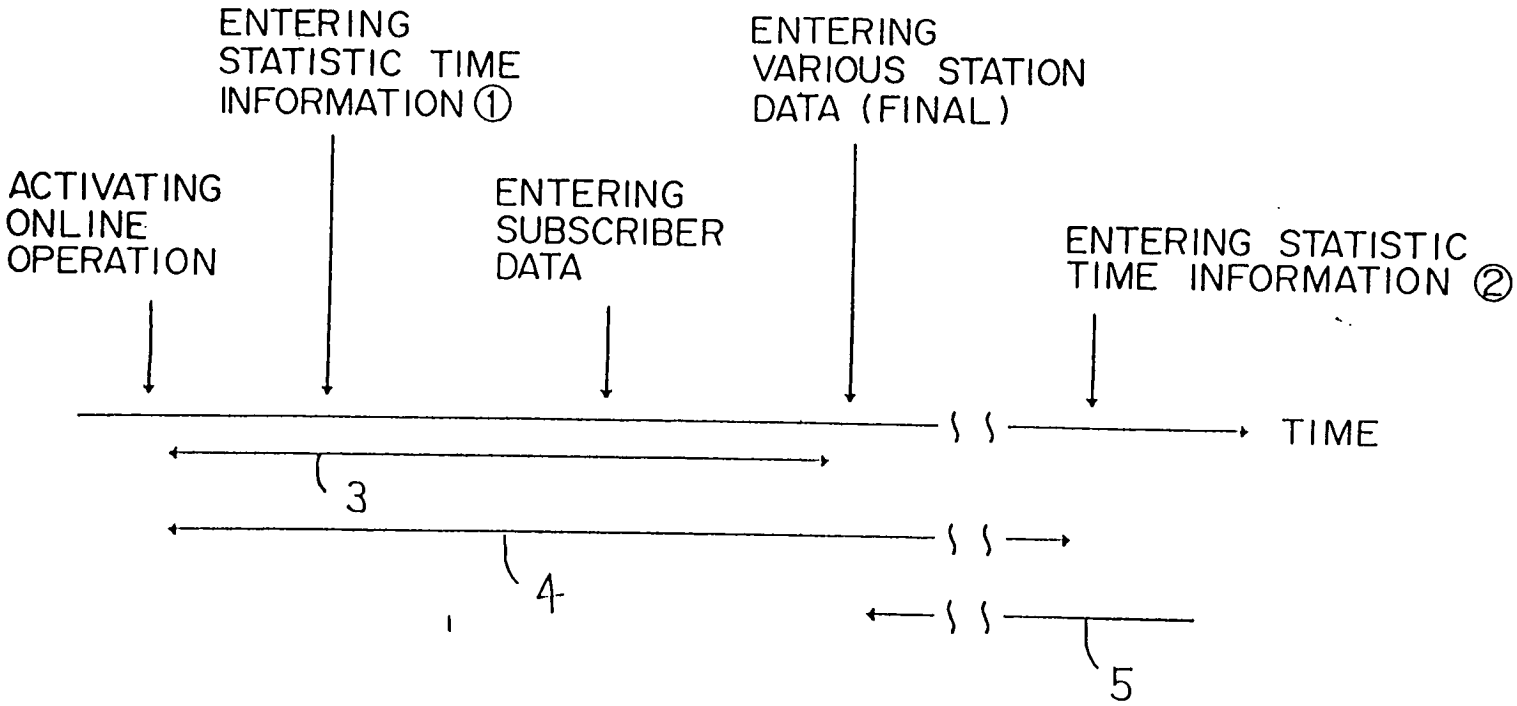

ENTERING
STATISTIC TIME
INFORMATION ①
ENTERING
VARIOUS STATION
DATA (FINAL)
ACTIVATING
ONLINE
OPERATION
ENTERING
SUBSCRIBER
DATA
ENTERING STATISTIC
TIME INFORMATION ②
TIME
3
4
5

FIG. 441

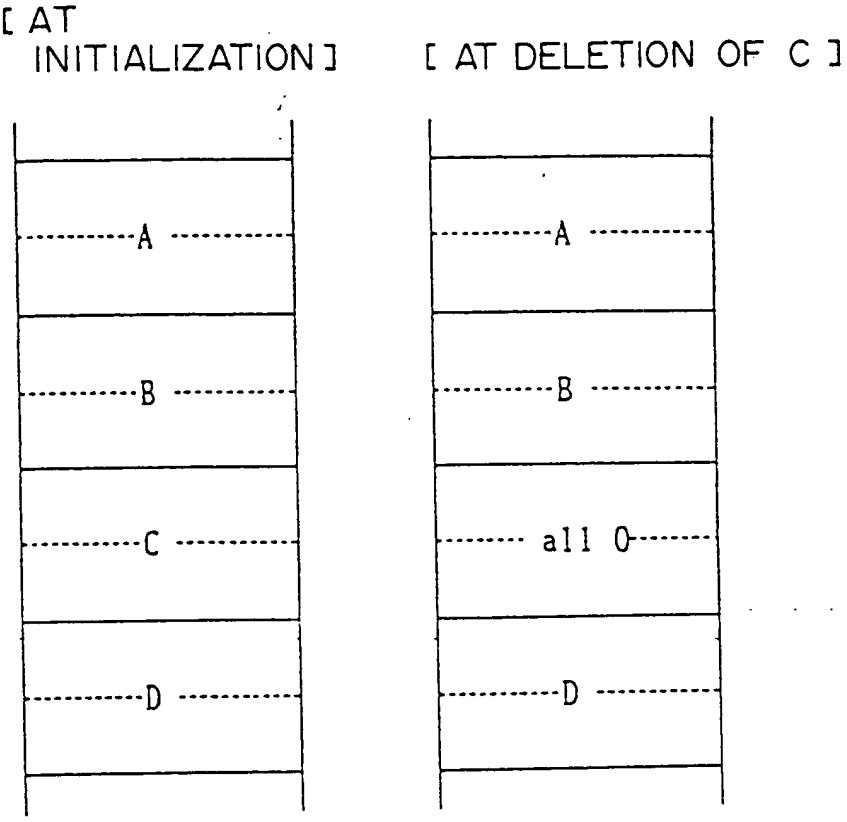


FIG. 442

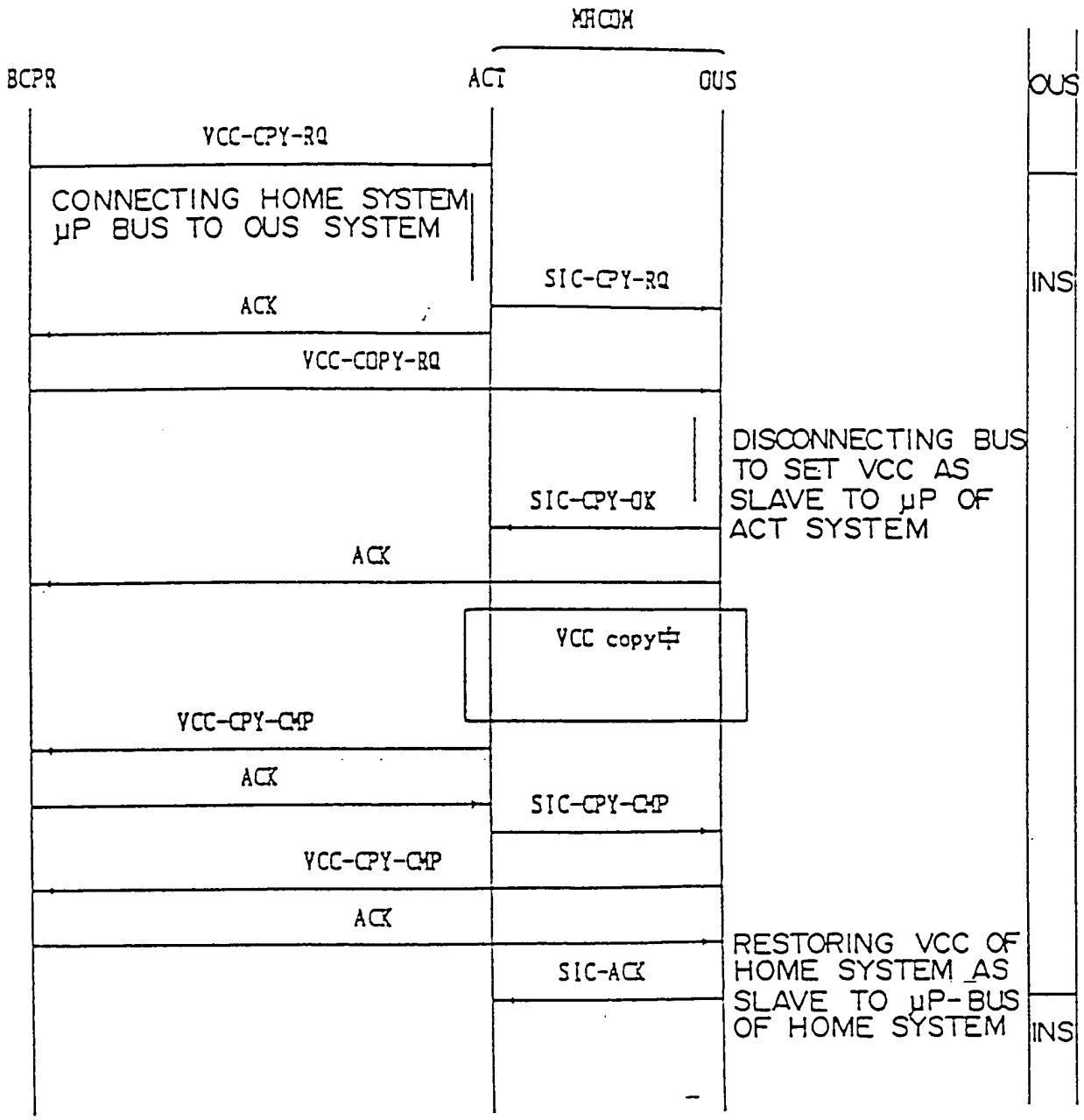

BCPR
ACT
OUS
OUS
VCC-CPY-RQ
CONNECTING HOME SYSTEM μP BUS TO OUS SYSTEM
SIC-CPY-RQ
INS
ACK
VCC-COPY-RQ
DISCONNECTING BUS TO SET VCC AS SLAVE TO μP OF ACT SYSTEM
SIC-CPY-OK
ACK
VCC copy中
VCC-CPY-CMP
ACK
SIC-CPY-CMP
VCC-CPY-CMP
ACK
RESTORING VCC OF HOME SYSTEM AS SLAVE TO μP-BUS OF HOME SYSTEM
SIC-ACK
INS

FIG. 443

ITEM	FAULT TYPE	NOTIFICATION METHOD	NOTIFYING SYSTEM	SUSPECT UNIT	ACTION					REMARKS
					ASSW SYSTEM SWITCH	FAULT BLOCK	FAULT MESSAGE	ALM LIGHTED	MAKING DIAGNOSIS	
1	HARDWARE FAULT (EXCEPT SIGNALLING UNIT AND RMUX UNIT)	HOME SYSTEM E-MSCN	ACT	ACT MHCOM	O	O	O	O	O PREVIOUS ACT	ACTIVATING DIAGNOSIS FROM MATE SYSTEM
			SBY	SBY MHCOM	—	O	O	O	O SBY	
2	HARDWARE FAULT (SIGNALLING UNIT AND RNUX UNIT)	MATE SYSTEM E-MSCN	ACT	SBY MHCOM	—	O	O	O	O SBY	
			SBY	ACT MHCOM	O	O	O	O	O PREVIOUS ACT	
3	OBP FAULT	MATE SYSTEM E-MSCN	ACT	SBY MHCOM	—	O	O	O	O SBY	
			SBY	ACT MHCOM	O	O	O	O	O PREVIOUS ACT	
4	MATE POWER PWCB FAULT (DISCONNECTION OF FUSE)	MATE SYSTEM E-MSCN	ACT	SBY SYSTEM POWER PWCB	—	O	O	O	O SBY	POWER SUPPLIED BY POWER PWCB CLOSING MHCOM ↓ BLOCKING ASSW OF CORRESPONDING SYSTEM
			SBY	ACT SYSTEM POWER PWCB	O	O	O	O	O PREVIOUS ACT	

FIG. 444

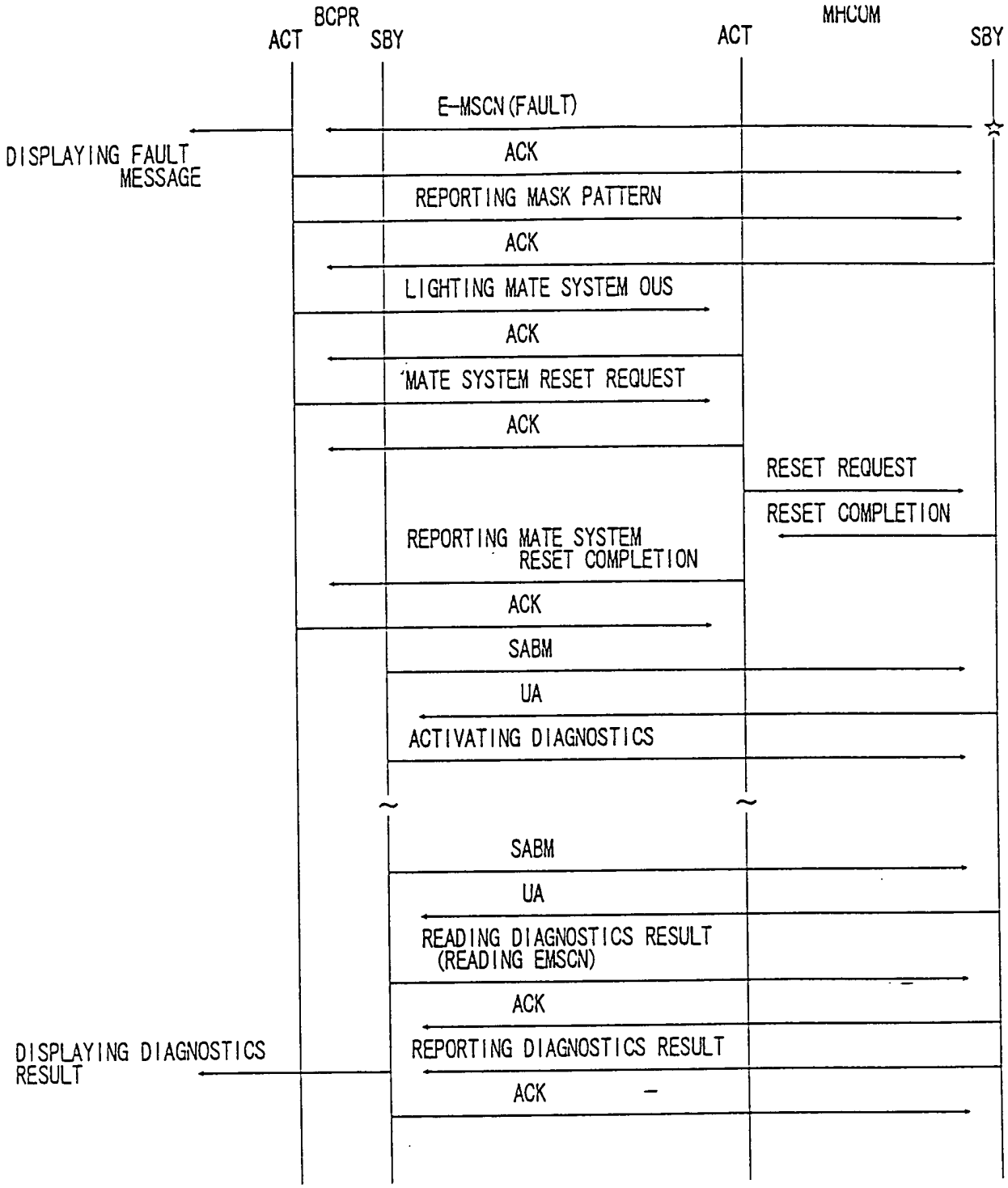

BCPR
ACT
SBY
MHCOM
ACT
SBY
E-MSCN (FAULT)
DISPLAYING FAULT MESSAGE
ACK
REPORTING MASK PATTERN
ACK
LIGHTING MATE SYSTEM OUS
ACK
MATE SYSTEM RESET REQUEST
ACK
RESET REQUEST
RESET COMPLETION
REPORTING MATE SYSTEM RESET COMPLETION
ACK
SABM
UA
ACTIVATING DIAGNOSTICS
SABM
UA
READING DIAGNOSTICS RESULT (READING EMSCN)
ACK
REPORTING DIAGNOSTICS RESULT
ACK
DISPLAYING DIAGNOSTICS RESULT

FIG. 445

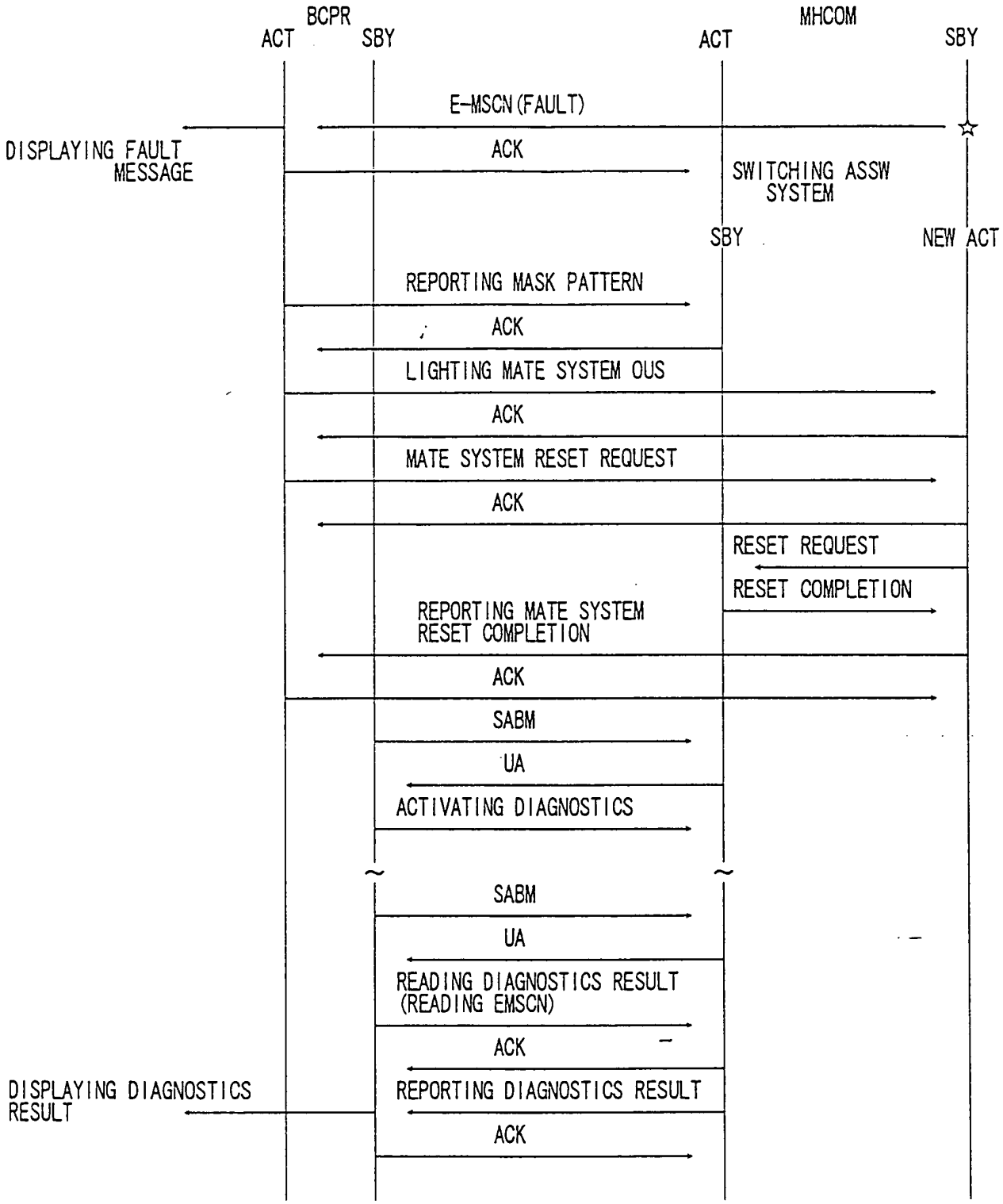

BCPR
ACT
SBY
MHCOM
ACT
SBY
E-MSCN(FAULT)
DISPLAYING FAULT MESSAGE
ACK
SWITCHING ASSW SYSTEM
SBY
NEW ACT
REPORTING MASK PATTERN
ACK
LIGHTING MATE SYSTEM OUS
ACK
MATE SYSTEM RESET REQUEST
ACK
RESET REQUEST
RESET COMPLETION
REPORTING MATE SYSTEM RESET COMPLETION
ACK
SABM
UA
ACTIVATING DIAGNOSTICS
SABM
UA
READING DIAGNOSTICS RESULT (READING EMSCN)
ACK
DISPLAYING DIAGNOSTICS RESULT
REPORTING DIAGNOSTICS RESULT
ACK

FIG. 446

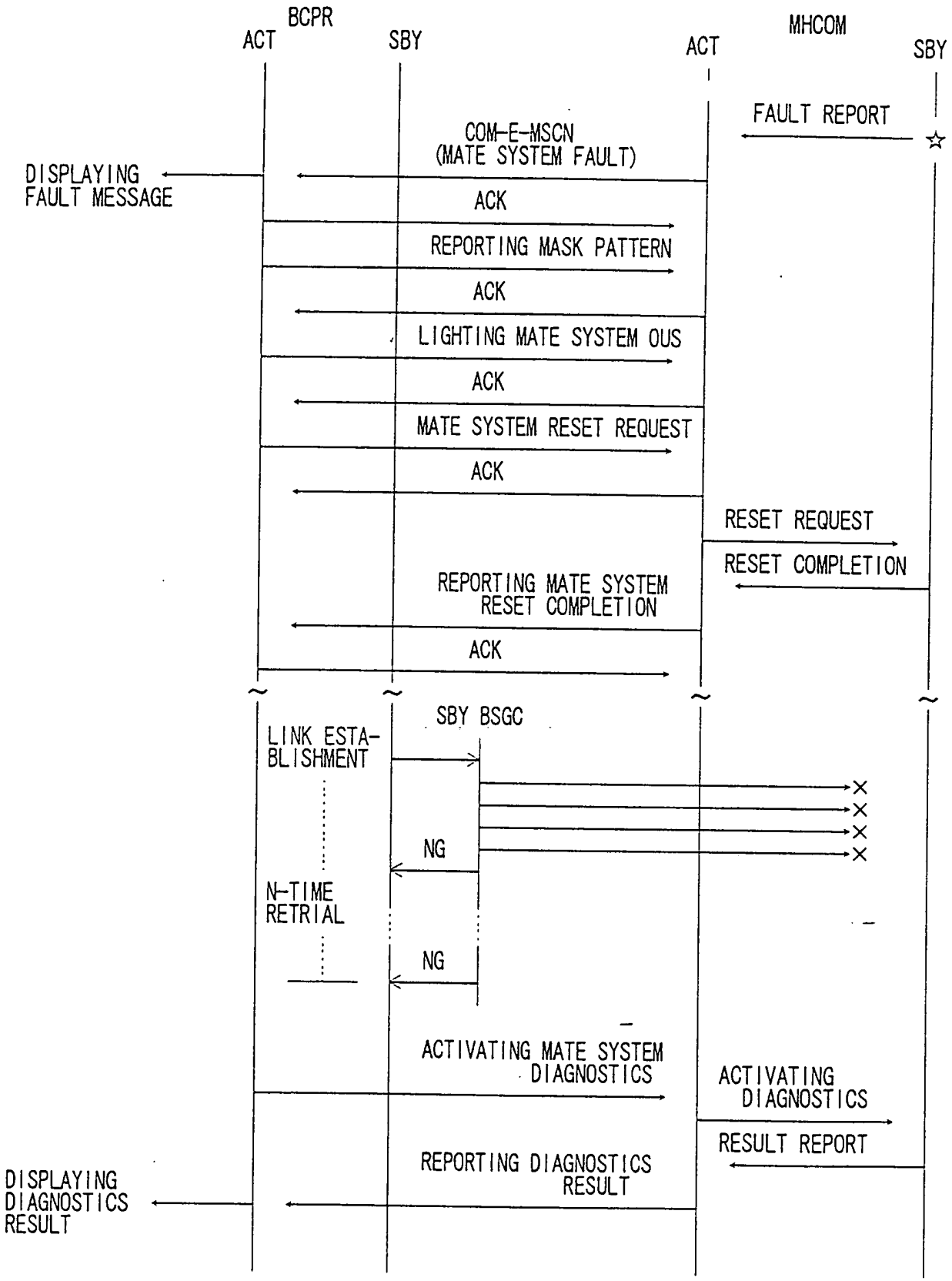

BCPR
ACT
SBY
MHCOM
ACT
SBY
FAULT REPORT
COM-E-MSCN
(MATE SYSTEM FAULT)
DISPLAYING
FAULT MESSAGE
ACK
REPORTING MASK PATTERN
ACK
LIGHTING MATE SYSTEM OUS
ACK
MATE SYSTEM RESET REQUEST
ACK
RESET REQUEST
RESET COMPLETION
REPORTING MATE SYSTEM
RESET COMPLETION
ACK
SBY BSGC
LINK ESTA-
BLISHMENT
NG
N-TIME
RETRIAL
NG
ACTIVATING MATE SYSTEM
DIAGNOSTICS
ACTIVATING
DIAGNOSTICS
RESULT REPORT
REPORTING DIAGNOSTICS
RESULT
DISPLAYING
DIAGNOSTICS
RESULT

FIG. 447

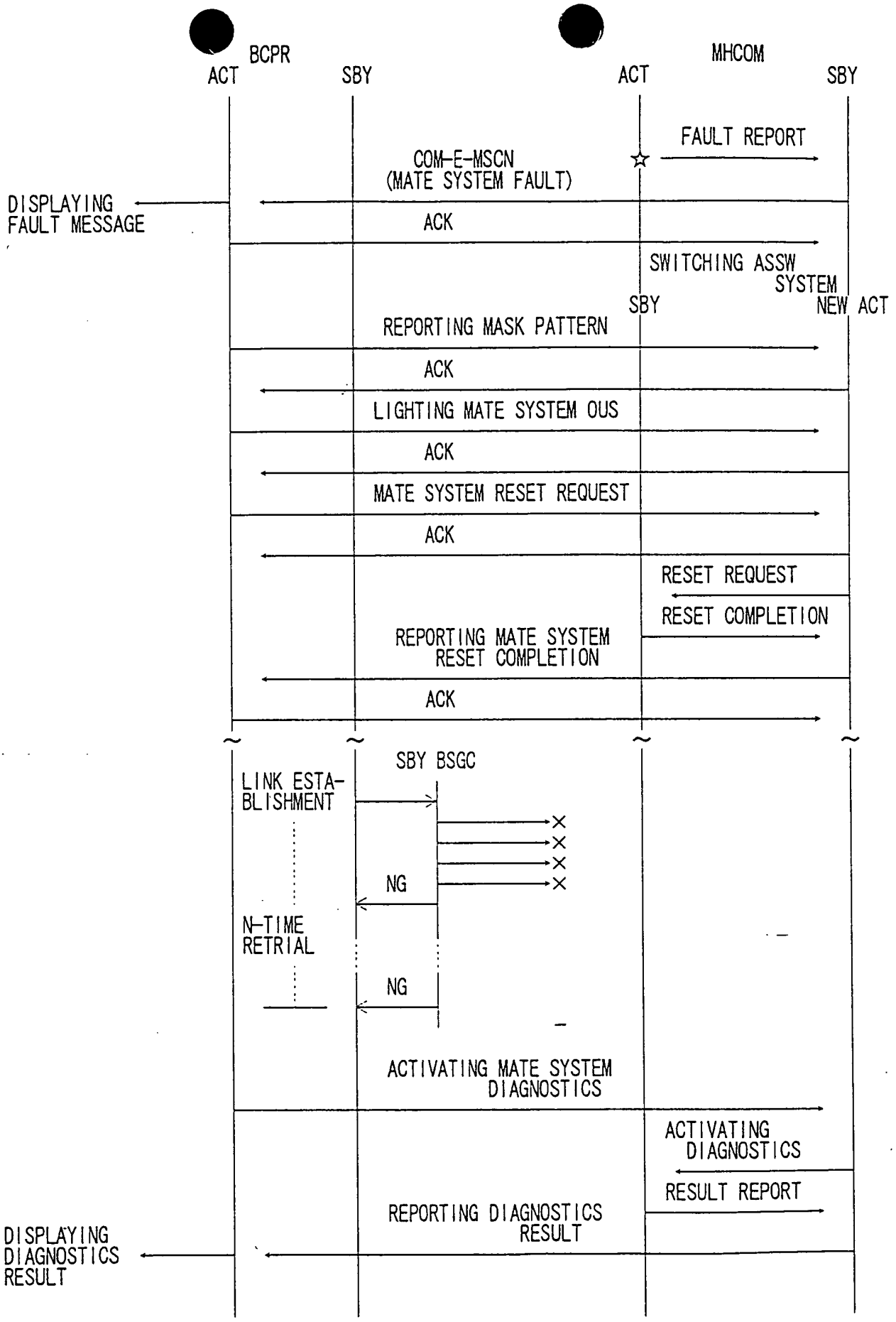

BCPR
ACT
SBY
MHCOM
ACT
SBY
FAULT REPORT
COM-E-MSCN
(MATE SYSTEM FAULT)
DISPLAYING
FAULT MESSAGE
ACK
SWITCHING ASSW
SYSTEM
SBY
NEW ACT
REPORTING MASK PATTERN
ACK
LIGHTING MATE SYSTEM OUS
ACK
MATE SYSTEM RESET REQUEST
ACK
RESET REQUEST
RESET COMPLETION
REPORTING MATE SYSTEM
RESET COMPLETION
ACK
SBY BSGC
LINK ESTA-
BLISHMENT
NG
N-TIME
RETRIAL
NG
ACTIVATING MATE SYSTEM
DIAGNOSTICS
ACTIVATING
DIAGNOSTICS
RESULT REPORT
REPORTING DIAGNOSTICS
RESULT
DISPLAYING
DIAGNOSTICS
RESULT

FIG. 448

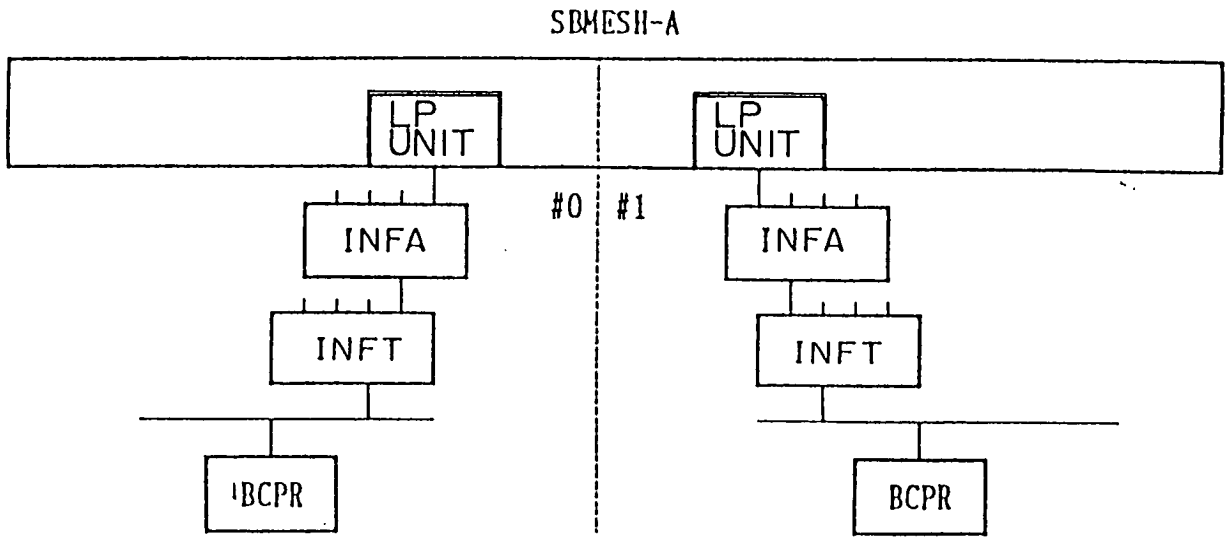


FIG. 449

BIT	CONTENTS	POLARITY
31	DISPLAYING RESET COMPLETION	1 WHEN RESET COMPLETION
30	DON'T CARE	———
29	LP UNIT FAULT	1 WHEN FAULT OCCURS
28	DMA ACCESS ERROR 1	1 WHEN ERROR OCCURS
27	DMA ACCESS ERROR 2	1 WHEN ERROR OCCURS
26	DMA PARITY ERROR	1 WHEN ERROR OCCURS
25	DMA TIME OVER	1 AT TIME OVER
24	DON'T CARE	———
23	MPAL : MATE LP UNIT FAULT	1 WHEN FAULT OCCURS
22	MFAL : MATE FUSE ALARM	1 WHEN ALARM IS OUTPUT
21	HOME SDMX ⇨ SMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
20	HOME SDMX ⇨ SMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
19	MATE SDMX ⇨ SMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
18	MATE SDMX ⇨ SMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
17	SMLP ⇨ HOME SMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
16	SMLP ⇨ HOME SMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
15	SMLP ⇨ MATE SMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
14	SMLP ⇨ MATE SMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
13	HOME RDMX ⇨ RMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
12	HOME RDMX ⇨ RMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
11	MATE RDMX ⇨ RMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
10	MATE RDMX ⇨ RMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
09	RMLP ⇨ HOME RMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
08	RMLP ⇨ HOME RMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
07	RMLP ⇨ MATE RMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
06	RMLP ⇨ MATE RMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
05	DON'T CARE	———
04	DON'T CARE	———
03	DON'T CARE	———
02	DON'T CARE	———
01	HOME MH-COM ⇨ LP CROSS-CONNECTION FAULT SOURCE CLOCK NG	1 AT NG
00	MATE MH-COM ⇨ LP CROSS-CONNECTION FAULT SOURCE CLOCK NG	1 AT NG

FIG. 450

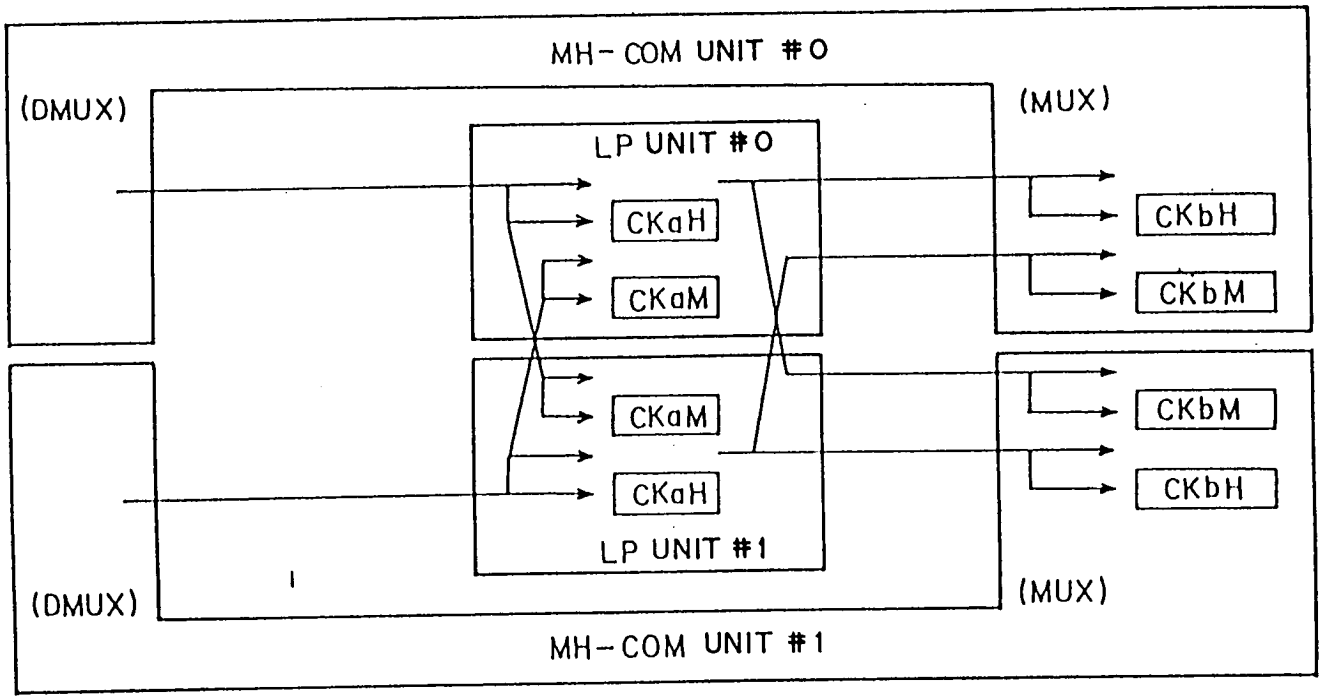

MH-COM UNIT #0
(DMUX)
LP UNIT #0
CKaH
CKaM
(MUX)
CKbH
CKbM
CKaM
CKaH
LP UNIT #1
CKbM
CKbH
(DMUX)
(MUX)
MH-COM UNIT #1

FIG. 451

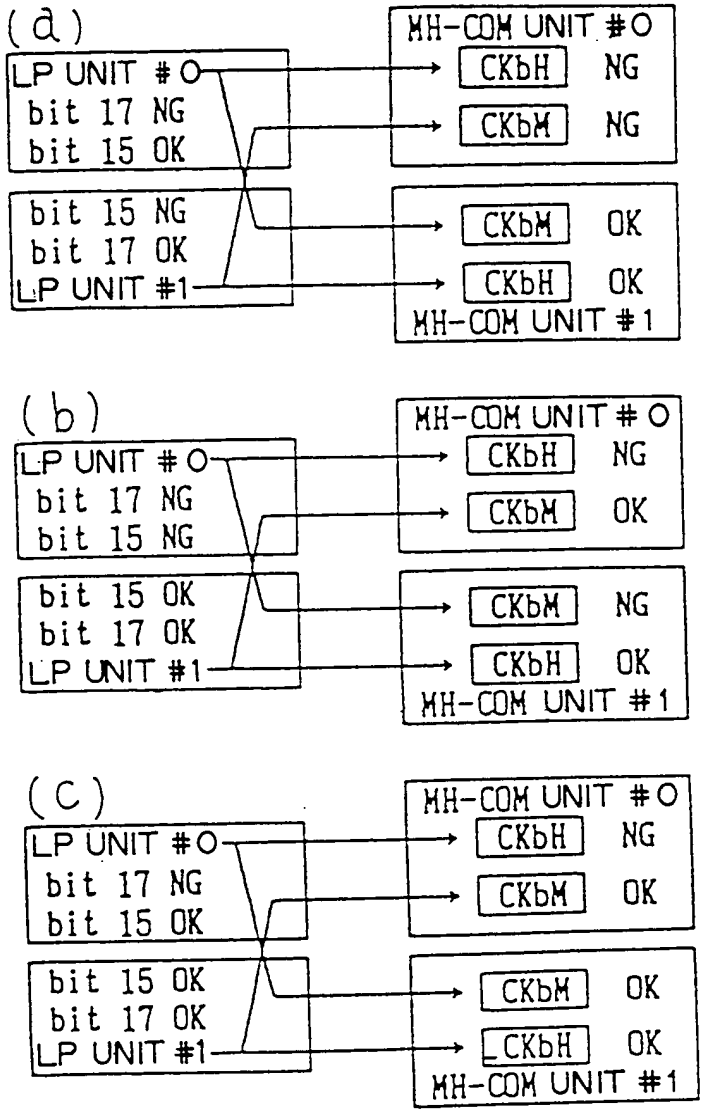

(a)
LP UNIT #0
bit 17 NG
bit 15 OK
bit 15 NG
bit 17 OK
LP UNIT #1
MH-COM UNIT #0
CKbH NG
CKbM NG
CKbM OK
CKbH OK
MH-COM UNIT #1
(b)
LP UNIT #0
bit 17 NG
bit 15 NG
bit 15 OK
bit 17 OK
LP UNIT #1
MH-COM UNIT #0
CKbH NG
CKbM OK
CKbM NG
CKbH OK
MH-COM UNIT #1
(c)
LP UNIT #0
bit 17 NG
bit 15 OK
bit 15 OK
bit 17 OK
LP UNIT #1
MH-COM UNIT #0
CKbH NG
CKbM OK
CKbM OK
CKbH OK
MH-COM UNIT #1

FIG. 452

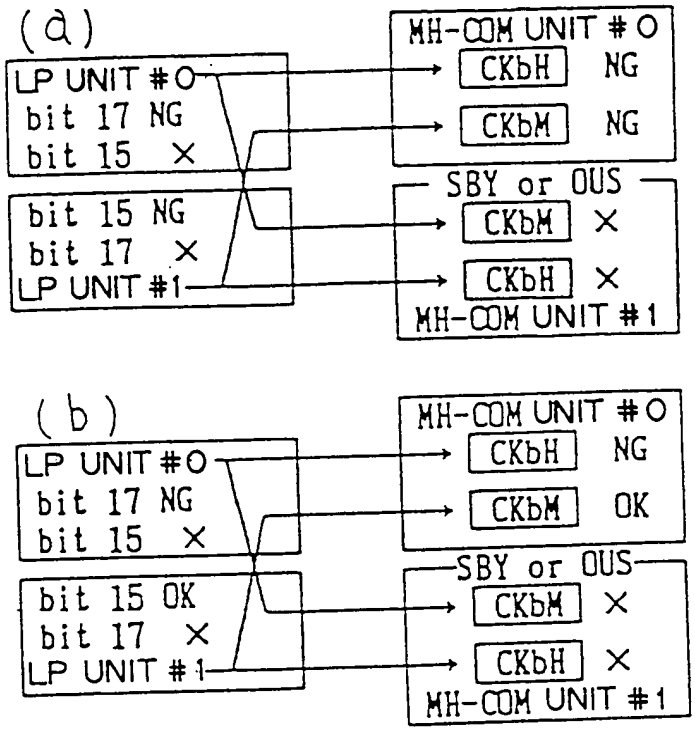

(a)
LP UNIT #0
bit 17 NG
bit 15 ×
bit 15 NG
bit 17 ×
LP UNIT #1
MH-COM UNIT #0
CKbH NG
CKbM NG
SBY or OUS
CKbM ×
CKbH ×
MH-COM UNIT #1
(b)
LP UNIT #0
bit 17 NG
bit 15 ×
bit 15 OK
bit 17 ×
LP UNIT #1
MH-COM UNIT #0
CKbH NG
CKbM OK
SBY or OUS
CKbM ×
CKbH ×
MH-COM UNIT #1

FIG. 453

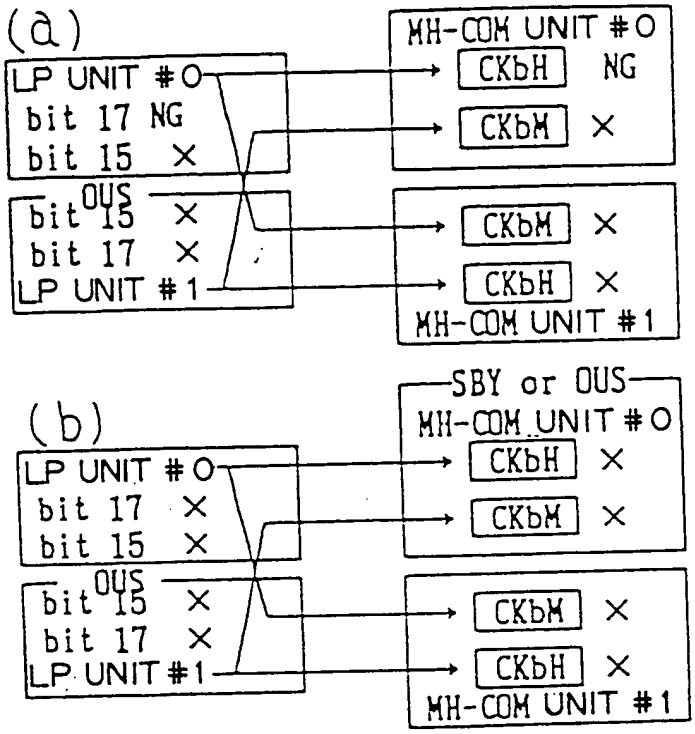

(a)
LP UNIT #0
bit 17 NG
bit 15 ×
OUS
bit 15 ×
bit 17 ×
LP UNIT #1
MH-COM UNIT #0
CKbH NG
CKbM ×
CKbM ×
CKbH ×
MH-COM UNIT #1
(b)
LP UNIT #0
bit 17 ×
bit 15 ×
OUS
bit 15 ×
bit 17 ×
LP UNIT #1
SBY or OUS
MH-COM UNIT #0
CKbH ×
CKbM ×
CKbM ×
CKbH ×
MH-COM UNIT #1

FIG. 454

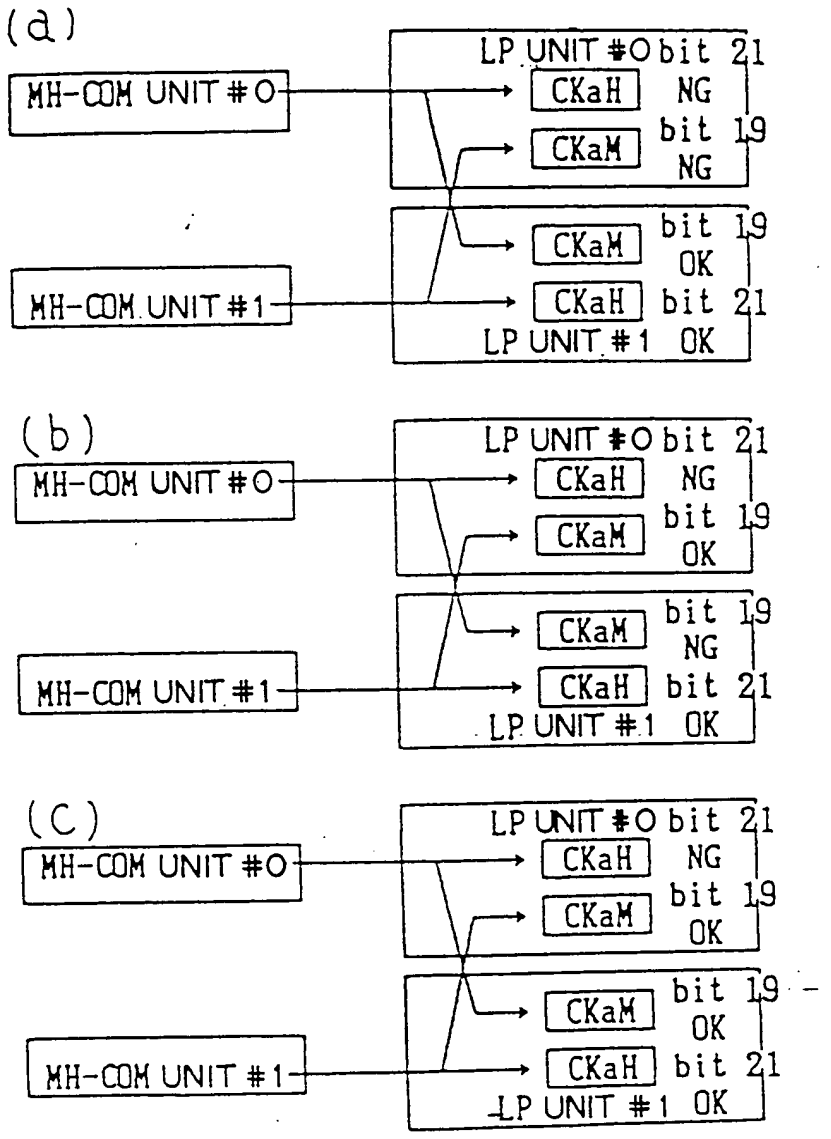

(a)
MH-COM UNIT #0
MH-COM UNIT #1
LP UNIT #0 bit 21
CKaH
NG
bit 19
CKaM
NG
CKaM
bit 19
OK
CKaH
bit 21
LP UNIT #1 OK
(b)
MH-COM UNIT #0
MH-COM UNIT #1
LP UNIT #0 bit 21
CKaH
NG
bit 19
CKaM
OK
CKaM
bit 19
NG
CKaH
bit 21
LP UNIT #1 OK
(C)
MH-COM UNIT #0
MH-COM UNIT #1
LP UNIT #0 bit 21
CKaH
NG
bit 19
CKaM
OK
CKaM
bit 19
OK
CKaH
bit 21
LP UNIT #1 OK

FIG. 455

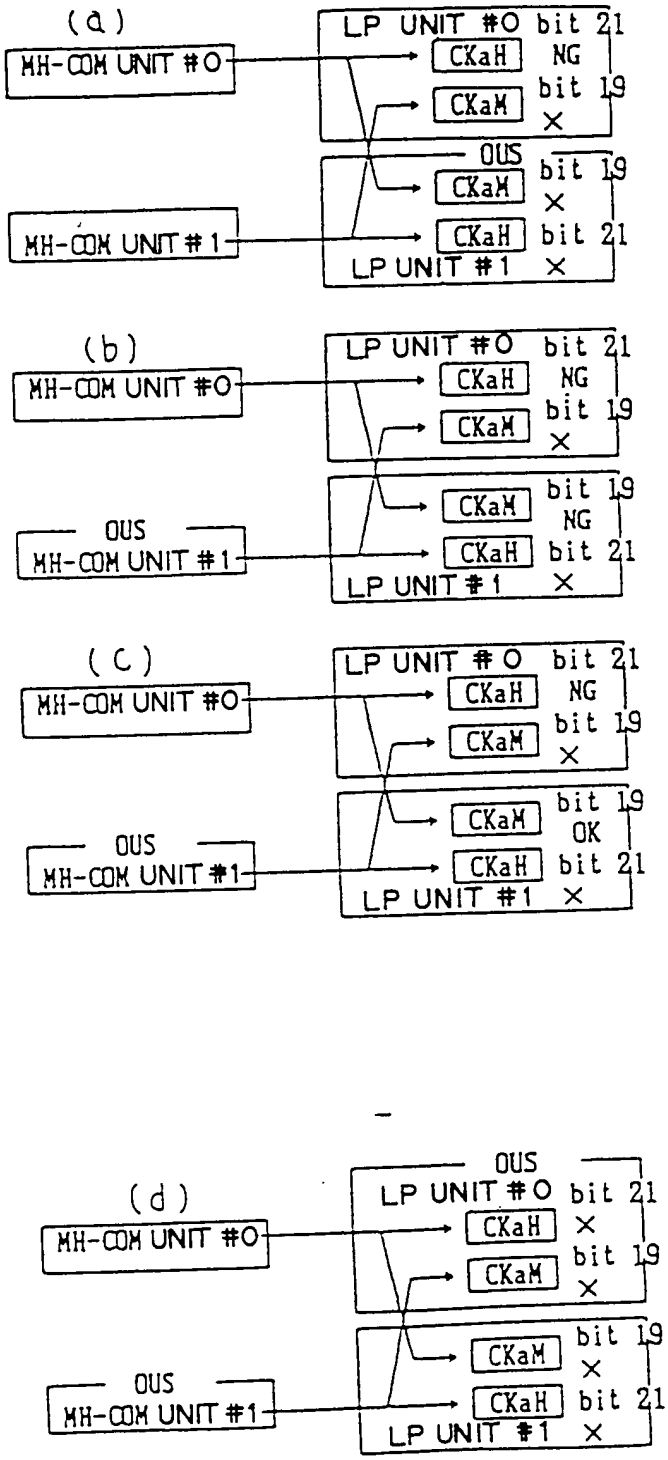

(a)
MH-COM UNIT #0
LP UNIT #0 bit 21
CKaH NG
CKaM bit 19 ×
OUS
CKaM bit 19 ×
MH-COM UNIT #1
CKaH bit 21
LP UNIT #1 ×
(b)
MH-COM UNIT #0
LP UNIT #0 bit 21
CKaH NG
CKaM bit 19 ×
OUS
MH-COM UNIT #1
CKaM bit 19 NG
CKaH bit 21
LP UNIT #1 ×
(C)
MH-COM UNIT #0
LP UNIT #0 bit 21
CKaH NG
CKaM bit 19 ×
OUS
MH-COM UNIT #1
CKaM bit 19 OK
CKaH bit 21
LP UNIT #1 ×
(d)
MH-COM UNIT #0
OUS
LP UNIT #0 bit 21
CKaH ×
CKaM bit 19 ×
OUS
MH-COM UNIT #1
CKaM bit 19 ×
CKaH bit 21
LP UNIT #1 ×

FIG. 456

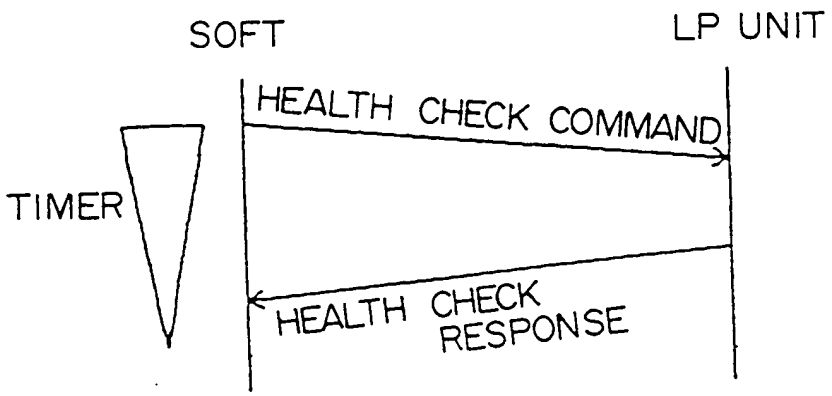

SOFT
LP UNIT
HEALTH CHECK COMMAND
TIMER
HEALTH CHECK
RESPONSE

FIG. 457

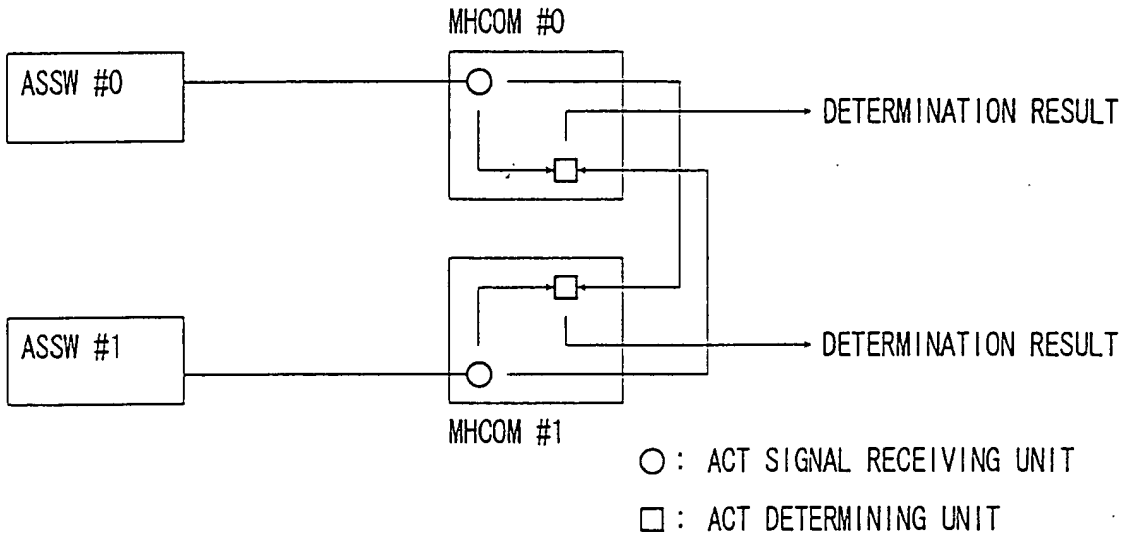

MHCOM #0
ASSW #0
DETERMINATION RESULT
ASSW #1
DETERMINATION RESULT
MHCOM #1
○ : ACT SIGNAL RECEIVING UNIT
□ : ACT DETERMINING UNIT

FIG. 458

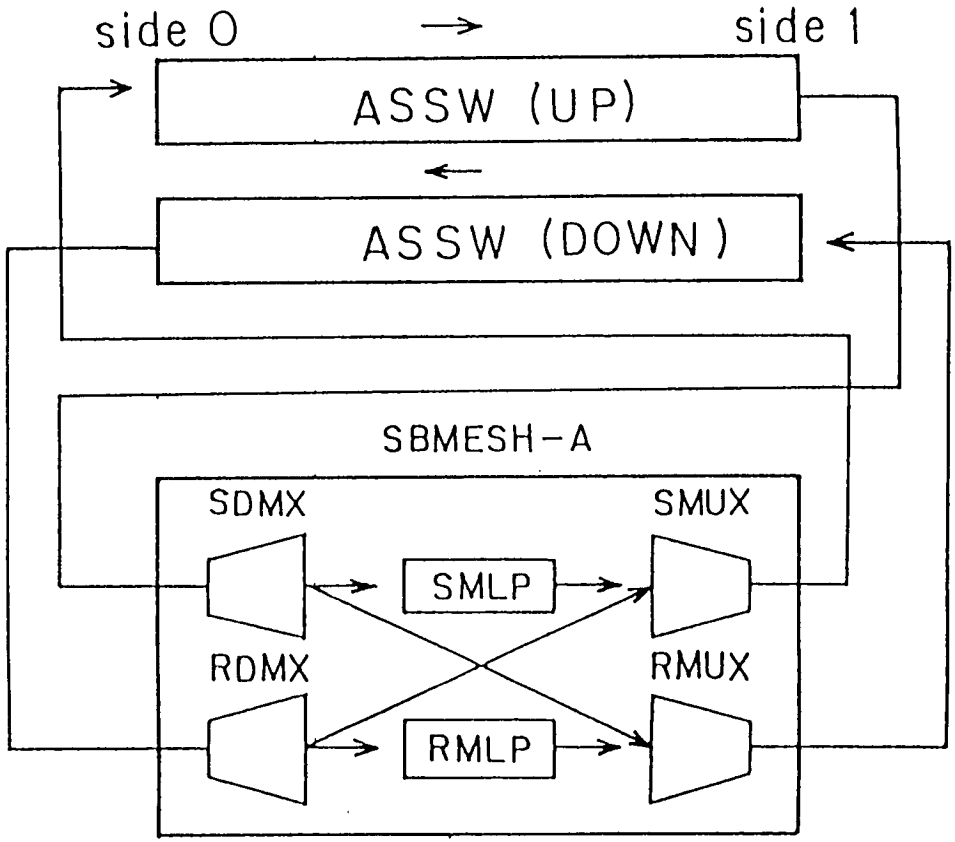

side 0
side 1
ASSW (UP)
ASSW (DOWN)
SBMESH-A
SDMX
SMUX
SMLP
RDMX
RMUX
RMLP

FIG. 459

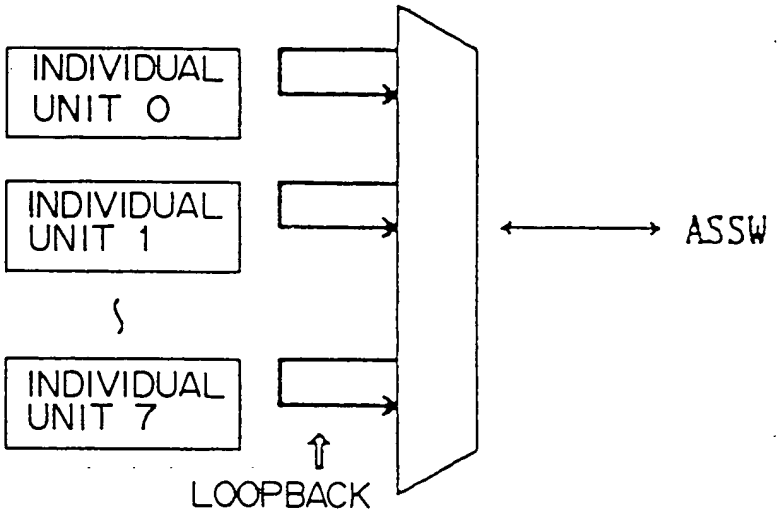

INDIVIDUAL UNIT 0
INDIVIDUAL UNIT 1
INDIVIDUAL UNIT 7
ASSW
LOOPBACK

FIG. 460

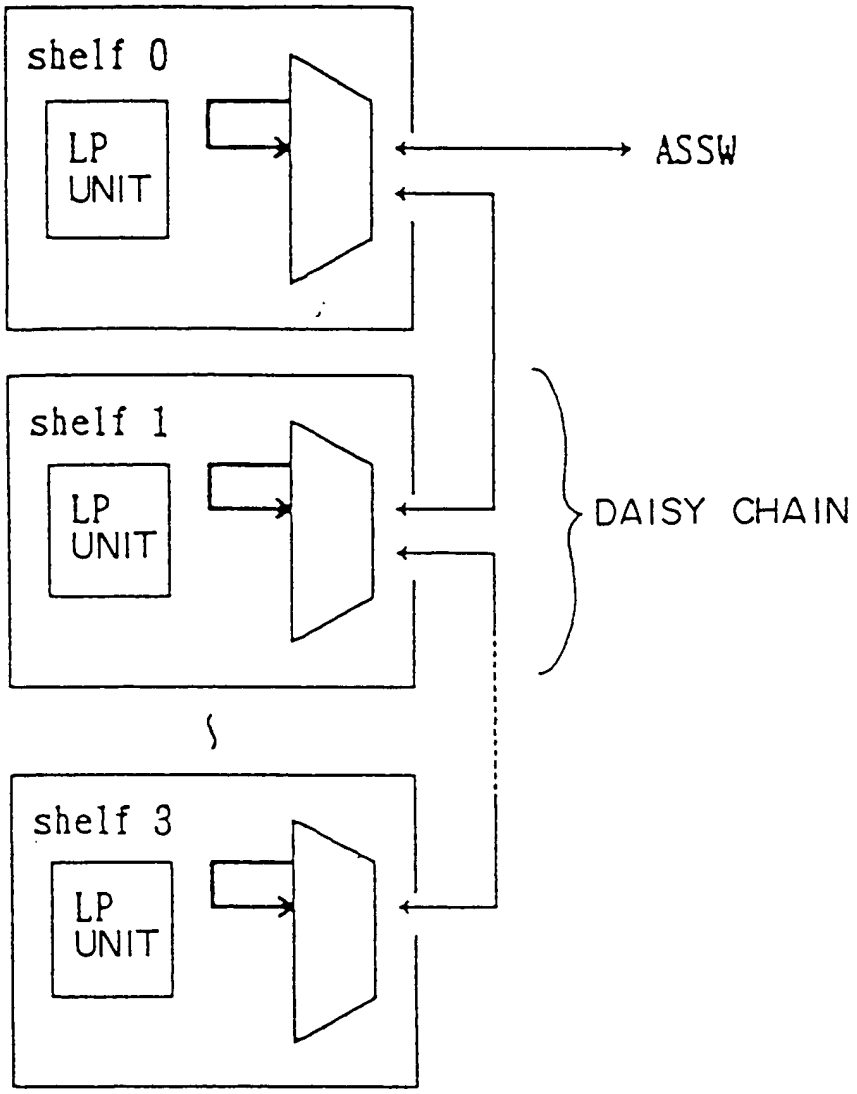

shelf 0
LP UNIT
ASSW
shelf 1
LP UNIT
DAISY CHAIN
shelf 3
LP UNIT

FIG. 461

shelf No.	UL	TAGC	COM	SIG	0
0	0	0	0	0	1
1	0	1	0	0	1
2	0	2	0	0	1
3	0	3	0	0	1

FIG. 462

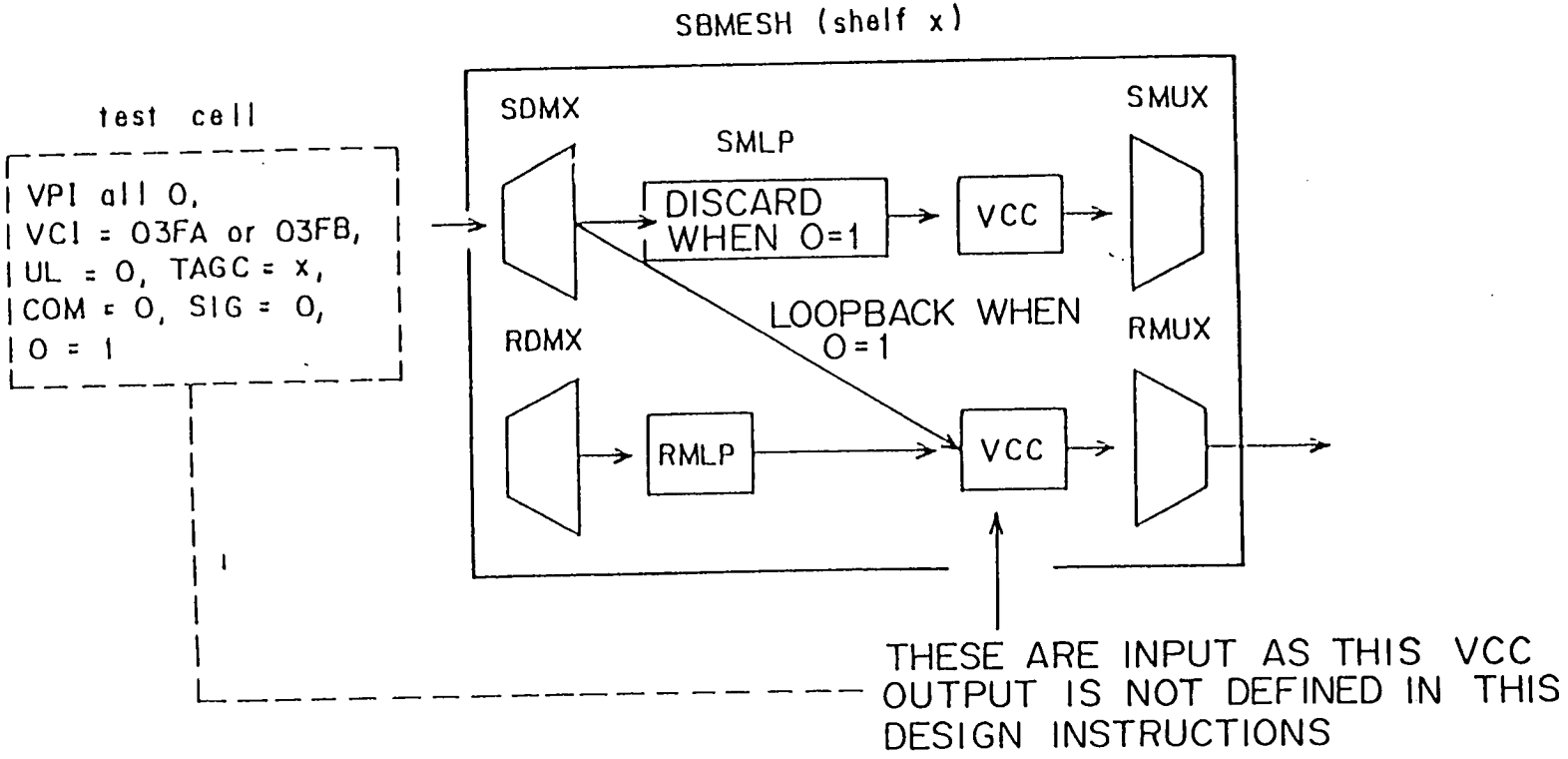
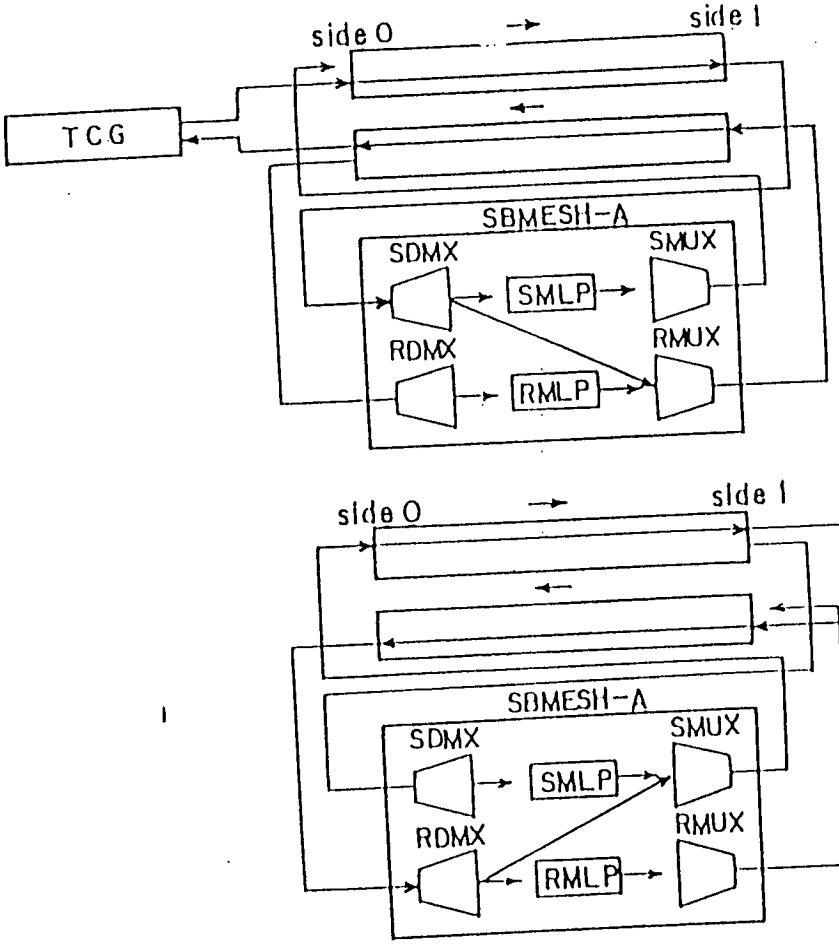

SBMESH (shelf x)
test cell
VPI all 0,
VCI = 03FA or 03FB,
UL = 0, TAGC = x,
COM = 0, SIG = 0,
0 = 1
SDMX
SMLP
DISCARD WHEN 0=1
VCC
SMUX
LOOPBACK WHEN 0=1
RDMX
RMUX
RMLP
VCC
THESE ARE INPUT AS THIS VCC OUTPUT IS NOT DEFINED IN THIS DESIGN INSTRUCTIONS

FIG. 463



UP TO FOUR SBMESHSs ARE CONNECTED AS DAISY CHAIN. LOOPBACK TEST IS CONDUCTED IN EACH SHELF.

UP TO FOUR SBMESHSs ARE CONNECTED AS DAISY CHAIN. LOOPBACK TEST IS CONDUCTED IN EACH SHELF.

FIG. 464

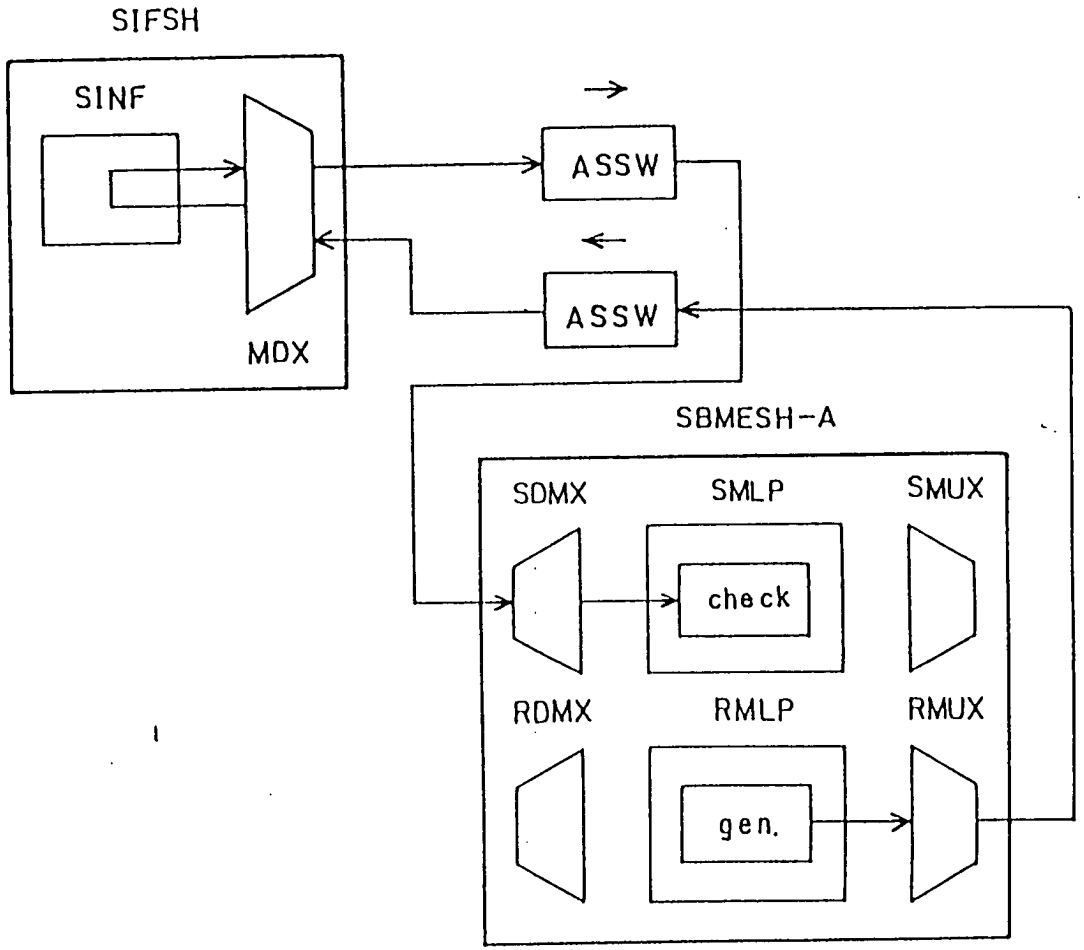

SIFSH
SINF
MDX
ASSW
ASSW
SBMESH-A
SDMX
SMLP
SMUX
check
RDMX
RMLP
RMUX
gen.

FIG. 465

TEST OBJECT	EXISTENCE OF BLOCK	LOOPBACK
SMDS DS1 DT SMDS DS3 DT	BLOCKED	USING LOOP FUNCTION OF LINE (ALL CELLS ARE LOOPED BACK)
ATM DS1 DT ATM DS3 DT SINF UMBILICAL DS3 DT	NOT BLOCKED	USING SPECIFIED VPI/VCI LOOPBACK FUNCTION (TEST CELLS ARE LOOPED BACK)

FIG. 466

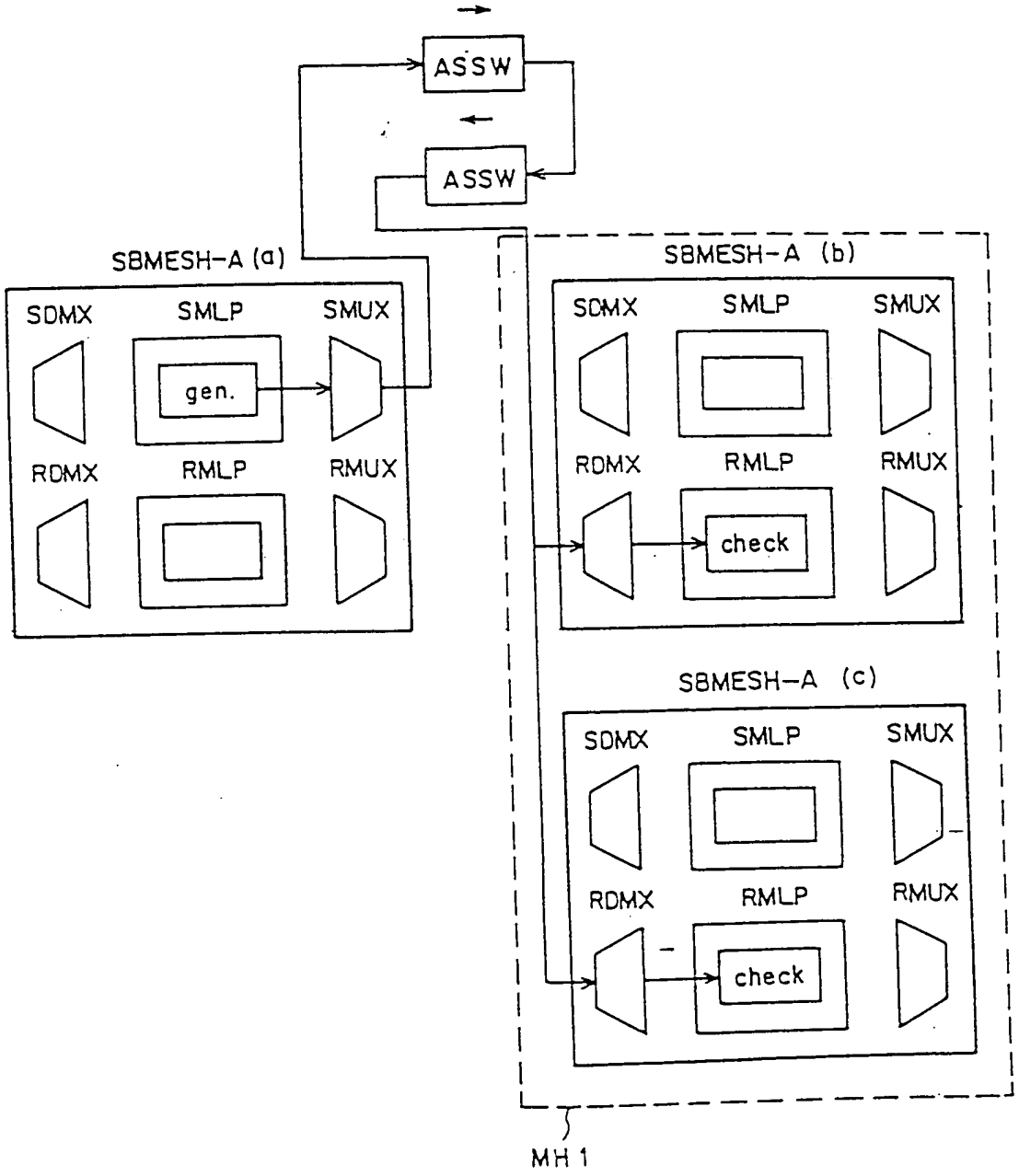
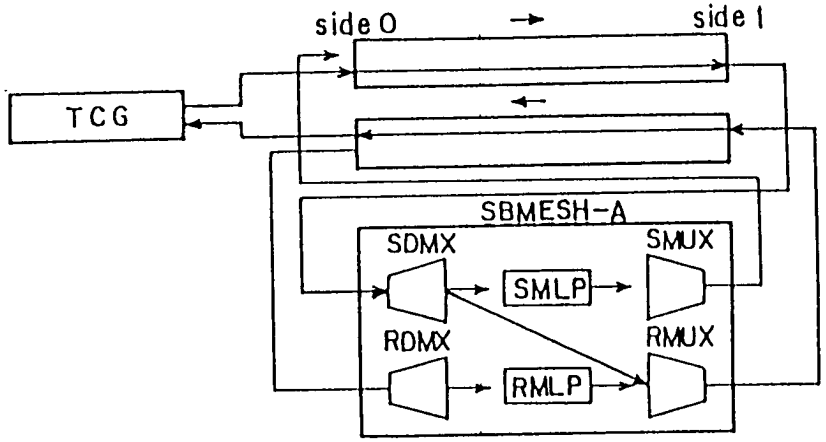
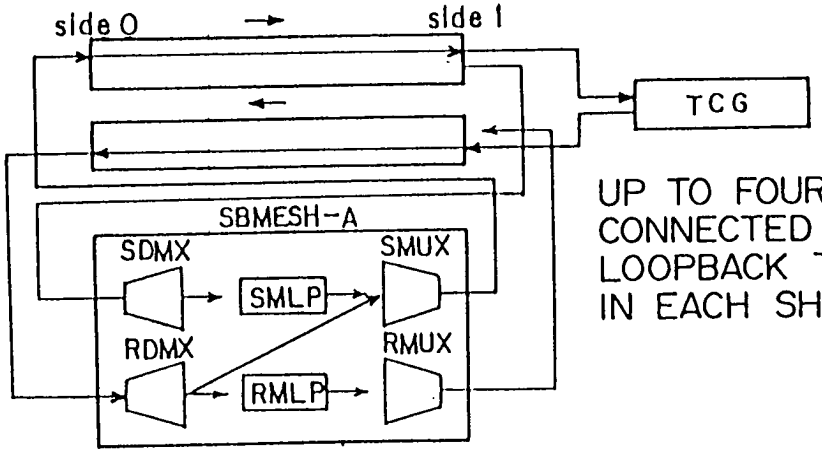

ASSW
ASSW
SBMESH-A (a)
SDMX
SMLP
SMUX
gen.
RDMX
RMLP
RMUX
SBMESH-A (b)
SDMX
SMLP
SMUX
RDMX
RMLP
RMUX
check
SBMESH-A (c)
SDMX
SMLP
SMUX
RDMX
RMLP
RMUX
check
MH 1

FIG. 467



UP TO FOUR SBMESHSs ARE CONNECTED AS DAISY CHAIN. LOOPBACK TEST IS CONDUCTED IN EACH SHELF.



UP TO FOUR SBMESHSs ARE CONNECTED AS DAISY CHAIN. LOOPBACK TEST IS CONDUCTED IN EACH SHELF.

FIG. 468

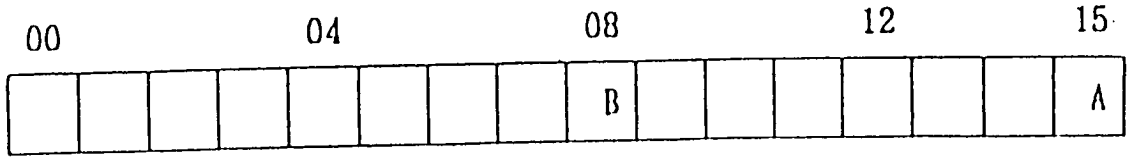
0		8		16		24	31
TEST CELL SENDING UNIT FAULT DISPLAY AREA				TEST CELL RECEIVING UNIT FAULT DISPLAY AREA			
CELL 7	CELL 6	CELL 5	CELL 4	CELL 3	CELL 2	CELL 1	CELL 0
CELL 15	CELL 14	CELL 13	CELL 12	CELL 11	CELL 10	CELL 9	CELL 8
CELL 23	CELL 22	CELL 21	CELL 20	CELL 19	CELL 18	CELL 17	CELL 16
CELL 31	CELL 30	CELL 29	CELL 28	CELL 27	CELL 26	CELL 25	CELL 24
CELL 7	CELL 6	CELL 5	CELL 4	CELL 3	CELL 2	CELL 1	CELL 0
CELL 15	CELL 14	CELL 13	CELL 12	CELL 11	CELL 10	CELL 9	CELL 8
CELL 23	CELL 22	CELL 21	CELL 20	CELL 19	CELL 18	CELL 17	CELL 16
CELL 31	CELL 30	CELL 29	CELL 28	CELL 27	CELL 26	CELL 25	CELL 24
CELL 7	CELL 6	CELL 5	CELL 4	CELL 3	CELL 2	CELL 1	CELL 0
CELL 15	CELL 14	CELL 13	CELL 12	CELL 11	CELL 10	CELL 9	CELL 8
CELL 23	CELL 22	CELL 21	CELL 20	CELL 19	CELL 18	CELL 17	CELL 16
CELL 31	CELL 30	CELL 29	CELL 28	CELL 27	CELL 26	CELL 25	CELL 24

SNI-SBMESH PVC TEST RESULT DISPLAY AREA

MESH-MH PVC TEST RESULT DISPLAY AREA (WHEN SPECIFIC TEST DA IS USED)

MESH-MH PVC TEST RESULT DISPLAY AREA (WHEN ALLOCATED DA IS USED)

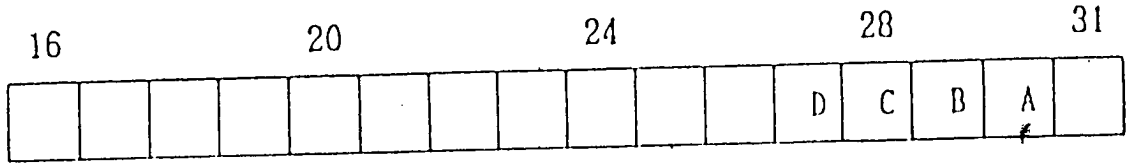
FIG. 469



A : HLP02A I/O add. 0296 D0
B : HLP02A I/O add. 0300 D0
BLANK : 0

FIG. 470

6698201 EP2220



A : HLP02A I/O add. 0296 D1
B : HLP02A I/O add. 0296 D2
C : HLP02A I/O add. 0296 D3
D : HLP02A I/O add. 0296 D4
BLANK : 0

FIG. 471

6692807 EP2726360



FIG. 472

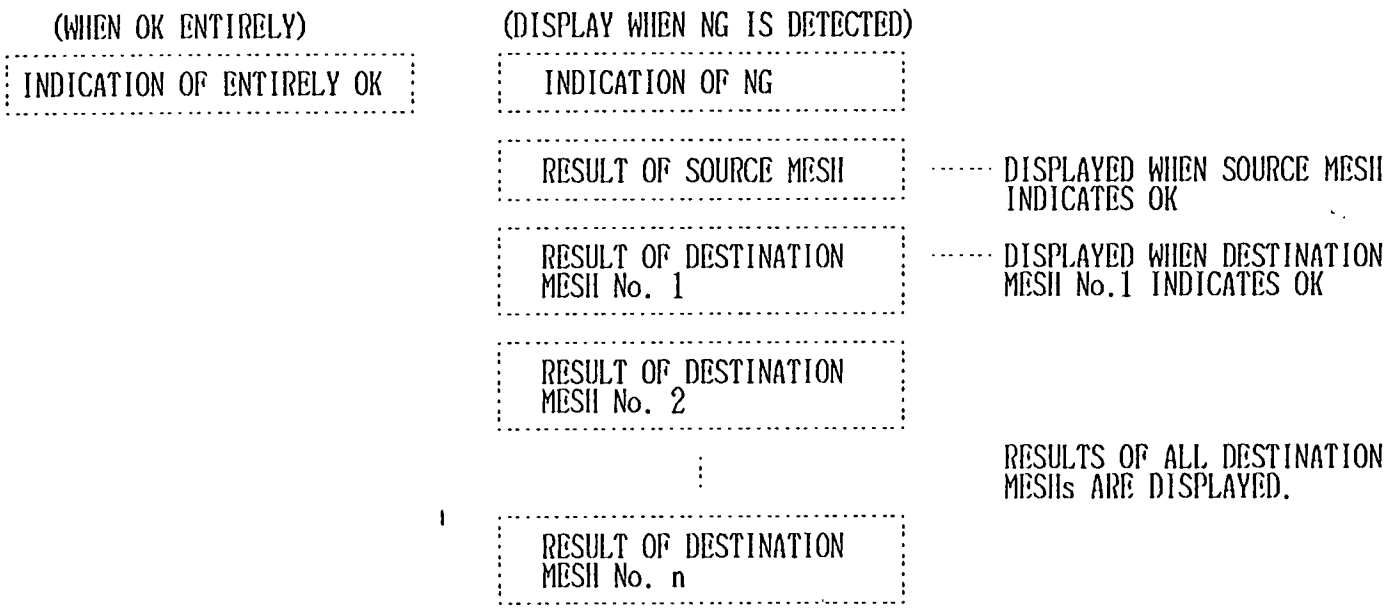

(WHEN OK ENTIRELY)
INDICATION OF ENTIRELY OK
(DISPLAY WHEN NG IS DETECTED)
INDICATION OF NG
RESULT OF SOURCE MESH
DISPLAYED WHEN SOURCE MESH INDICATES OK
RESULT OF DESTINATION MESH No. 1
DISPLAYED WHEN DESTINATION MESH No.1 INDICATES OK
RESULT OF DESTINATION MESH No. 2
RESULTS OF ALL DESTINATION MESHs ARE DISPLAYED.
RESULT OF DESTINATION MESH No. n

FIG. 473

(WHEN OK ENTIRELY)

INDICATION OF ENTIRELY OK

(DISPLAY WHEN NG IS DETECTED)

INDICATION OF NG

RESULT OF SOURCE MESH ..... DISPLAYED WHEN SOURCE MESH INDICATES OK

RESULT OF DESTINATION MESH No. 1 ..... DISPLAYED WHEN DESTINATION MESH No. 1 INDICATES OK

RESULT OF DESTINATION MESH No. 2

⋮

RESULTS OF ALL DESTINATION MESHs ARE DISPLAYED.

RESULT OF DESTINATION MESH No. n

(DISPLAY WHEN RETRIAL IS REQUESTED)

INDICATION OF REQUEST FOR RETRIAL

RESULT OF SOURCE MESH

RESULT OF DESTINATION MESH No. 1 ..... DISPLAYED WHEN DESTINATION MESH No. 1 DOES NOT REQUEST FOR RETRIAL

RESULT OF DESTINATION MESH No. 2

⋮

RESULTS OF ALL DESTINATION MESHs ARE DISPLAYED.

RESULT OF DESTINATION MESH No. n

FIG. 474

	PURPOSE	USE	STORAGE POSITION	ACTIVATION METHOD	REPORT OF RESULT
CONSTRUCTION TP	CONFIRMING NORMALITY OF HARDWARE AFTER COMPLETION OF CONSTRUCTION	FOR ACTUAL CONSTRUCTION	BUILT IN ROM OF HSF05A	AT POWER SUPPLY (INSERTING PWCB INTO SBMESH)	OK/NG INDICATION ON 7 SEG LED
FIRST TEST OF TP	HSF05A CONFIRMING UNIT OPERATION	FIRST TEST UNIT TEST		DIP-SW 01 = ON DIP-SW 02 = ON + ① AT POWER SUPPLY ② RESET SW ON	OK/NG INDICATION ON 7 SEG LED
THIRD TEST OF TP	FOR DEVICE TEST AT DELIVERY FROM FACTORY	MHCOM DELIVERY TEST		DIP-SW 01 = ON DIP-SW 02 = OFF + ① AT POWER SUPPLY ② RESET SW ON	OK/NG INDICATION ON 7 SEG LED
DP	FOR ONLINE DIAGNOSITCS	ON-LINE		AUTOMATIC DIAG-NOSTICS WHEN FAULT OCCURS COMMAND DIAGNOS-TICS	OK/NG INDICATION ON 7 SEG LED REPORT DIAGNOS-TICS RESULT TO COM-E-MSCN

FIG. 475

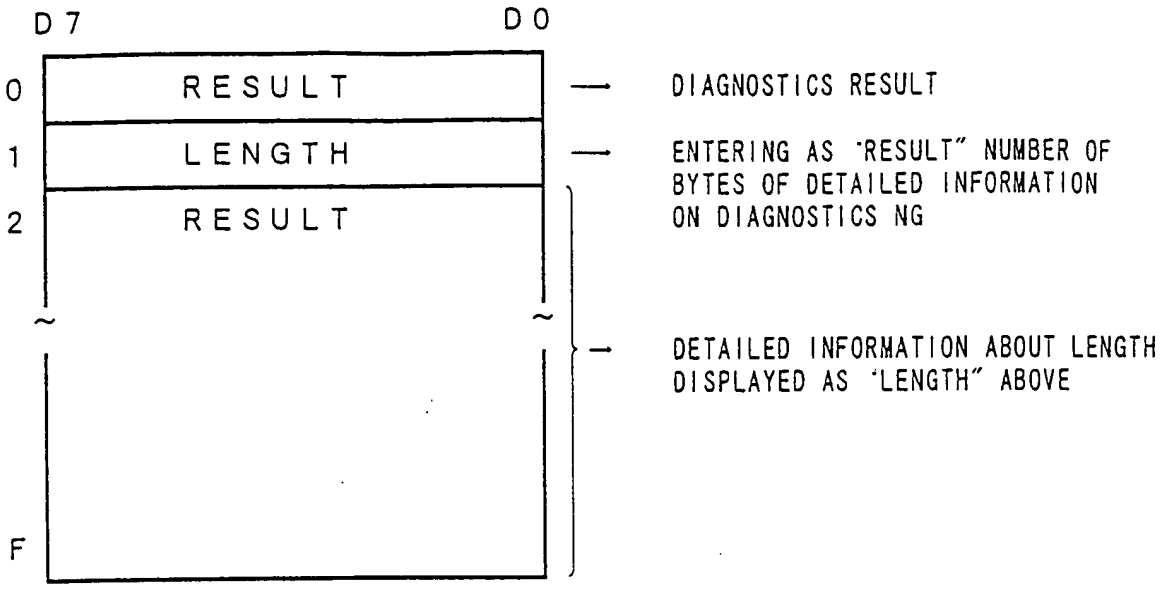
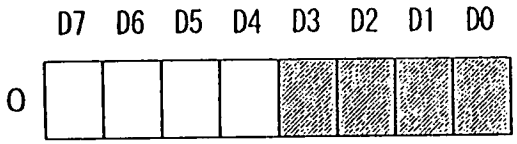

D7
D0
0
RESULT
1
LENGTH
2
RESULT
F
DIAGNOSTICS RESULT
ENTERING AS "RESULT" NUMBER OF BYTES OF DETAILED INFORMATION ON DIAGNOSTICS NG
DETAILED INFORMATION ABOUT LENGTH DISPLAYED AS "LENGTH" ABOVE

FIG. 476



1= DIAGNOSTICS TIMEOUT
1= POWER DISCONNECTION IN MATE SYSTEM
0= HOME SYSTEM DIAGNOSTICS RESULT INDICATION
1= MATE SYSTEM DIAGNOSTICS RESULT INDICATION

} THESE ARE ASSIGNED BY DIAGNOSTICS ACTIVATION TASK AFTER COMPLETION OF DIAGNOSTICS.

ALL 0 IN D0 THROUGH D6 WHEN DIAGNOSTICS INDICATES OK.

D0~D3 : 1 = CNT PWCB (HSF05A) NG
2 = SMUX/RDMX PWCB (HMX10A) NG
3 = RMUX/SDMX PWCB (HMX11A) NG
4 = VCC/SCHED PWCB (HMX12A) NG

FIG. 477

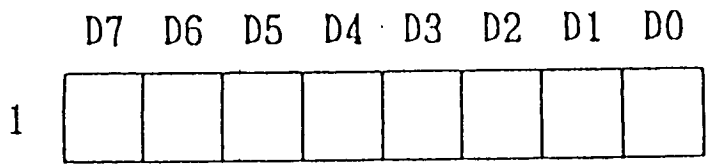


FIG. 478

	D7	D0
2	Di LOWER ORDER BYTE (D7~D0)	
3	Di HIGHER ORDER BYTE (D15~D8)	
4	Ax LOWER ORDER BYTE (D7~D0)	
5	Ax HIGHER ORDER BYTE (D15~D8)	
6	Bx LOWER ORDER BYTE (D7~D0)	
7	Bx HIGHER ORDER BYTE (D15~D8)	
8	Cx LOWER ORDER BYTE (D7~D0)	
9	Cx HIGHER ORDER BYTE (D15~D8)	
~	Don't care	~
F		

FIG. 479

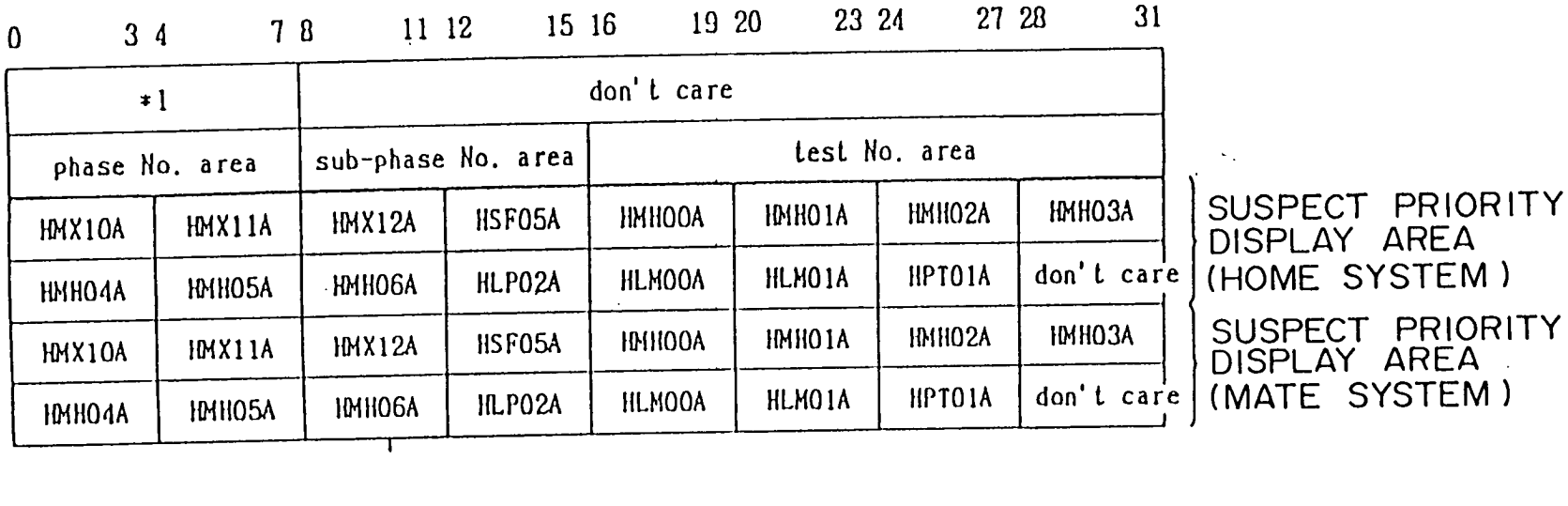

0 3 4 7 8 11 12 15 16 19 20 23 24 27 28 31
*1
don't care
phase No. area
sub-phase No. area
test No. area
HMX10A
HMX11A
HMX12A
HSF05A
HMH00A
HMH01A
HMH02A
HMH03A
HMH04A
HMH05A
HMH06A
HLP02A
HLM00A
HLM01A
HPT01A
don't care
HMX10A
HMX11A
HMX12A
HSF05A
HMH00A
HMH01A
HMH02A
HMH03A
HMH04A
HMH05A
HMH06A
HLP02A
HLM00A
HLM01A
HPT01A
don't care
SUSPECT PRIORITY DISPLAY AREA (HOME SYSTEM)
SUSPECT PRIORITY DISPLAY AREA (MATE SYSTEM)

FIG. 480

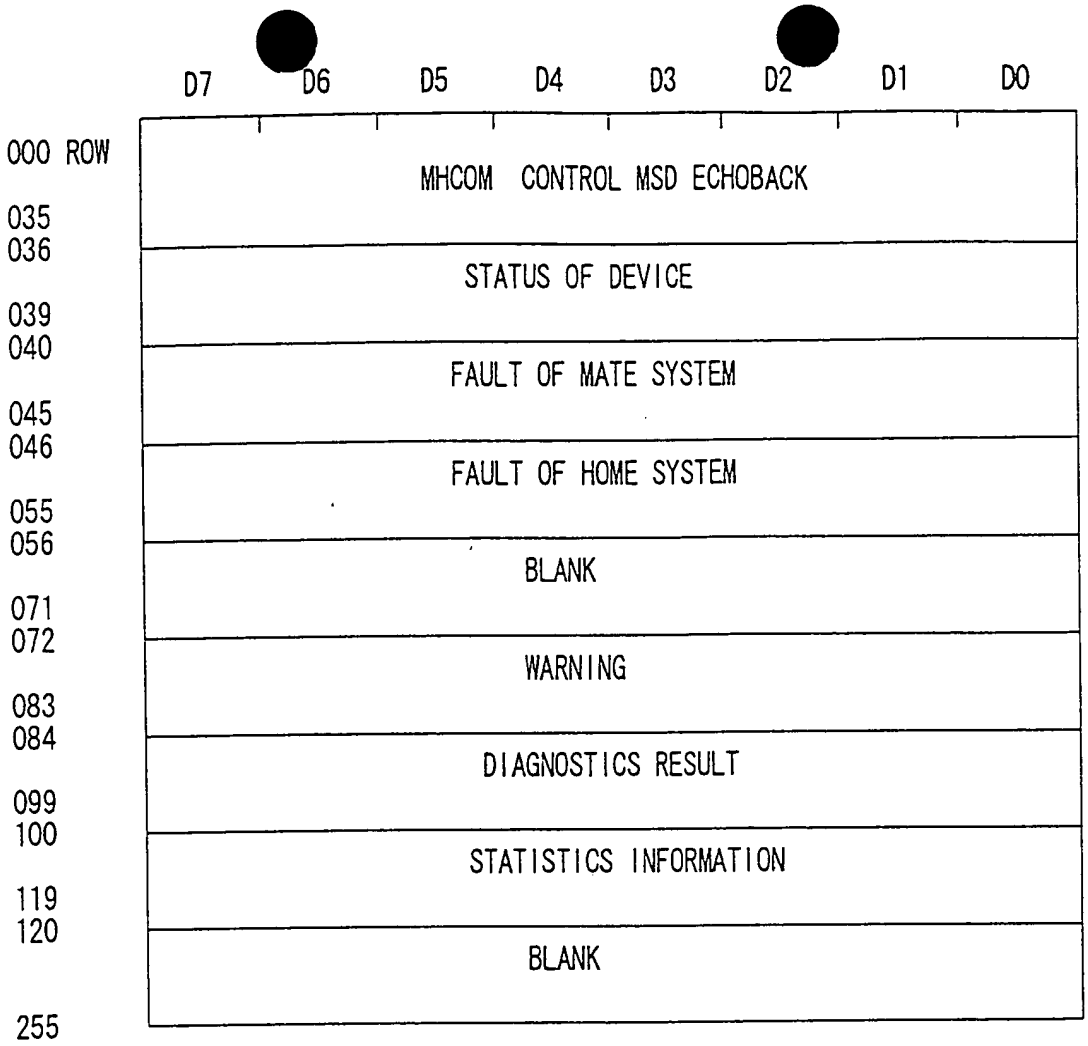

D7
D6
D5
D4
D3
D2
D1
D0
000 ROW
035
036
039
040
045
046
055
056
071
072
083
084
099
100
119
120
255
MHCOM CONTROL MSD ECHOBACK
STATUS OF DEVICE
FAULT OF MATE SYSTEM
FAULT OF HOME SYSTEM
BLANK
WARNING
DIAGNOSTICS RESULT
STATISTICS INFORMATION
BLANK

FIG. 481

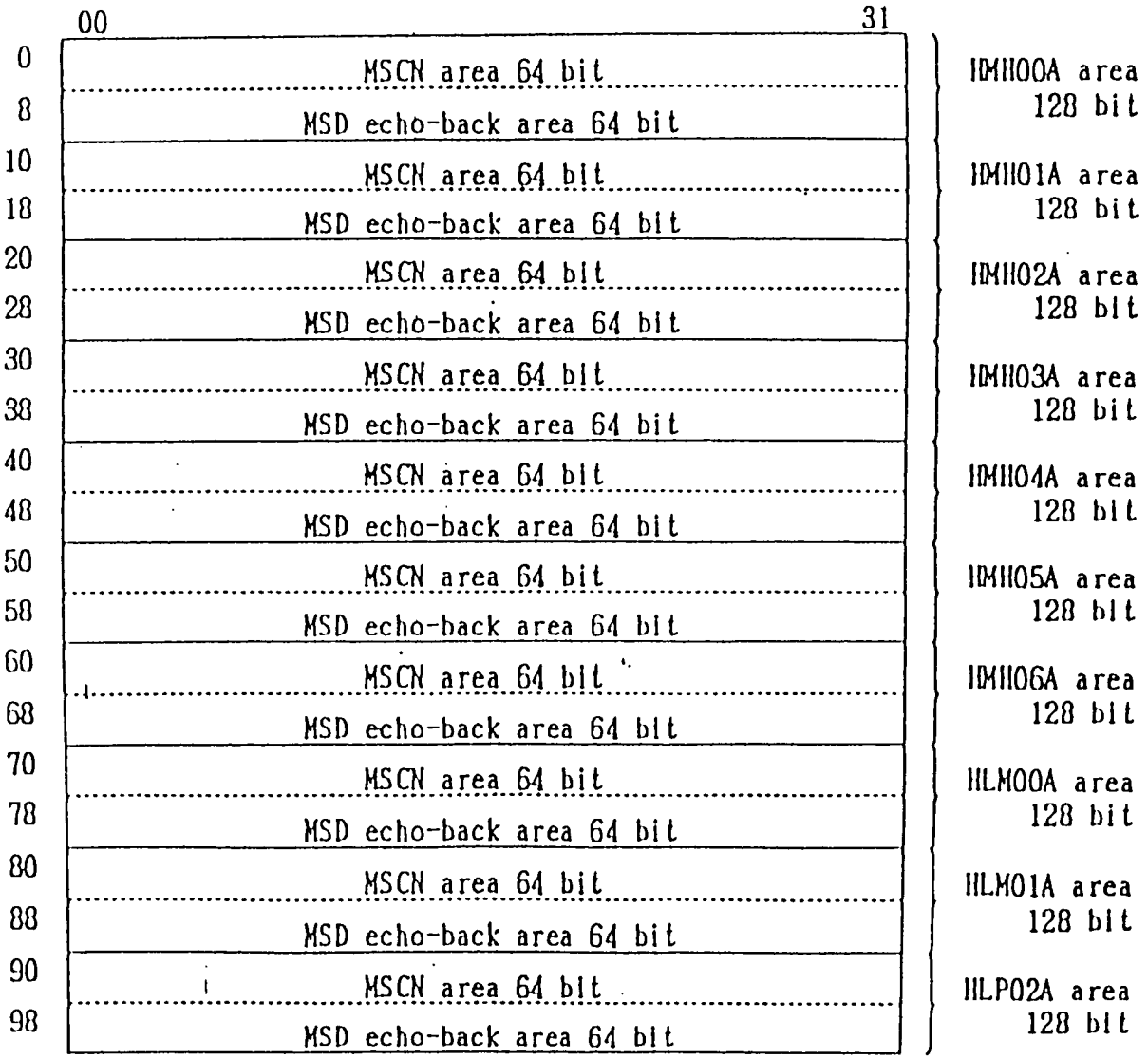

00
31
0
MSCN area 64 bit
8
MSD echo-back area 64 bit
IMH00A area 128 bit
10
MSCN area 64 bit
18
MSD echo-back area 64 bit
IMH01A area 128 bit
20
MSCN area 64 bit
28
MSD echo-back area 64 bit
IMH02A area 128 bit
30
MSCN area 64 bit
38
MSD echo-back area 64 bit
IMH03A area 128 bit
40
MSCN area 64 bit
48
MSD echo-back area 64 bit
IMH04A area 128 bit
50
MSCN area 64 bit
58
MSD echo-back area 64 bit
IMH05A area 128 bit
60
MSCN area 64 bit
68
MSD echo-back area 64 bit
IMH06A area 128 bit
70
MSCN area 64 bit
78
MSD echo-back area 64 bit
HLM00A area 128 bit
80
MSCN area 64 bit
88
MSD echo-back area 64 bit
HLM01A area 128 bit
90
MSCN area 64 bit
98
MSD echo-back area 64 bit
HLP02A area 128 bit

FIG. 482

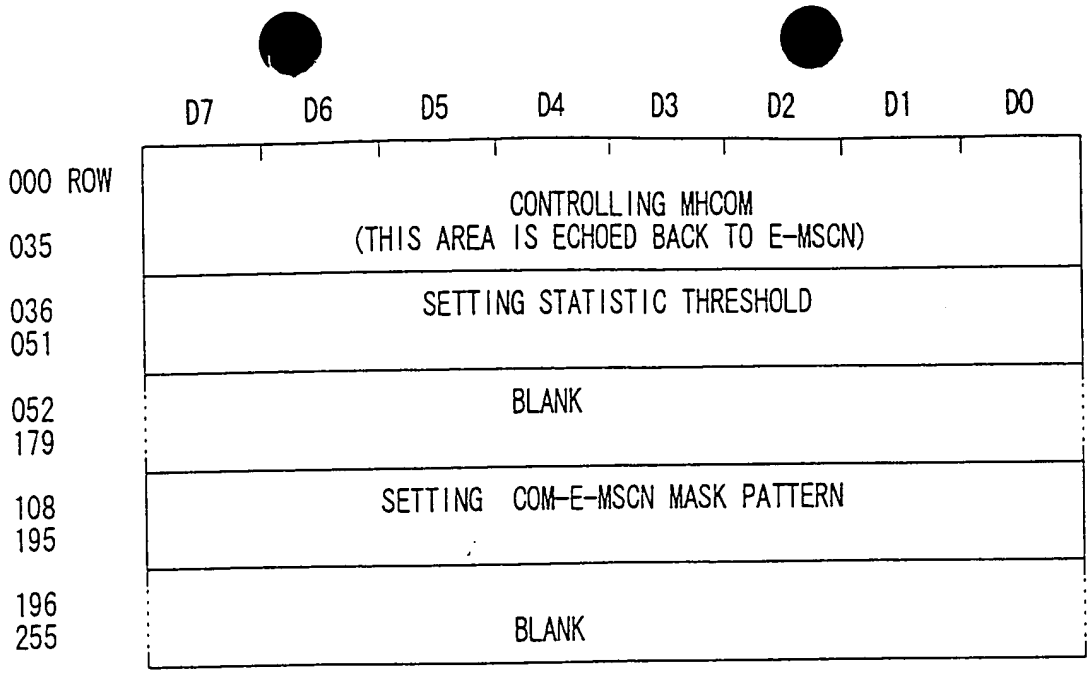


FIG. 483

6,052,364 2,000,000

ROW	D7	D6	D5	D4	D3	D2	D1	D0	
0	RESETTING MATE SYSTEM	RESETTING HOME SYSTEM							
1					PRESENT OS	MATE SYSTEM SHALM	MATE SYSTEM SHOS	MATE SYSTEM OS	
2							SELECTING OL2B	SELECTING OL2A	
3							HOME SYSTEM DIAGNOSTICS ACTIVATION	MATE SYSTEM DIAGNOSTICS ACTIVATION	
4									
5	MSB	SPECIFYING INTRA-STATION LAP BAND							
6	(SPECIFYING VALUE n FOR 64 KBPS X n. VARIABLE 1~4075)							LSB	
7 23									
24				DEMUX 15-MINUTE NOTIFICATION	START OF STATISTICS		MUX 15-MINUTE NOTIFICATION	START OF STATISTICS	SMLP
25							MUX 15-MINUTE NOTIFICATION	START OF STATISTICS	RMLP
26				DEMUX 15-MINUTE NOTIFICATION	START OF STATISTICS				R-TCG
27 31									
32				DEMUX 15-MINUTE NOTIFICATION	START OF STATISTICS		MUX 15-MINUTE NOTIFICATION	START OF STATISTICS	h-SIG
33 35									

FIG. 484

0927213.032509

POINT NAME	STORAGE POSITION	EXPLANATION
RESETTING MATE SYSTEM	0 ROW D7	RESET INSTRUCTION POINT OF MATE SYSTEM MHCOM. AUTOMATIC RESET POINT. SETTING THIS POINT DISCONNECTS INTRA-STATION COMMUNICATIONS LAP.
RESETTING HOME SYSTEM	0 ROW D6	RESET INSTRUCTION POINT OF HOME SYSTEM MHCOM. AUTOMATIC RESET POINT. SETTING THIS POINT DISCONNECTS INTRA-STATION COMMUNICATIONS LAP.
PRESENT OS	1 ROW D3	LIGHTING LAMP INDICATING PRESENT OS BY SETTING THIS POINT.
MATE SYSTEM SHALM	1 ROW D2	LIGHTING LAMP (ACCOMMODATED IN HPT01A) INDICATING MATE SYSTEM SHELF ALM BY SETTING THIS POINT.
MATE SYSTEM SHOS	1 ROW D1	LIGHTING LAMP (ACCOMMODATED IN HPT01A) INDICATING MATE SYSTEM SHELF OS BY SETTING THIS POINT.
MATE SYSTEM SHOS	1 ROW D0	LIGHTING LAMP (ACCOMMODATED IN HSF05A) INDICATING MATE SYSTEM MHCOM OS BY SETTING THIS POINT.
SELECTING OL2B	2 ROW D1	COMPULSORILY SELECTING OPTICAL 8MCLK #1 BY CHANGING THIS POINT FROM RESET TO SET.
SELECTING OL2A	2 ROW D0	COMPULSORILY SELECTING OPTICAL 8MCLK #0 BY CHANGING THIS POINT FROM RESET TO SET.
HOME SYSTEM DIAGNOSTICS ACTIVATION	3 ROW D1	PERFORMING ONLINE DP IN HOME SYSTEM BY CHANGING THIS POINT FROM RESET TO SET. IF HOME SYSTEM IS ACT, IT IS NOT PERFORMED.
MATE SYSTEM DIAG-NOSTICS ACTIVATION FIFO FULL	3 ROW D0	REQUESTING MATE SYSTEM TO PERFORM ONLINE DP IN HOME SYSTEM BY CHANGING THIS POINT FROM RESET TO SET. IF MATE SYSTEM IS ACT, THE REQUEST IS IGNORED.
	5 ~6 ROW	· SPECIFYING BAND OF INTRA-STATION LAP. D7 D0 MSB ← BAND OF INTRA-STATION LAP → LSB SPECIFYING n FOR 64 KBPS X n (n=1 ~4075) DEFAULT IS n = 1
SDMX 15-MINUTE NOTIFICATION	24 ROW D4	15-MINUTE NOTIFICATION FOR STATISTIC PROCESS OF SDMX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
SDMX START OF STATISTICS	24 ROW D3	INSTRUCTING TO START STATISTIC PROCESS OF SDMX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
SMUX 15-MINUTE NOTIFICATION	24 ROW D1	15-MINUTE NOTIFICATION FOR STATISTIC PROCESS OF SMUX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
SMUX START OF STATISTICS	24 ROW D0	INSTRUCTING TO START STATISTIC PROCESS OF SMUX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
RMUX 15-MINUTE NOTIFICATION	25 ROW D1	15-MINUTE NOTIFICATION FOR STATISTIC PROCESS OF RMUX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
RMUX START OF STATISTICS	25 ROW D0	INSTRUCTING TO START STATISTIC PROCESS OF RMUX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.

FIG. 485

POINT NAME	STORAGE POSITION	EXPLANATION
RTCG-DMX 15-MINUTE NOTIFICATION	26 ROW D4	15-MINUTE NOTIFICATION FOR STATISITC PROCESS OF RTCG-DMX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
RTCG-MDX START OF STATISTICS	26 ROW D3	INSTRUCTING TO START STATISTIC PROCESS OF RTCG-DMX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-DMX 15-MINUTE NOTIFICATION	32 ROW D4	15-MINUTE NOTIFICATION FOR STATISITC PROCESS OF HOME SIG-DMX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-DMX START OF STATISTICS	32 ROW D3	INSTRUCTING TO START STATISTIC PROCESS OF SIG-DMX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-MUX 15-MINUTE NOTIFICATION	32 ROW D1	15-MINUTE NOTIFICATION FOR STATISITC PROCESS OF HOME SIG-MUX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-MUX START OF STATISTICS	32 ROW D0	INSTRUCTING TO START STATISTIC PROCESS OF SIG-MUX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.

FIG. 486

ROW	D7	D6	D5	D4	D3	D2	D1	D0
36								
37								
38			DMUX	MUX	Unit No.			
39	Q1							
40	QA							
41	QA'							
42	QB							
43	QB'							
44	QC							
45	QC'							
46	QD							
47	QD'							
48	0	0	0	0	SPECIFIC VCI			
49	SPECIFIC VCI							
50	SPECIFIC VCI							
51	SPECIFIC VCI							

FIG. 487

POINT NAME	STORAGE POSITION	EXPLANATION
DEMUX MUX UNIT No.	38 ROW	・PARAMETER GROUP SPECIFYING FOR WHICH STATISTIC INFORMATION COLLECTION POINT STATISTIC THRESHOLD VALUE IS SET. ROW 102 D7 … D0: [ ][DMUX][MUX][MSB ← UNIT No. → LSB] DUMX .... "1" INDICATES THAT THRESHOLD IS SET FOR DEMULTIPLEXER. MUX .... "1" INDICATES THAT THRESHOLD IS SET FOR MULTIPLEXER. ※ DMUX AND MUX CANNOT BE SIMULTANEOUSLY SET TO 1. IF BOTH FIELDS ARE SIMULTANEOUSLY SET TO 1. MHCOM RECOGNIZES SETTINGS. UNIT No. .... INDICATES FOR WHICH LINE THRESHOLD IS SET (REFER TO FOLLOWING TABLE.)

UNIT No.	LINE TYPE	MUX	DEMUX
0	SMLP	○	○
1	RMLP	○	×
2	R-TCG	×	○
8	HOME SYSTEM INTRA-STATION COMMUNICATIONS	○	○

INDICATES EXISTENCE OF MUX/DEMUX IN EACH LINE.

※ NO COMBINATION IS MADE AMONG X-MARKED MUX, DEMUX, AND UNIT No. (BECAUSE CORRESPONDING POINT DOES NOT CONTAIN MUX AND DEMUX). WHEN X-MARKED COMBINATION IS SET, MHCOM IGNORES IT.

Q1 LOGICAL THRESHOLD VALUE	39 ROW	・LOGICAL THRESHOLD VALUE IS SET FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS Q1, CELLS SRE DISCARDED. THRESHOLD IS SET IN RANGE OF 0~70(H). ROW 39 D7 … D0: [ ][MSB ← Q1(LOGICAL THRESHOLD VALUE) →LSB] ※ DEFAULT IS MAXIMUM VALUE (112 CELLS).
QA, QA' (DISCARD START/RELEASE THRESHOLD FOR CELL OF P=0, CON=0.)	40, 41ROW	・QA ... DISCARD START THRESHOLD FOR CELL OF P=0, CON=0 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS QA, DISCARD OF CELL OF P=0, CON=0 IS STARTED. ・QA' ... DISCARD RELEASE THRESHOLD FOR CELL OF P=0, CON=0 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER DOES NOT EXCEEDS QA', DISCARD OF CELL OF P=0, CON=0 IS RELEASED. ROW 40(41) D7 … D0: [ ][MSB ← QA(QA') → LSB] ※ DEFAULT IS MAXIMUM VALUE (112 CELLS). $0 < QA' \leqq QA$

FIG. 488

POINT NAME	STORAGE POSITION	EXPLANATION
QB, QB' (DISCARD START/RELEASE THRESHOLD FOR CELL OF P=0, CON=1.)	42, 43ROW	・QB ... DISCARD START THRESHOLD FOR CELL OF P=0, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS QB, DISCARD OF CELL OF P=0, CON=1 IS STARTED. ・QB' ... DISCARD RELEASE THRESHOLD FOR CELL OF P=0, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER DOES NOT EXCEEDS QB', DISCARD OF CELL OF P=0, CON=1 IS RELEASED. ROW D7 D0 42 (43) MSB ← QB (QB') → LSB ※ DEFAULT IS MAXIMUM VALUE (112 CELLS). $0 < QB' \leqq QB$
QC, QC' (DISCARD START/RELEASE THRESHOLD FOR CELL OF P=1, CON=0.)	42, 43ROW	・QC ... DISCARD START THRESHOLD FOR CELL OF P=1, CON=0 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS QC, DISCARD OF CELL OF P=1, CON=0 IS STARTED. ・QC' ... DISCARD RELEASE THRESHOLD FOR CELL OF P=1, CON=0 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER DOES NOT EXCEEDS QC', DISCARD OF CELL OF P=1, CON=0 IS RELEASED. ROW D7 D0 44 (45) MSB ← QC (QC') → LSB ※ DEFAULT IS MAXIMUM VALUE (112 CELLS). $0 < QC' \leqq QC$
QD, QD' (DISCARD START/RELEASE THRESHOLD FOR CELL OF P=1, CON=1.)	42, 43ROW	・QD ... DISCARD START THRESHOLD FOR CELL OF P=1, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS QD, DISCARD OF CELL OF P=1, CON=1 IS STARTED. ・QD' ... DISCARD RELEASE THRESHOLD FOR CELL OF P=1, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER DOES NOT EXCEEDS QD', DISCARD OF CELL OF P=1, CON=1 IS RELEASED. ROW D7 D0 46 (47) MSB ← QD (QD') → LSB ※ DEFAULT IS MAXIMUM VALUE (112 CELLS). $0 < QD' \leqq QD$
SPECIFIC VPI/VCI	48 ~ 51 ROW	・SPECIFYING SPECIFIC VPI/VCI TO MONITOR NUMBER OF PASSING CELLS IN POINT SPECIFIED BY 38ROW. ROW D7 D0 48 MSB ← 49 SPECIFIC VPI (12) → LSB 50 MSB ← 51 SPECIFIC VCI (16) → LSB

FIG. 489

ROW	D7	D6	D5	D4	D3	D2	D1	D0
52 179				BLANK				
180	8							1WORD
181	16							9
182	24							17
183	32							25
184	40							33
185	48							41
186	56							49
187	64							57
188	72							65
189	80							-73
190	88							81
191	96				-			89
192	104							97
193	112							105
194	120							113
195	128							121

* MASK WORD WHICH IS SET TO "1".

FIG. 490

POINT NAME	STORAGE POSITION	EXPLANATION
SPECIFYING MASK	180 \ 195 ROW	· SPECIFYING MASK PATTERN OF COM-E-MSCN IN WORD UNIT.

E-MSD ROW No.	BIT POSITION	ROW NO. OF MASKED E-MSCN
180	D0	0, 1
	1	2, 3
	2	4, 5
	3	6, 7
	4	8, 9
	5	10, 11
	6	12, 13
	7	14, 15
181	D0	16, 17
194	D7	238, 239
195	D0	240, 241
	1	242, 243
	2	244, 245
	3	246, 247
	4	248, 249
	5	250, 251
	6	252, 253
	7	254, 255

※ "1" INDICATES MASKING.

FIG. 491

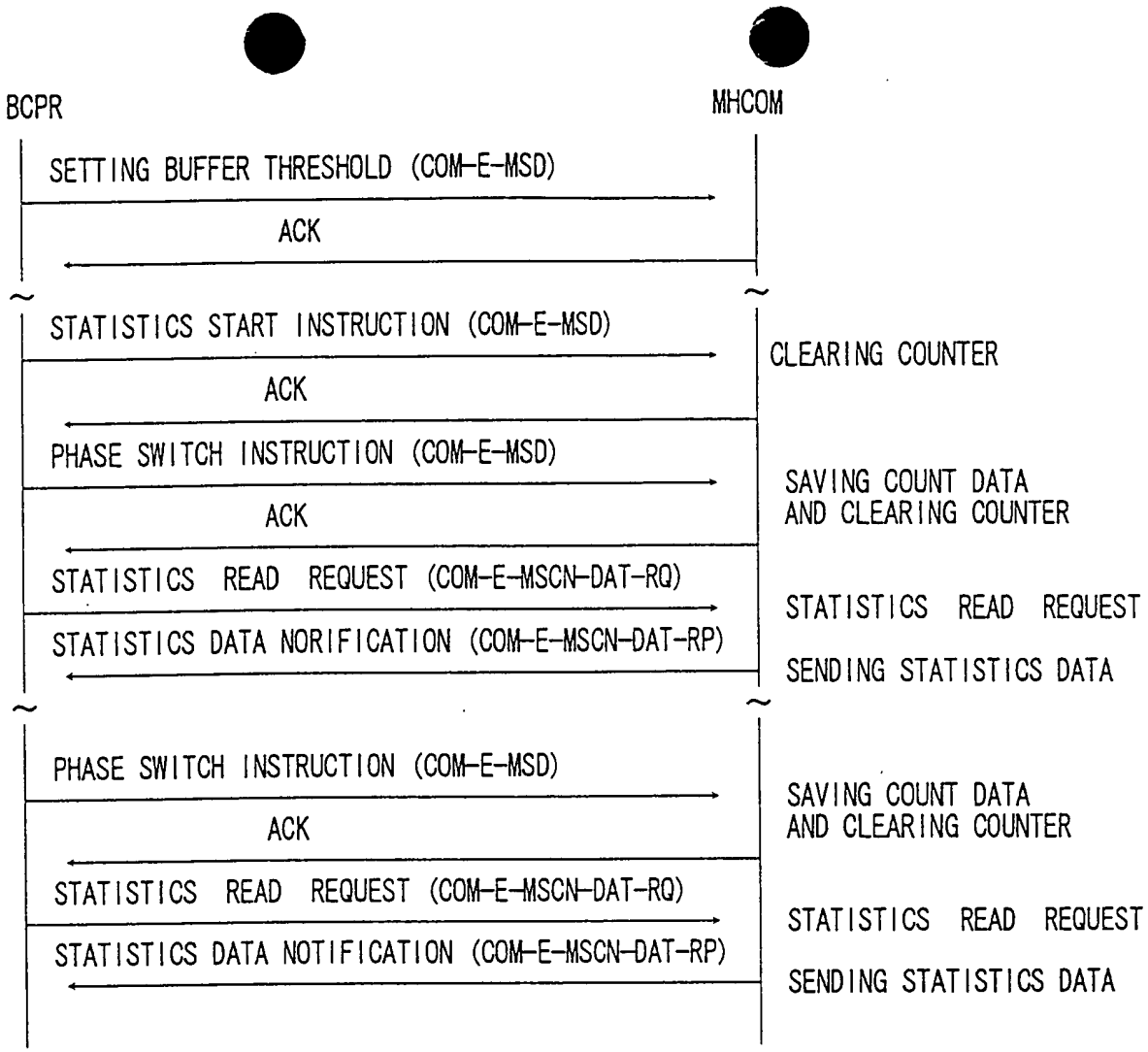
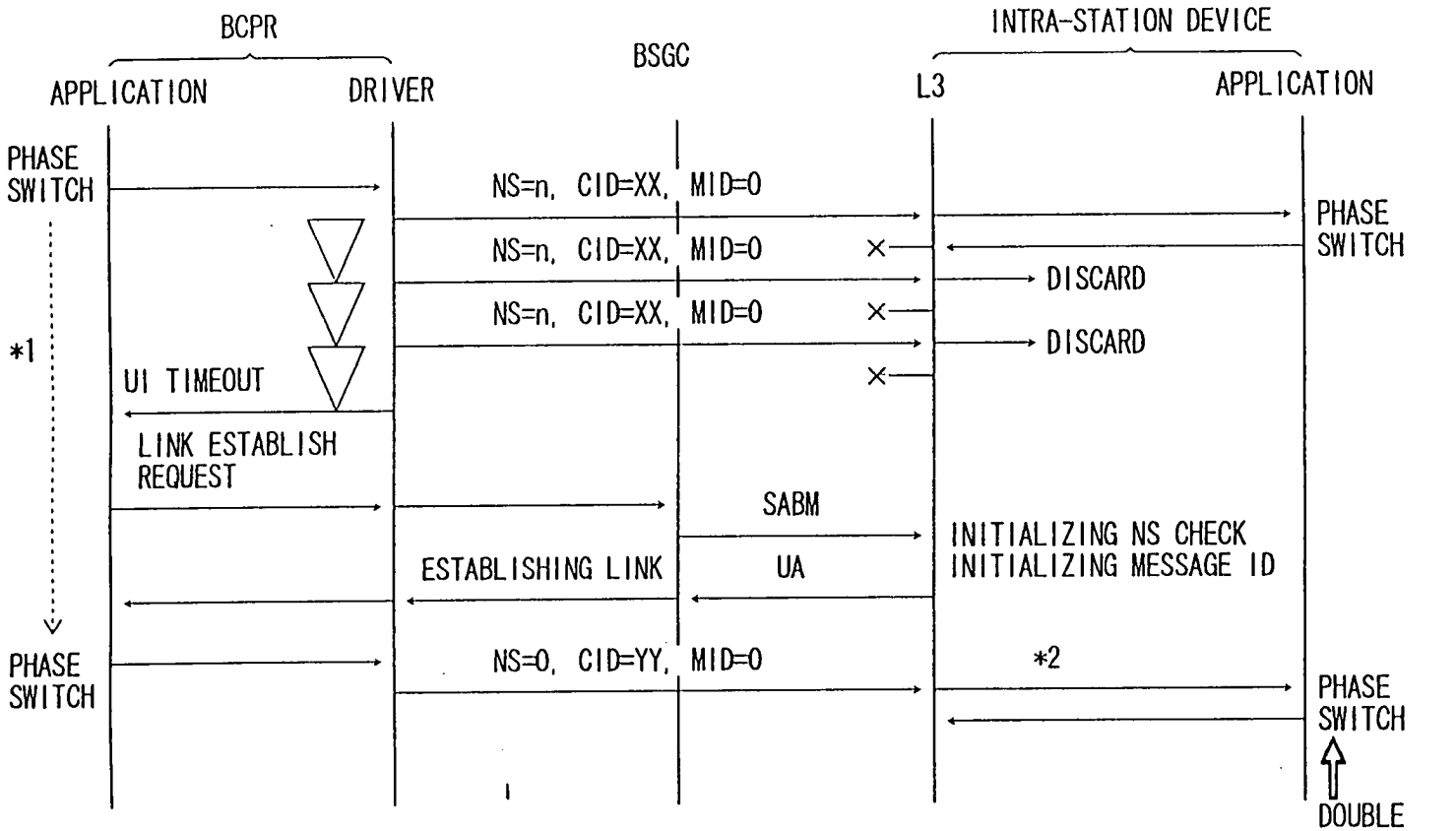

BCPR
MHCOM
SETTING BUFFER THRESHOLD (COM-E-MSD)
ACK
STATISTICS START INSTRUCTION (COM-E-MSD)
CLEARING COUNTER
ACK
PHASE SWITCH INSTRUCTION (COM-E-MSD)
SAVING COUNT DATA AND CLEARING COUNTER
ACK
STATISTICS READ REQUEST (COM-E-MSCN-DAT-RQ)
STATISTICS READ REQUEST
STATISTICS DATA NORIFICATION (COM-E-MSCN-DAT-RP)
SENDING STATISTICS DATA
PHASE SWITCH INSTRUCTION (COM-E-MSD)
SAVING COUNT DATA AND CLEARING COUNTER
ACK
STATISTICS READ REQUEST (COM-E-MSCN-DAT-RQ)
STATISTICS READ REQUEST
STATISTICS DATA NOTIFICATION (COM-E-MSCN-DAT-RP)
SENDING STATISTICS DATA

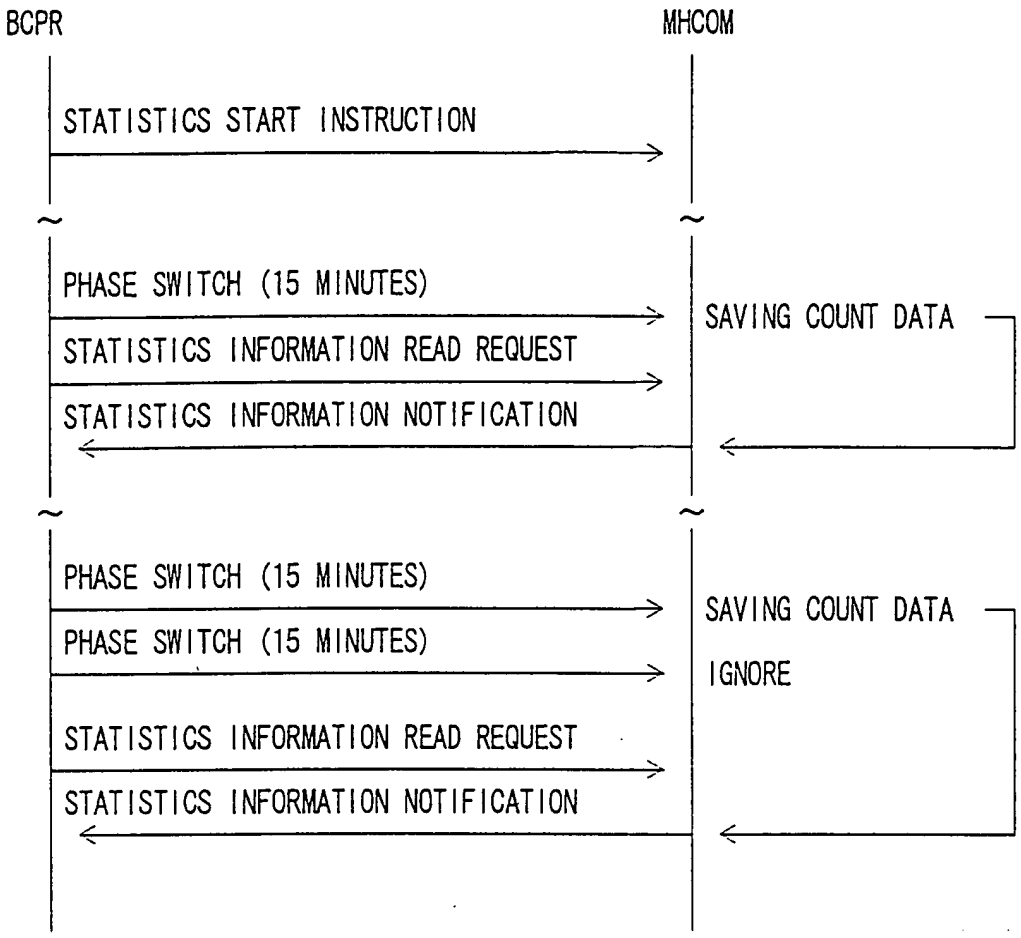
FIG. 492



*1 : COMMAND IS NOT COMPLETED AND RESET REQUEST IS ISSUED AFTER LINK IS RE-ESTABLISHED.

*2 : COMMAND IS SET DOUBLE BECAUSE DEVICE L3 DETERMINES NORMAL SEQUENCE.

FIG. 493


BCPR
MHCOM
STATISTICS START INSTRUCTION
PHASE SWITCH (15 MINUTES)
SAVING COUNT DATA
STATISTICS INFORMATION READ REQUEST
STATISTICS INFORMATION NOTIFICATION
PHASE SWITCH (15 MINUTES)
SAVING COUNT DATA
PHASE SWITCH (15 MINUTES)
IGNORE
STATISTICS INFORMATION READ REQUEST
STATISTICS INFORMATION NOTIFICATION

F I G. 494

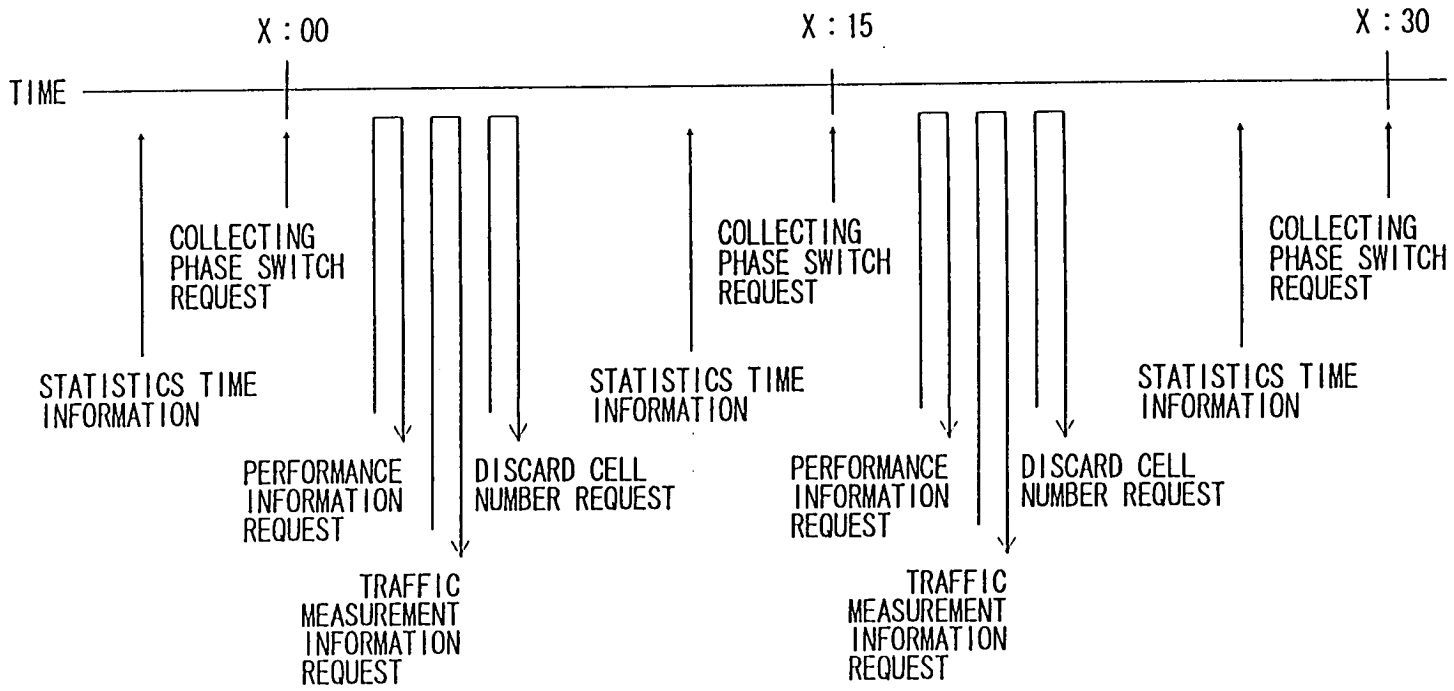

X : 00
X : 15
X : 30
TIME
COLLECTING PHASE SWITCH REQUEST
STATISTICS TIME INFORMATION
PERFORMANCE INFORMATION REQUEST
DISCARD CELL NUMBER REQUEST
TRAFFIC MEASUREMENT INFORMATION REQUEST
COLLECTING PHASE SWITCH REQUEST
STATISTICS TIME INFORMATION
PERFORMANCE INFORMATION REQUEST
DISCARD CELL NUMBER REQUEST
TRAFFIC MEASUREMENT INFORMATION REQUEST
COLLECTING PHASE SWITCH REQUEST
STATISTICS TIME INFORMATION

FIG. 495

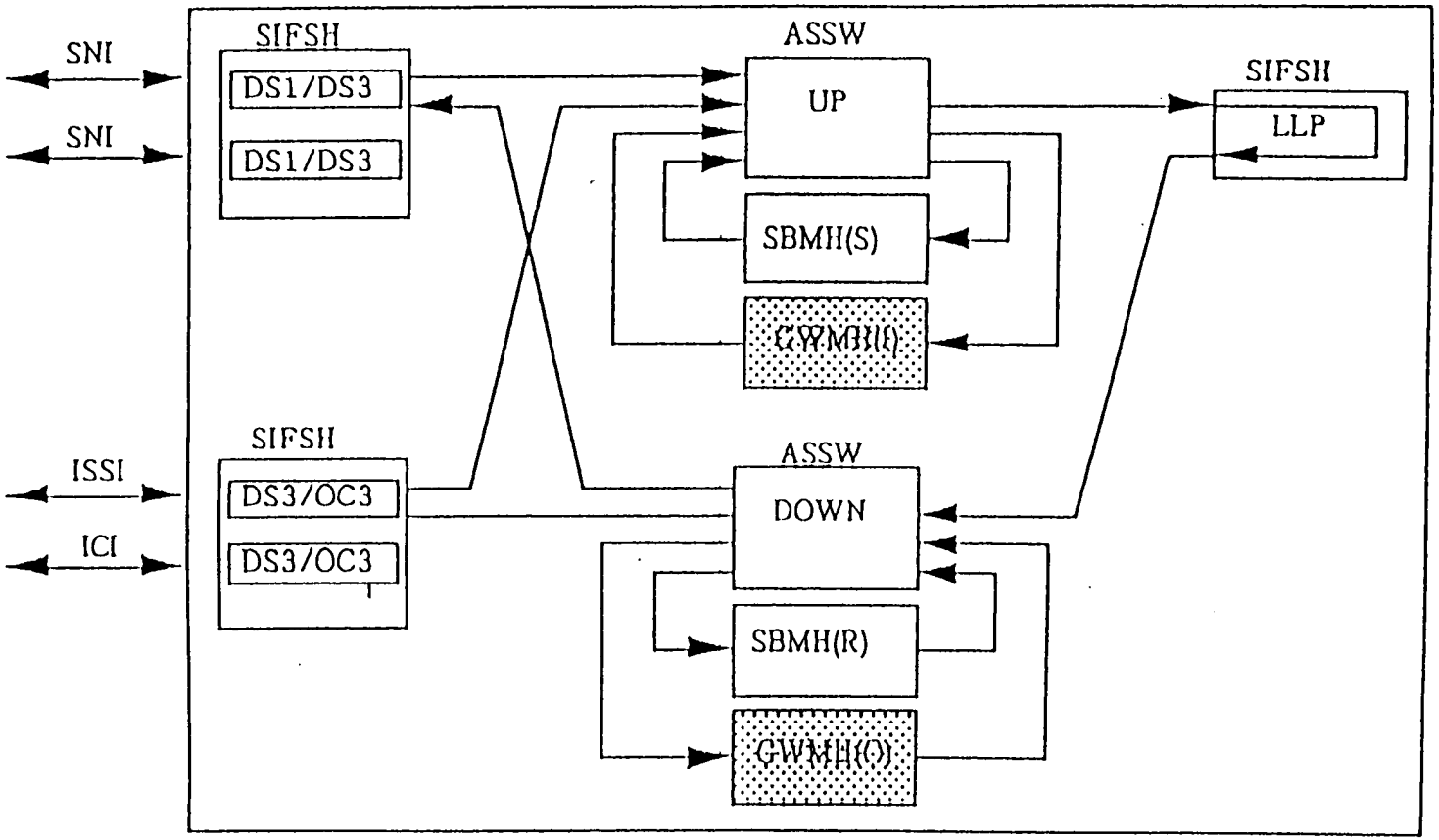

SNI
SNI
ISSI
ICI
SIFSH
DS1/DS3
DS1/DS3
SIFSH
DS3/OC3
DS3/OC3
ASSW
UP
SBMH(S)
GWMH(I)
ASSW
DOWN
SBMH(R)
GWMH(O)
SIFSH
LLP

FIG. 496

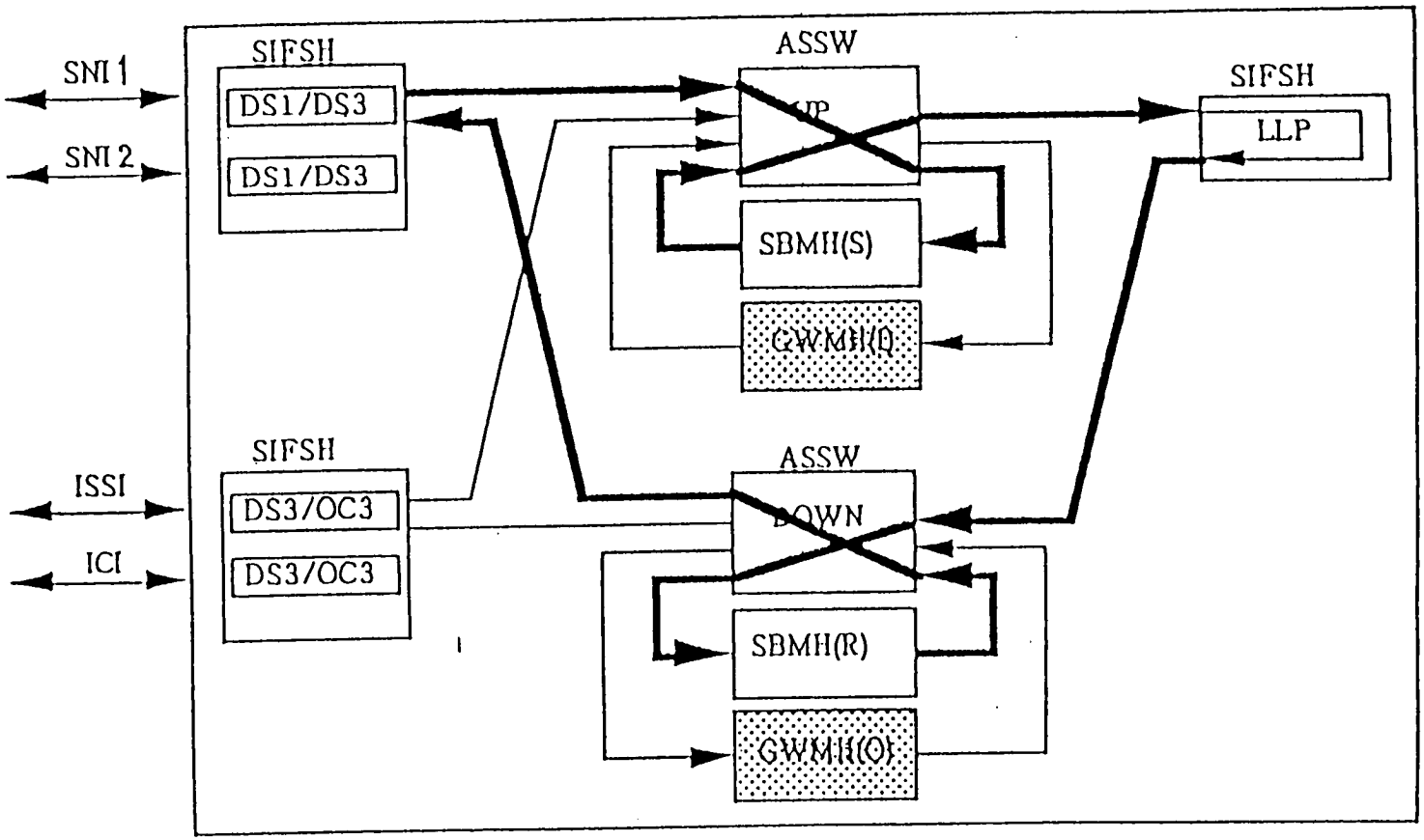

SNI 1
SNI 2
ISSI
ICI
SIFSH
DS1/DS3
DS1/DS3
SIFSH
DS3/OC3
DS3/OC3
ASSW
SBMH(S)
GWMH(I)
ASSW
SBMH(R)
GWMH(O)
SIFSH
LLP

FIG. 497

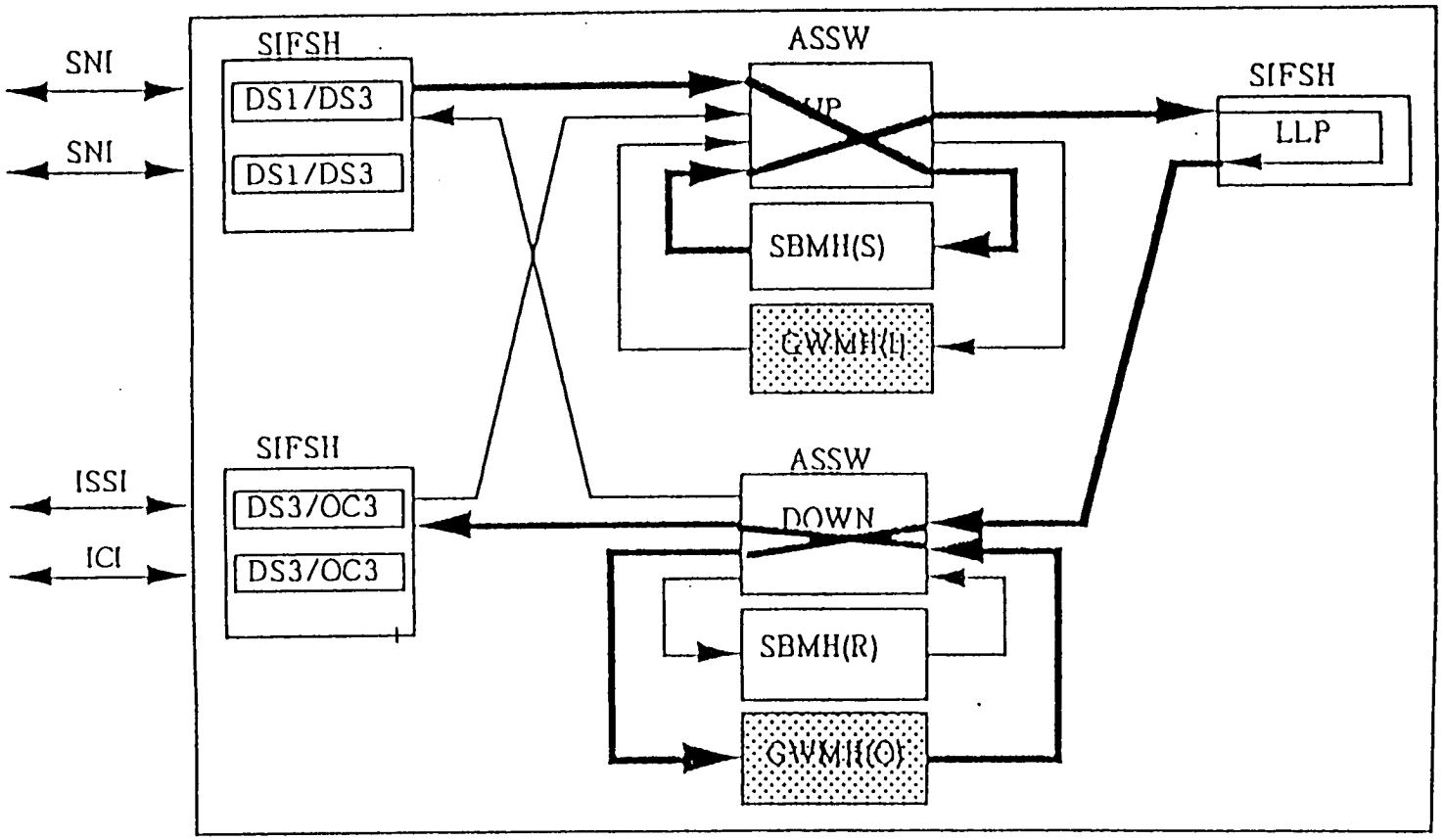

SNI
SNI
SIFSH
DS1/DS3
DS1/DS3
ASSW
UP
SBMH(S)
GWMH(U)
SIFSH
LLP
ISSI
ICI
SIFSH
DS3/OC3
DS3/OC3
ASSW
DOWN
SBMH(R)
GWMH(O)

FIG. 498

6692E0 EP2722

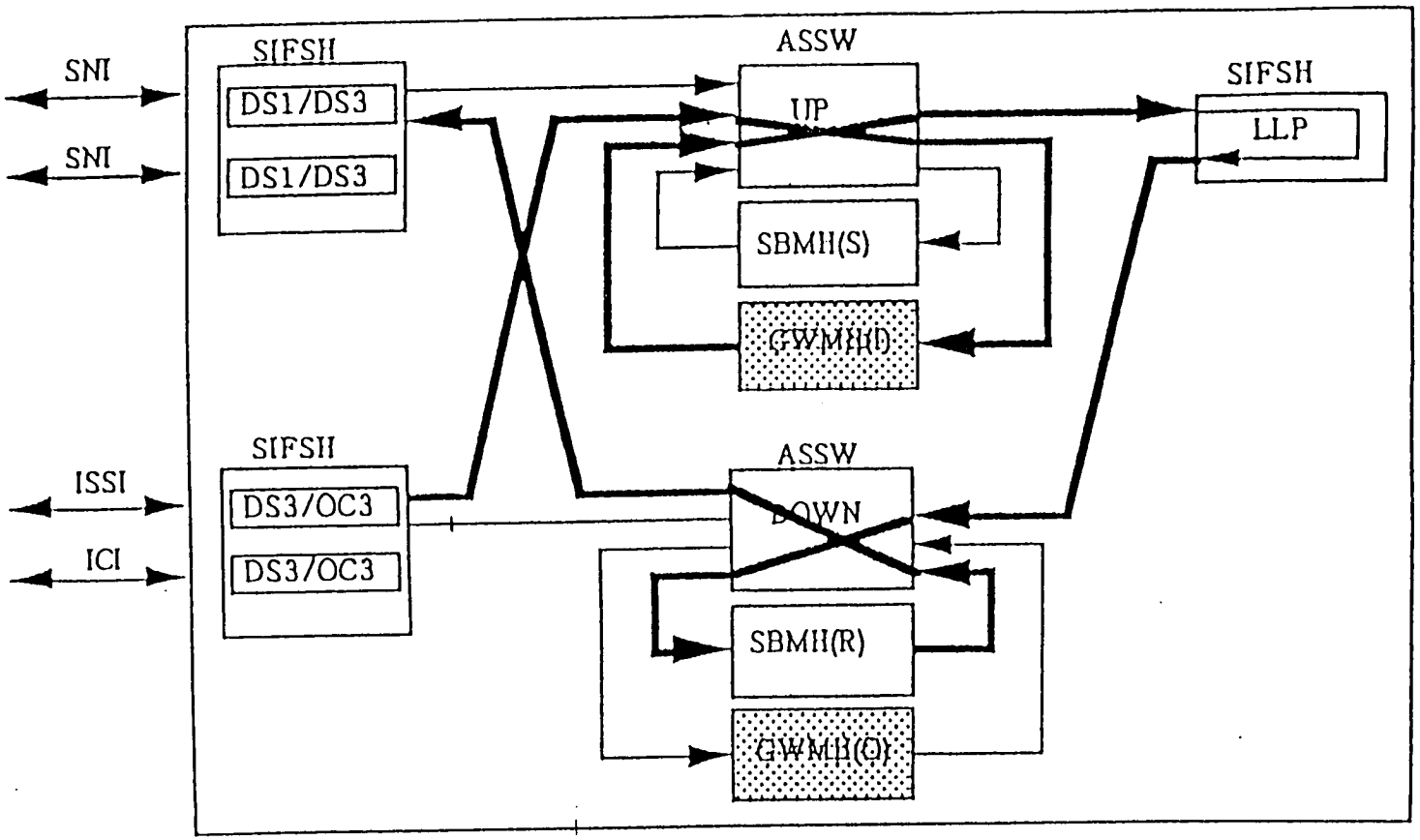


FIG. 499

69820 ET27260

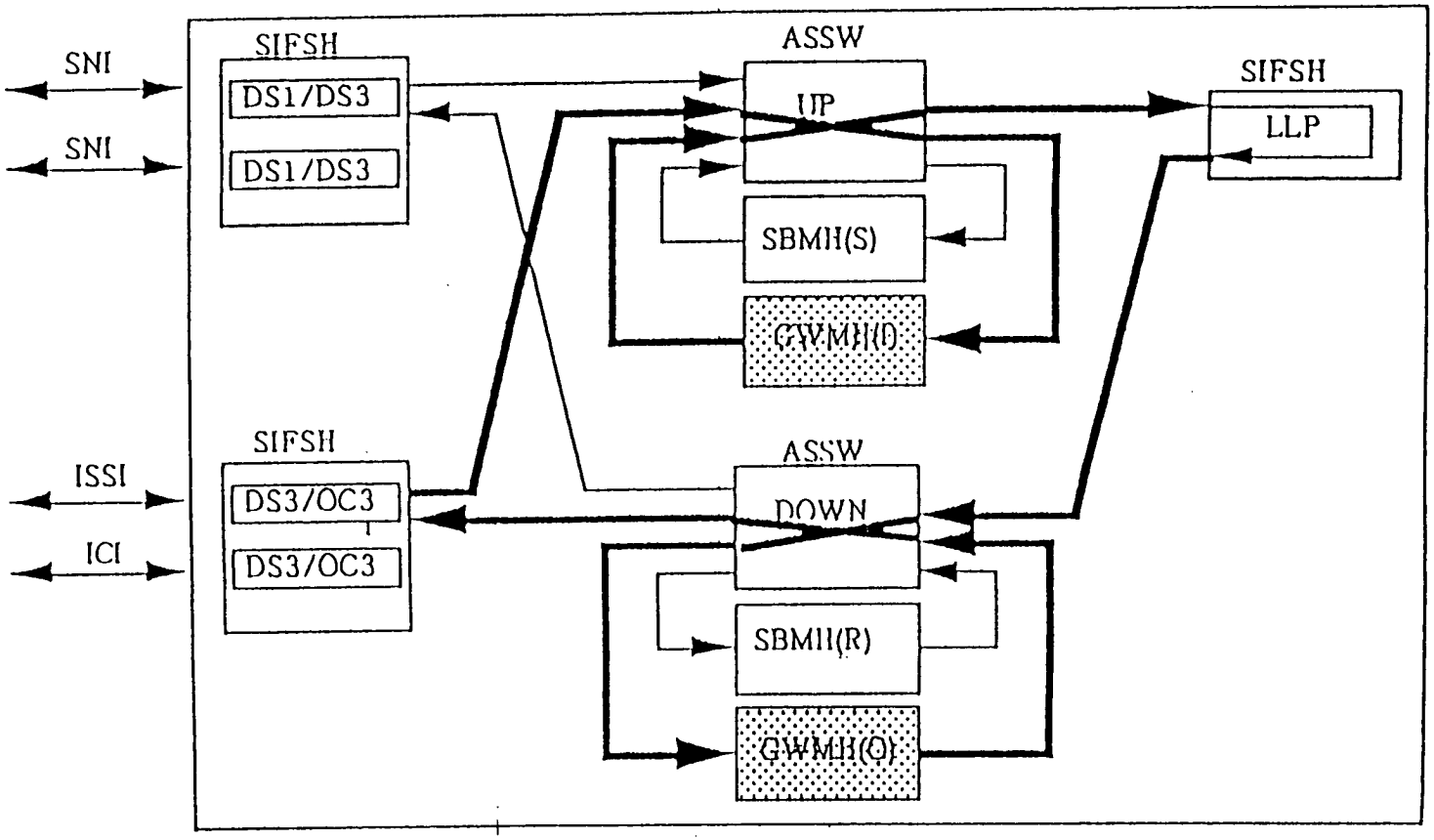


FIG. 500

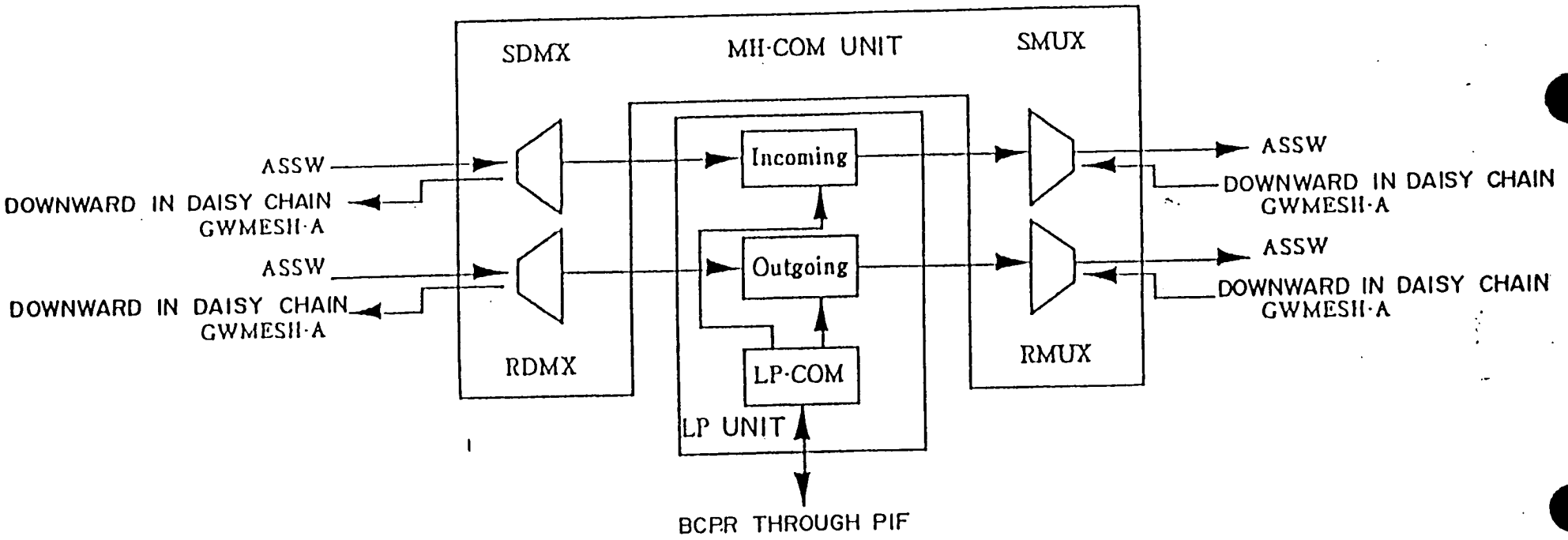

SDMX
MH-COM UNIT
SMUX
ASSW
DOWNWARD IN DAISY CHAIN
GWMESH-A
ASSW
DOWNWARD IN DAISY CHAIN
GWMESH-A
Incoming
Outgoing
LP-COM
LP UNIT
RDMX
RMUX
ASSW
DOWNWARD IN DAISY CHAIN
GWMESH-A
ASSW
DOWNWARD IN DAISY CHAIN
GWMESH-A
BCPR THROUGH PIF

FIG. 501

6692E0 EP22260

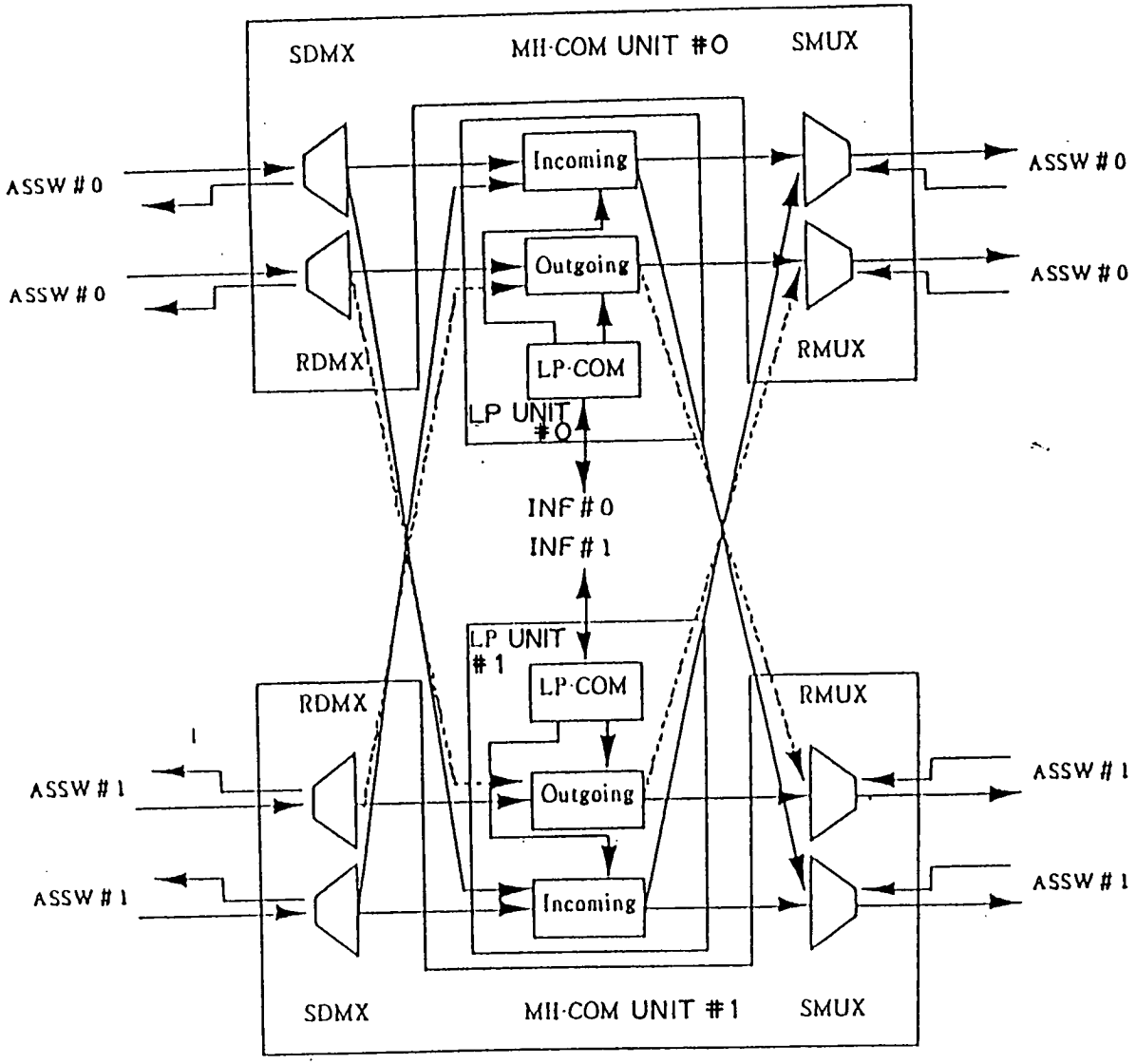


FIG. 502

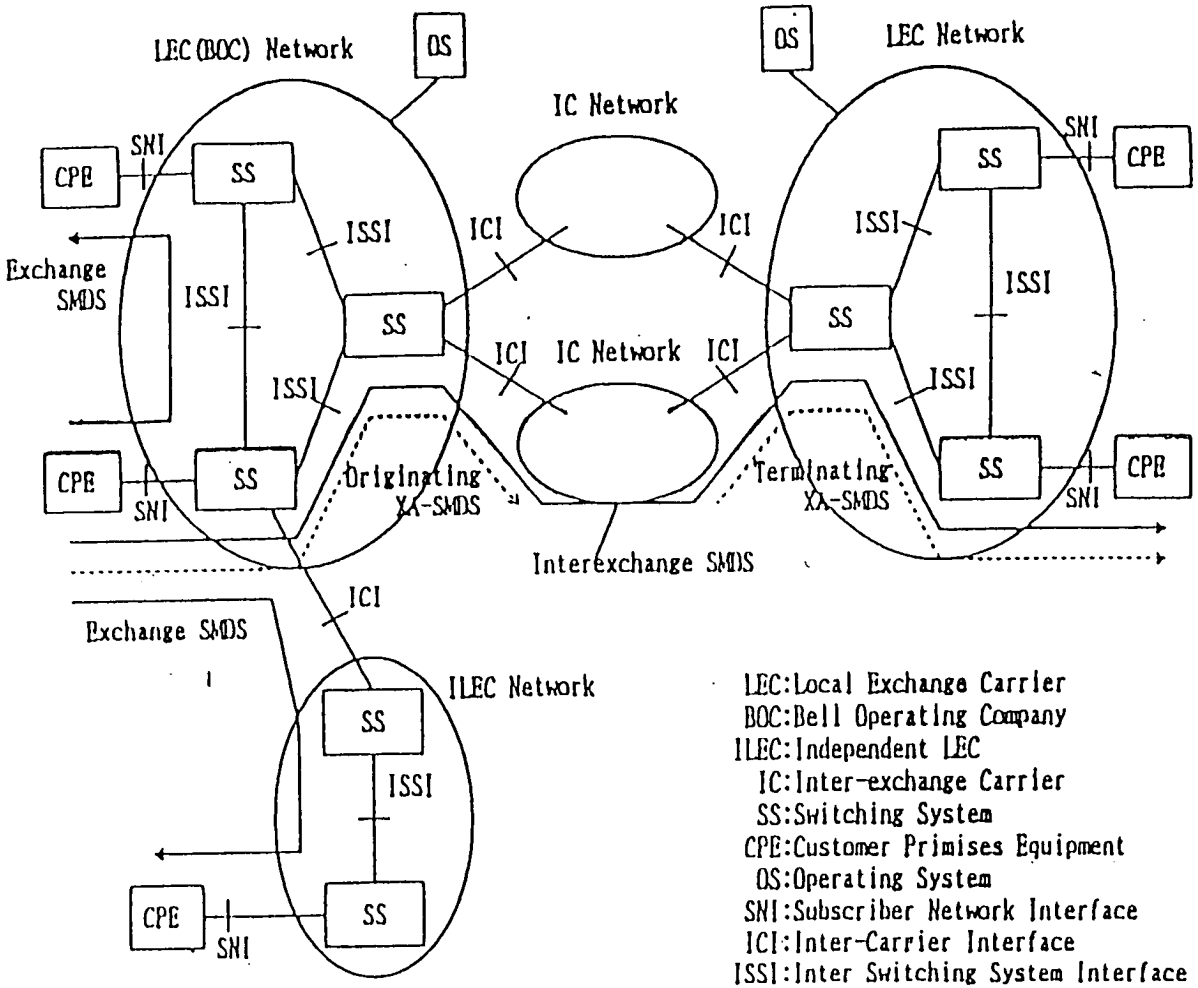
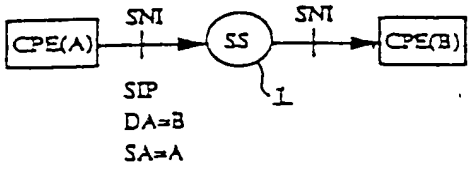

LEC(BOC) Network
OS
IC Network
OS
LEC Network
SNI
CPE
SS
ISSI
ICI
ICI
ISSI
SS
CPE
SNI
Exchange SMDS
ISSI
SS
ISSI
ICI
IC Network
ICI
ISSI
ISSI
CPE
SS
Originating XA-SMDS
Terminating XA-SMDS
SS
CPE
SNI
SNI
Interexchange SMDS
ICI
Exchange SMDS
ILEC Network
SS
ISSI
CPE
SS
SNI
LEC:Local Exchange Carrier
BOC:Bell Operating Company
ILEC:Independent LEC
IC:Inter-exchange Carrier
SS:Switching System
CPE:Customer Primises Equipment
OS:Operating System
SNI:Subscriber Network Interface
ICI:Inter-Carrier Interface
ISSI:Inter Switching System Interface

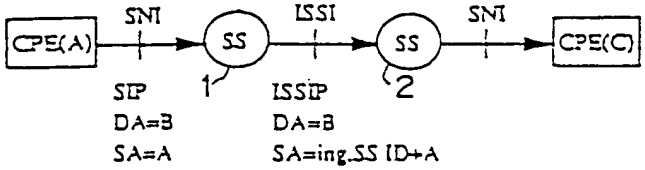
FIG. 503

Individual Address Routing (DATA IS TRANSMITTED AS BEING UNDIVIDED)

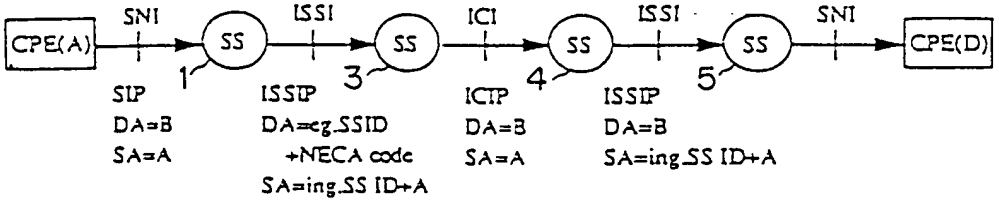
(1) COMMUNICATIONS IN SS



(2) COMMUNICATIONS IN LEC



(3) COMMUNICATIONS IN LATA EXTERNAL TO LEC



(4) COMMUNICATIONS EXTERNAL TO LATA

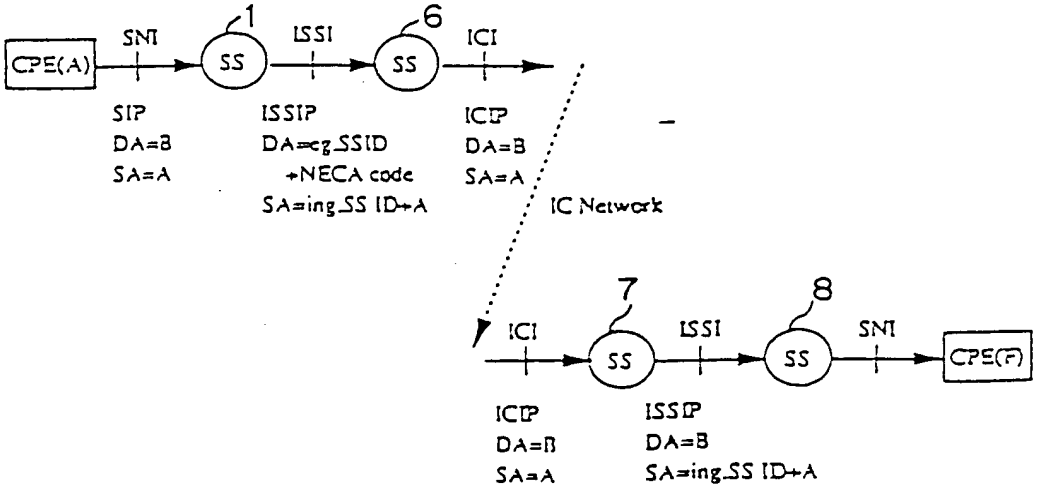


FIG. 504

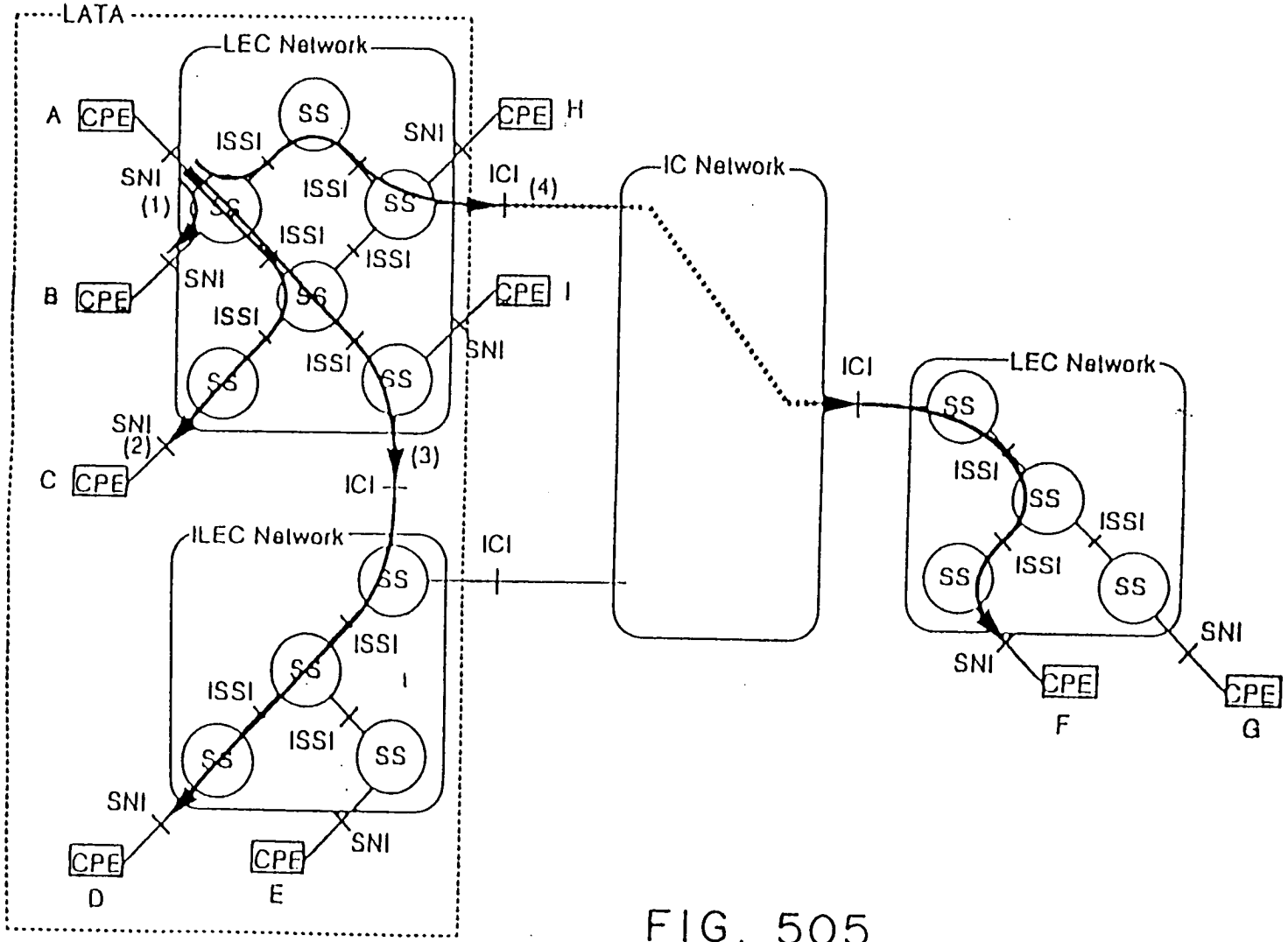
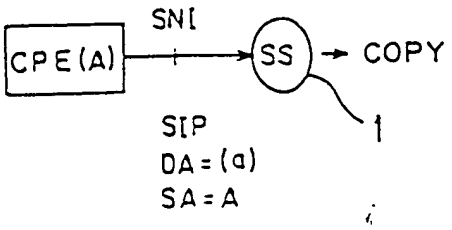
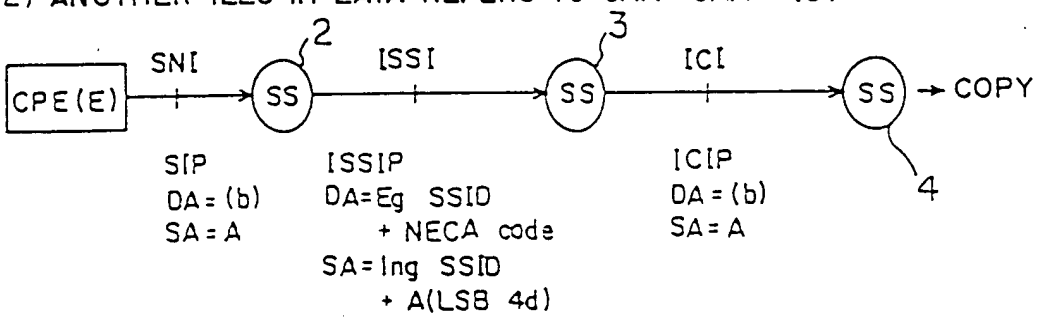

LATA
LEC Network
A
CPE
SNI
(1)
B
CPE
SNI
C
CPE
SNI
(2)
SS
ISSI
SNI
CPE
H
ICI
(4)
CPE
I
SNI
(3)
ICI
ILEC Network
ICI
SS
ISSI
J
SNI
CPE
D
CPE
E
SNI
IC Network
ICI
LEC Network
SS
ISSI
SNI
CPE
F
SNI
CPE
G

FIG. 505

(1) LEC OF HOME SYSTEM REFERS TO GAA GAA = (a)



(2) ANOTHER ILEC IN LATA REFERS TO GAA GAA = (b)



(3) GAA EXISTS IN OTHER THAN LATA GAA GAA = (c)

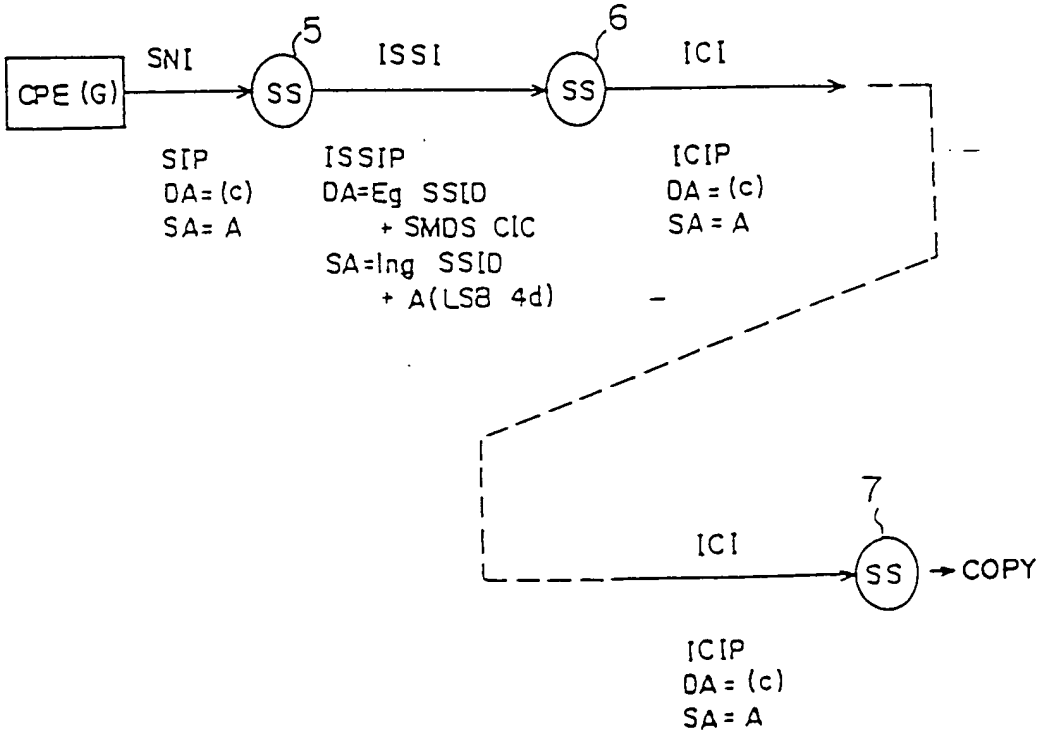


FIG. 506

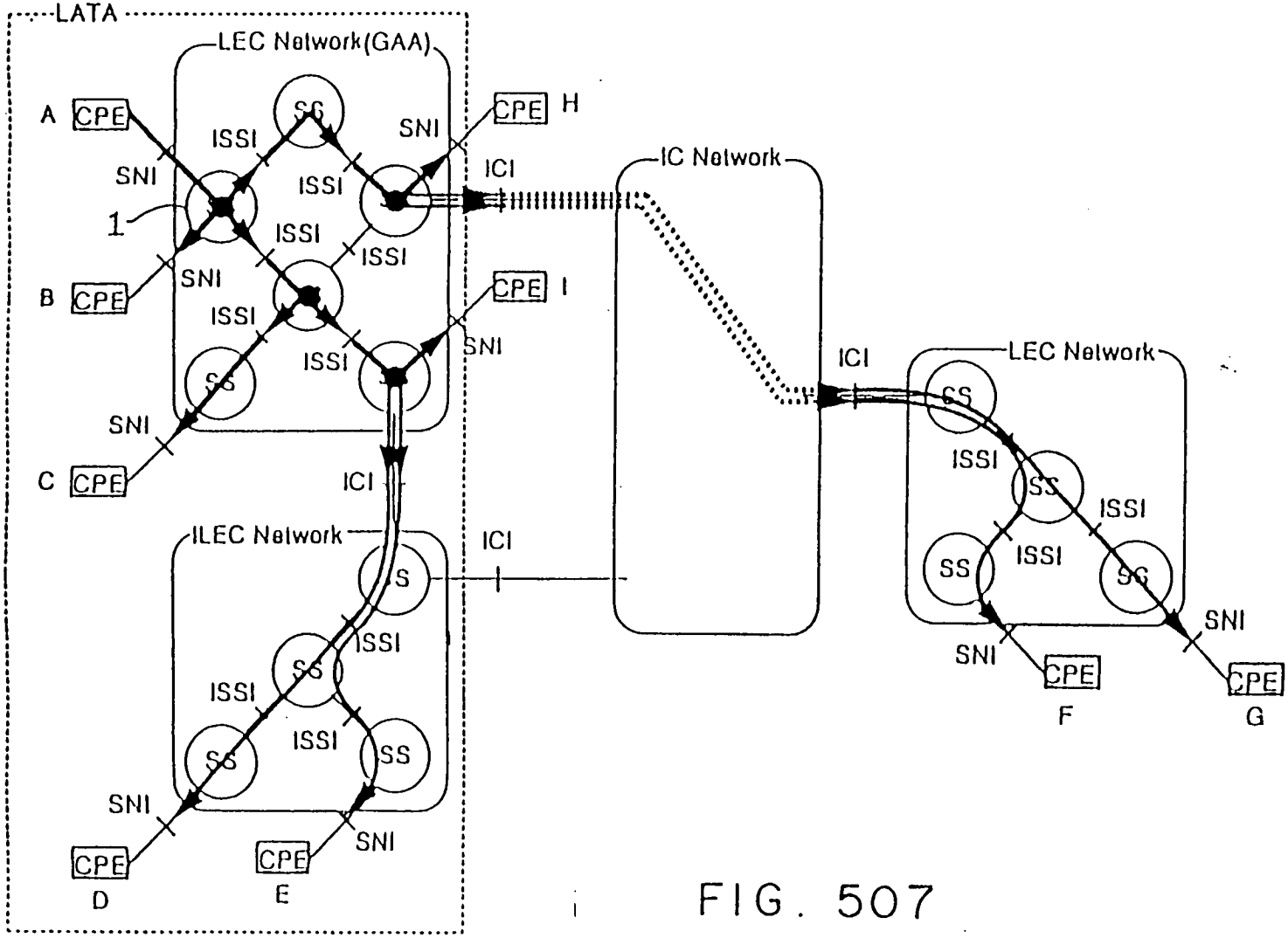

LATA
LEC Network(GAA)
A
CPE
SNI
1
B
CPE
SNI
C
CPE
SNI
ISSI
SG
SS
ICI
ILEC Network
S
D
CPE
E
CPE
H
I
IC Network
F
CPE
G
LEC Network

FIG. 507

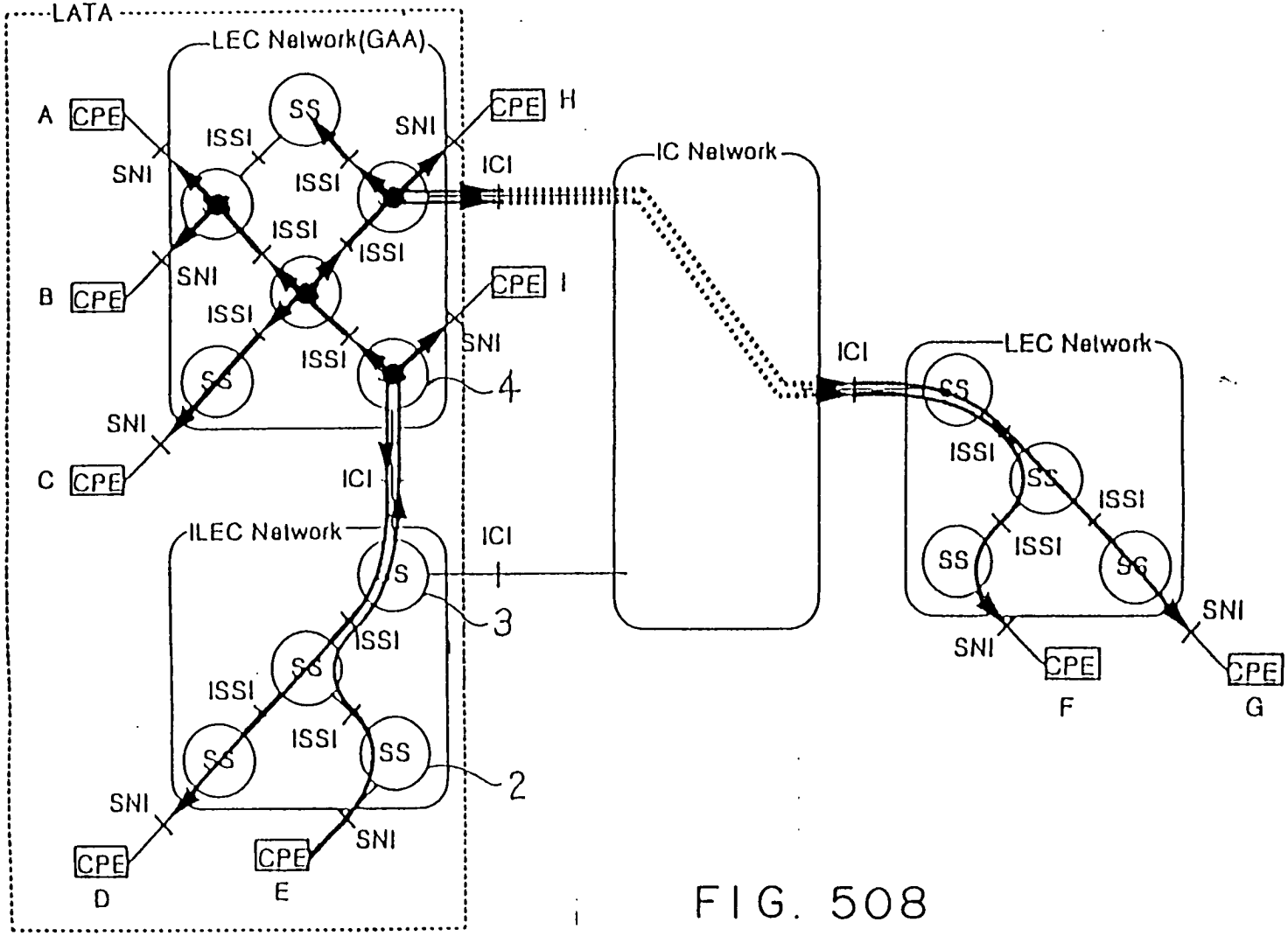

LATA
LEC Network(GAA)
A
CPE
SNI
B
CPE
SNI
C
CPE
SNI
SS
ISSI
SS
ISSI
SS
ISSI
SS
ISSI
SS
ISSI
SS
ISSI
SS
ISSI
SS
SNI
CPE
H
CPE
I
SNI
4
ICI
ILEC Network
ICI
S
3
SS
ISSI
SS
ISSI
SS
2
SNI
CPE
D
CPE
E
SNI
ICI
IC Network
ICI
LEC Network
SS
ISSI
SS
ISSI
SS
ISSI
SS
SNI
CPE
F
SNI
CPE
G

FIG. 508

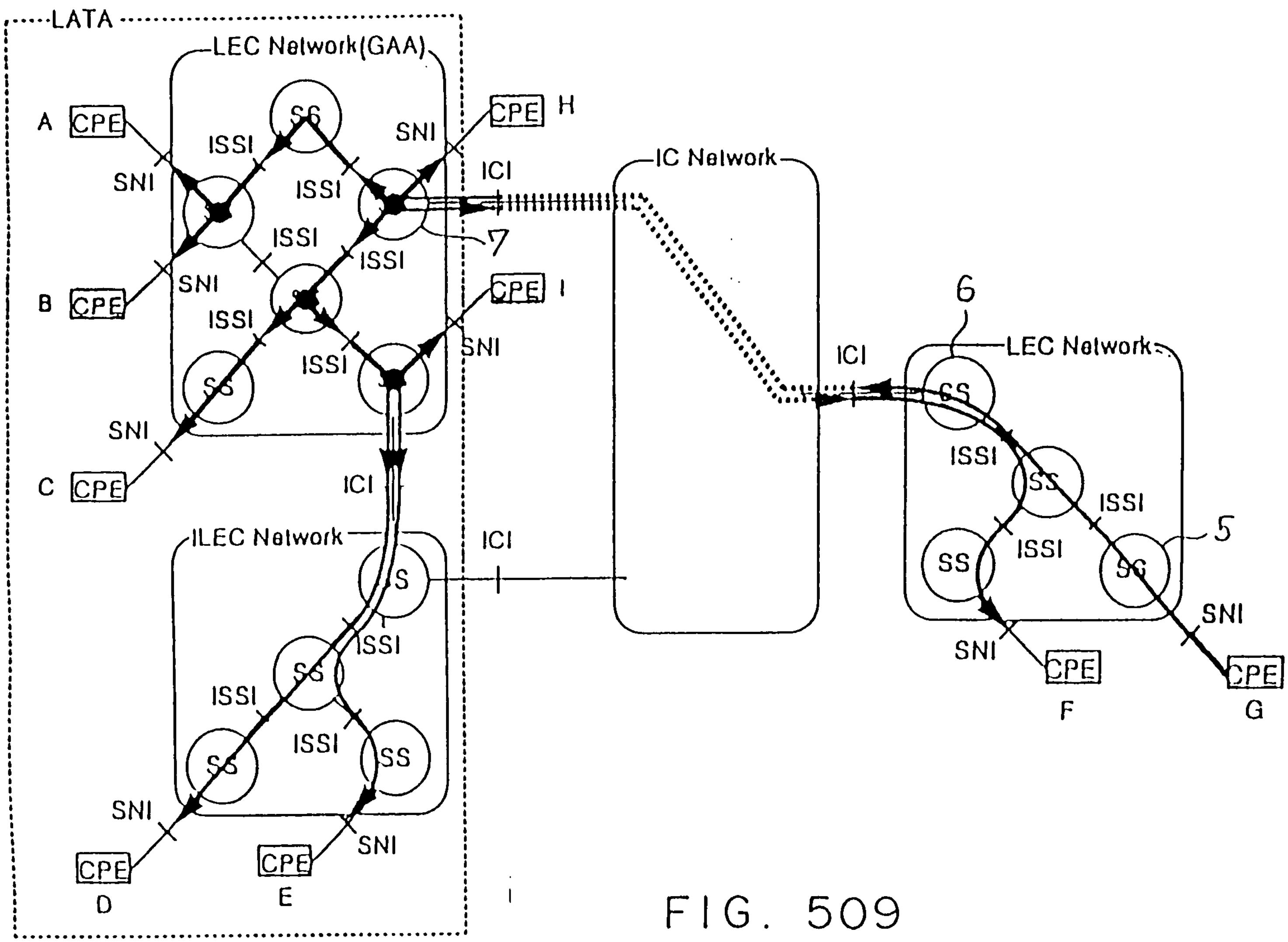

LATA
LEC Network(GAA)
A
B
C
CPE
CPE
CPE
SNI
SNI
SNI
SS
SS
ISSI
ISSI
ISSI
ISSI
ISSI
ISSI
SNI
SNI
CPE
H
CPE
I
ICI
7
ICI
ILEC Network
S
ISSI
SS
ISSI
ISSI
SS
SS
SNI
SNI
CPE
D
CPE
E
ICI
IC Network
ICI
6
LEC Network
SS
ISSI
SS
ISSI
SS
ISSI
SG
5
SNI
SNI
CPE
F
CPE
G

FIG. 509

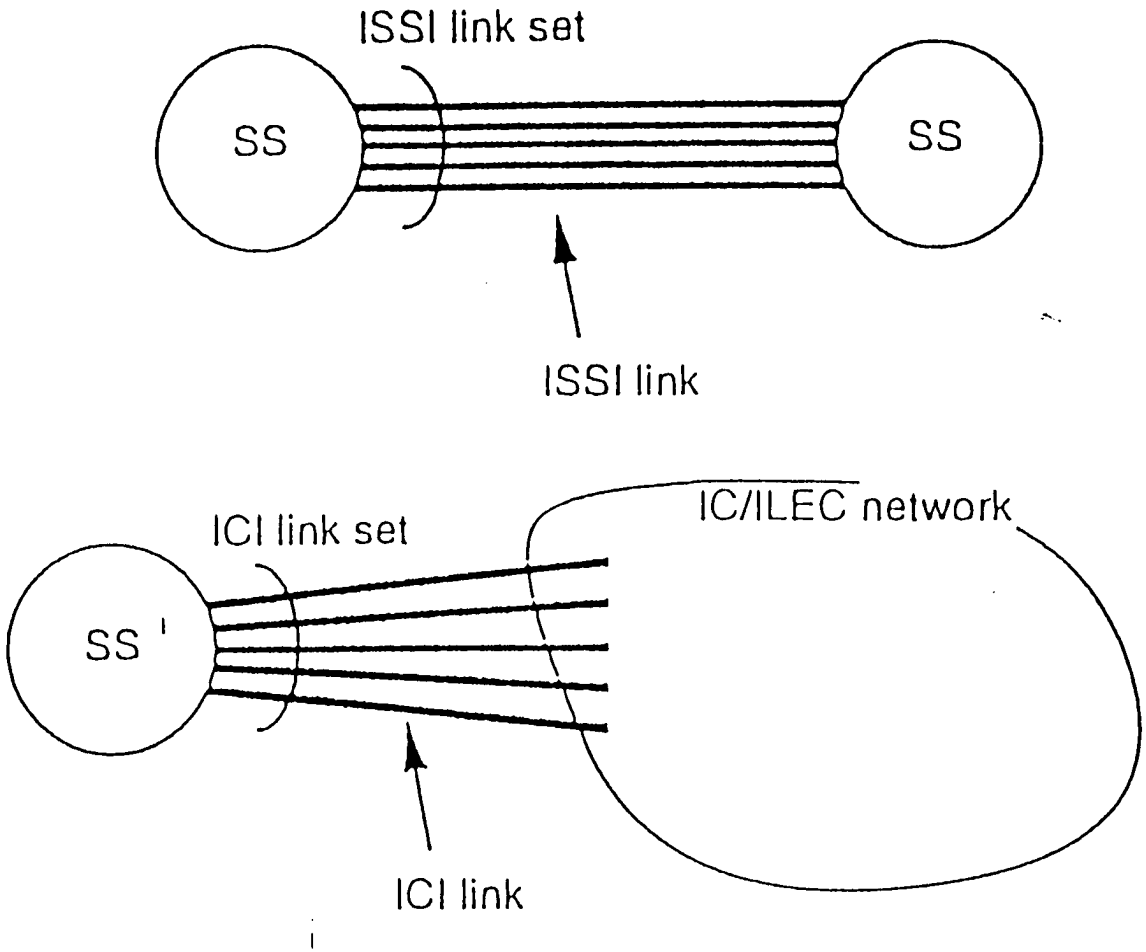

ISSI link set
SS
SS
ISSI link
ICI link set
IC/ILEC network
SS '
ICI link

FIG. 510

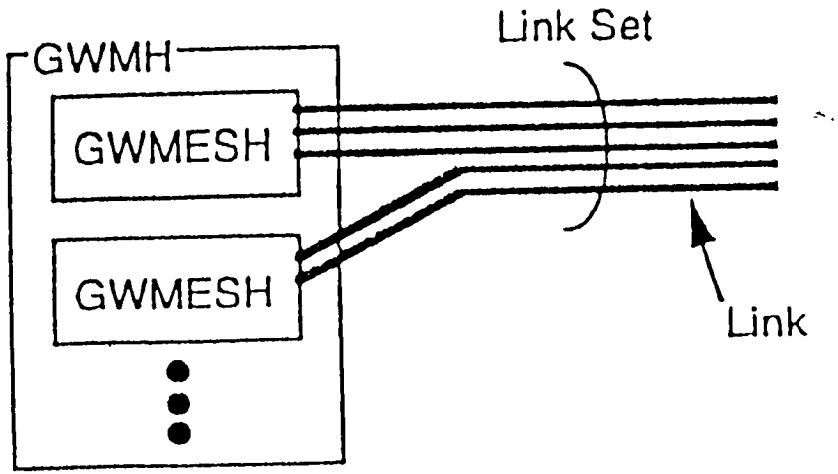


FIG. 511

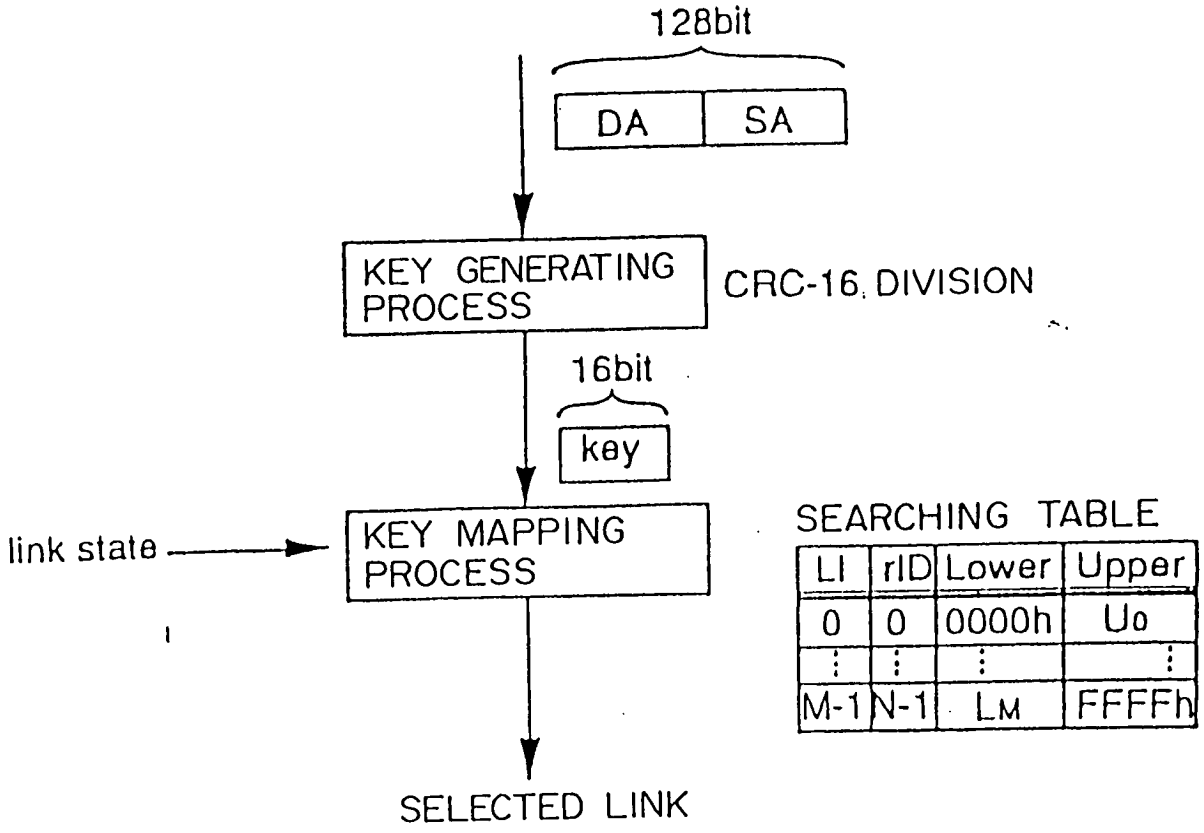
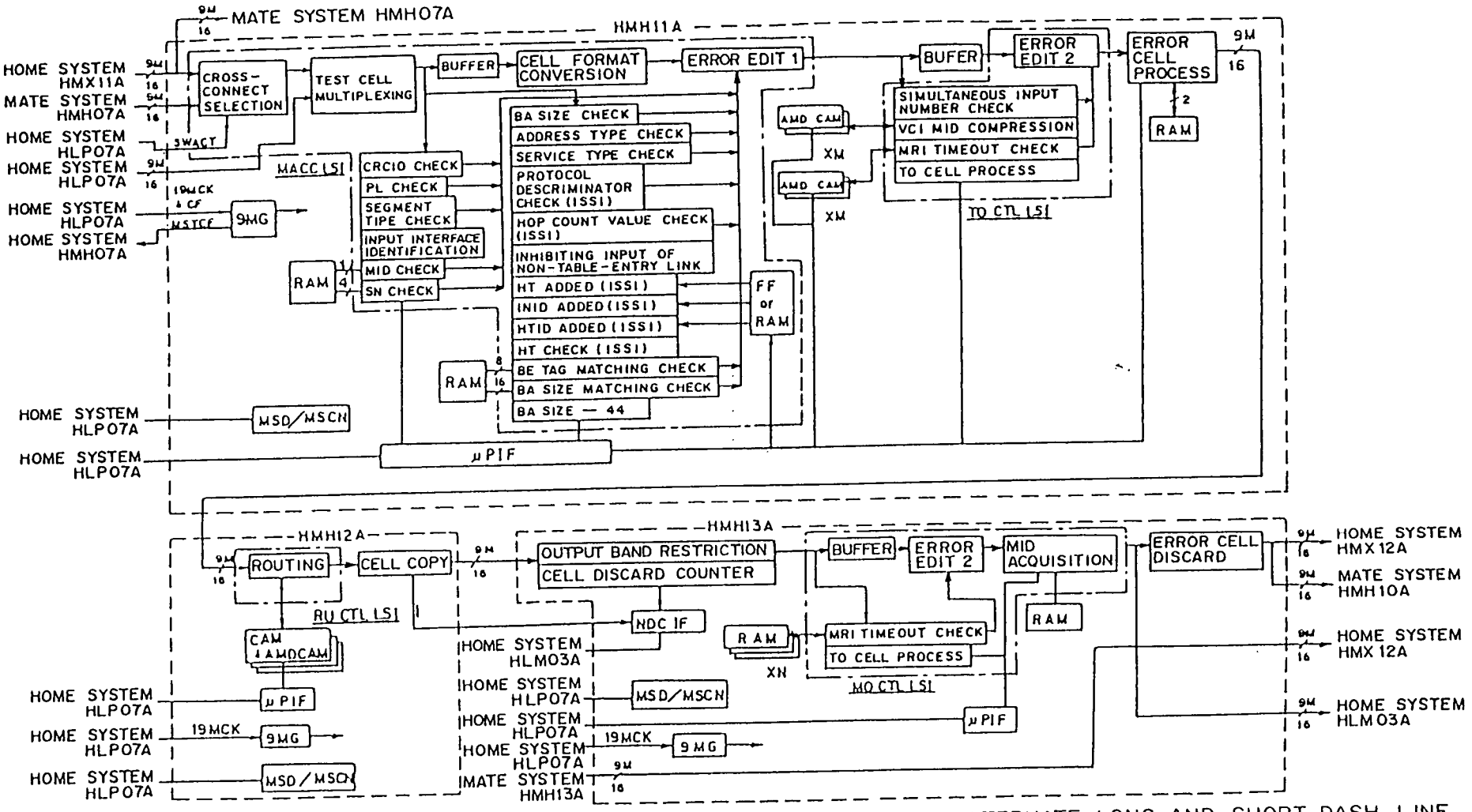

128bit
DA
SA
KEY GENERATING PROCESS
CRC-16 DIVISION
16bit
key
link state
KEY MAPPING PROCESS
SELECTED LINK
SEARCHING TABLE
LI
rID
Lower
Upper
0
0
0000h
U0
M-1
N-1
LM
FFFFh

FIG. 512

6,952,820 B2



NOTE : ALTERNATE LONG AND SHORT DASH LINE INDICATES PORTION TO BE PROCESSED INTO LSI.

FIG. 513

ITEM	BLOCK NAME	CONTENTS
1	CROSS-CONNECT SELECTION	MOX ACT SYSTEM DATA IS SELECTED ACCORDING TO SYSTEM INFORMATION OF SWITCH. TOC CELL (TEST CELL) IS DROPPED.
2	INPUT INTERFACE IDENTIFICATION	INPUT INTERFACE IS IDENTIFIED AS ISSI OR ICI.
3	TEST CELL MULTIPLEXING	TEST CELL IS MULTIPLEXED WHEN LINE IS IN IDLE CELL STATE. TEST CELL IS TRANSMITTED DURING DIAGNOSIS
4	CRC CHECK	CRC OPERATION IS PERFORMED ON CELL PAYLOAD AND CHECK IS MADE FOR ERROR.
5	PL CHECK	CHECK IS MADE THAT PAYLOAD LENGTH INDICATES PREDETERMINED VALUE.
6	SEGMENT TYPE CHECK	CHEK IS MADE WHETHER SEGMENT TYPE IS BOM, COM, EOM, OR SSM.
7	MID CHECK	CHECK IS MADE THAT VCI/MID IS NOT ACTIVE AT BOM AND VCI/MID IS ACTIVE AT COM AND EOM
8	SN CHECK	CHECK IS MADE THAT SN IS INITIALIZED AT BOM AND SN IS IN ORDER AT COM AND EOM.
9	BA SIZE CHECK	CHECK IS MADE THAT BASIZE INDICATES PREDETERMINED VALUE (40-9280).
10	AT CHECK	CHECK IS MADE THAT ADDRESS TYPE IN DA AND SA FORMAT INDICATES PREDETERMINED VALUE.
11	SERVICE TYPE CHECK	CHECK IS MADE THAT SERVICE TYPE INDICATES PREDETERMINED VALUE(NO ERROR FLAG IS SET)
12	PD CHECK	CHECK IS MADE THAT PROTOCOL DISCRIMINATOR INDICATES PREDETERMINED VALUE.
13	HOP COUNT CHECK	CHECK IS MADE THAT HOP COUNT FIELD VALUE DOES NOT INDICATE 0
14	IIT CHECK	CHECK IS MADE THAT INGRESS INTERFACE TYPE INDICATES PREDETERMINED VALUE.
15	BE TAG MATCHING CHECK	CHECK IS MADE THAT BE TAG OF L3 HEADER MATCHES BE TAG OF TAILER.
16	BA SIZE MATCHING CHECK	CHECK IS MADE THAT BE SIZE OF L3 HEADER MATCHES LENGTH OF TAILER.
17	ERROR EDIT I	ERROR CHECKED BY EACH CHECKER IS POSITIONED IN ERROR FLAG.
18	MRI TIMEOUT CHECK	MRI TIMEOUT IS DETERMINED IN L3POU UNIT.
19	ERROR EDIT II	ERROR CHECKED BY EACH CHECKER IS POSITIONED IN ERROR FLAG.
20	TO CELL PROCESS	WHEN TIMEOUT IS REACHED IN MRI TIMEOUT CHECK, TIMEOUT CELL IS TRANSMITTED WHEN CELL IS INVALID.
21	CELL FORMAT CONVERSION	FORMAT OF ICIP/ISSIP IS CONVERTED INTO INTER-MH INTERFACE FORMAT (INCLUDING INPUT INF ICI/ISSI DISCRIMINATION INFORMATION).
22	ERROR CELL PROCESS	IF L3POU IS DETERMINED TO BE ERRONEOUS AS RESULT OF EACH CHECK, IT IS SUSPENDED.
23	ROUTING	DA AND CARRIER FIELD VALUE ARE IDENTIFIED AND MESSAGE ROUTING TABLE IS REFERRED TO IN ORDER TO SPECIFY MH (SBMH AND GWMH) CONTAINING DESTINATION SNI, ISSI, AND ICI.
24	CELL COPY	WHEN THERE ARE PLURAL DESTINATION MHs AS RESULT OF ROUTING, CELLS ARE COPIED WITH VCI ASSIGNED TO EACH MH.
25	CELL DISCARD COUNTER	CELL (L2 OR L3?) IS COUNTED IF IT IS DISCARDED BECAUSE OF INSUFFICIENT CAPACITY OF CELL COPY BUFFER.
26	OUTPUT BAND RESTRICTION	OUTPUT BAND (PEAK RATE) IS LIMITED FOR EACH OUTPUT MH.
27	CELL DISCARD	CELL IS DISCARDED WHEN OUTPUT BAND LIMIT IS EXCEEDED.
28	DISCARD COUNTER	NUMBER OF L2 AND L3 MESSAGES DISCARDED BY OUTPUT BAND LIMIT IS COUNTED.
29	MRI TIMEOUT CHECK	MRI TIMEOUT IS DETERMINED IN L3 POU UNITS.
30	ERROR EDIT	ERROR CHECKED BY MRI TIMEOUT IS POSITIONED IN ERROR FLAG.
31	TO CELL PROCESS	WHEN TIMEOUT IS REACHED IN MRI TIMEOUT CHECK, TIMEOUT CELL IS TRANSMITTED WHEN CELL IS INVALID.
32	MID ACQUISITION	OUTPUT MID IS ASSIGNED IN OUTPUT MH UNITS.
33	ERROR CELL DISCARD	IF CELL IS DETERMINED TO BE ERRONEOUS AS RESULT OF EACH CHECK, IT IS DISCARDED.
34	μP INTERFACE	LP COM IS INTERFACED WITH μP (SCMT).
35	MSD/MSCN INTERFACE	LP COM IS INTERFACED WITH MSD/MSCN.
36	NOC INTERFACE	LP COM IS INTERFACED WITH μP IN RELATION TO NETWORK DATA COLLECTION (NOC).

FIG. 514

	Error Flag / Message	E1 MS	E1 RM	E2 MT	E2 CC	E2 PL	E2 EN	E1 MC	E2 MA	E2 SN	E2 BA	E2 DT	E2 ST	E2 PI	E2 PD	E2 HC	E2 H	E2 EM	E2 BE	E2 LE	PVC
A	Invalid Payload CRC Code	ON	ON		ON																M
B	Payload Length Error	ON	ON			ON															M
C	Encapsulation Error (Segment Type = SSM)	ON	ON				ON														M
D	BOM with Unexpected MID		OK						ON												M
	COM with Unexpected MID	ON	OK					ON													M
	EOM with Unexpected MID	ON	OK						ON												M
E	Unexpected SN Error	ON	OK					OK	OK	ON											M
F	Invalid BAsize Field Value	ON									ON										M
	Invalid DA Type	ON										ON									M
	Invalid SA Type	ON											ON								M
	Invalid Protocol ID (ICIP) & Invalid Service Type (ISSIP)	ON												ON							M
	Invalid Protocol Descriminator (ISSIP)	ON													ON						M
	Hop Count = 0 (ISSIP)	ON														ON					M
	Invalid Ingress Interface Type (ISSIP)	ON															ON				M
G	BEtag Mismatch	ON	OK																ON		M
	BAsize ≠ Length	ON	OK																OK	ON	M

'ON': EF INDICATING "ON" WHEN CHECK RESULT OUTPUTS NG
'OK': CHECK IS MADE ONLY WHEN OK-MARKED EF INDICATES "OK".
'NO MARK': CHECK IS MADE REGARDLESS OF OK OR NG OF 'NO MARK' EF.
'M': NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 515

	Error Flag / Message	E1 MS	E1 RM	E2 MT	E2 CC	E2 PL	E2 EN	E1 MC	E2 MA	E2 SN	E2 BA	E2 DT	E2 ST	E2 PI	E2 PD	E2 HC	E2 II	E2 EM	E2 BE	E2 LE	PVC
H	SIMULTANEOUS INPUT NUMBER CHECK 1	ON OK	OK															ON			M
	MRI Time Out 1	ON		ON																	M
J	ROUTING	OK	OK																		
	CELL COPY	OK	OK																		
	OUTPUT BAND LIMIT	OK	OK																		
K	SIMULTANEOUS IMPUT NUMBER CHECK 2	ON OK	OK															ON			
	MRI Time Out 2	ON		ON																	
	MID ACQUISITION	OK	OK																		
	DISCARDING ERROR CELL!	NG																			

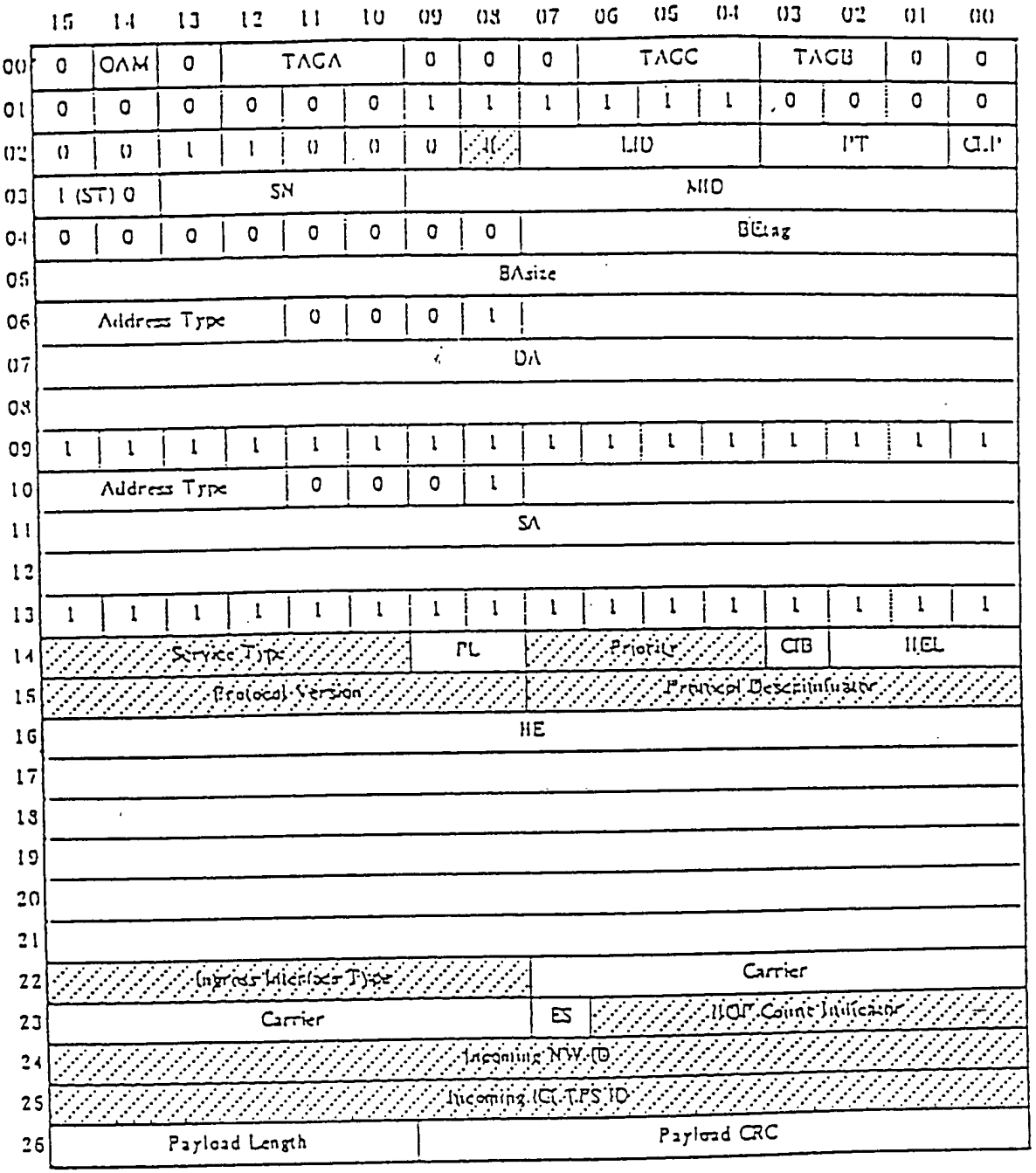
'ON': EF INDICATING "ON" WHEN CHECK RESULT OUTPUTS NG

'OK': CHECK IS MADE ONLY WHEN OK-MARKED EF INDICATES "OK".

'NO MARK': CHECK IS MADE REGARDLESS OF OK OR NG OF 'NO MARK'EF.

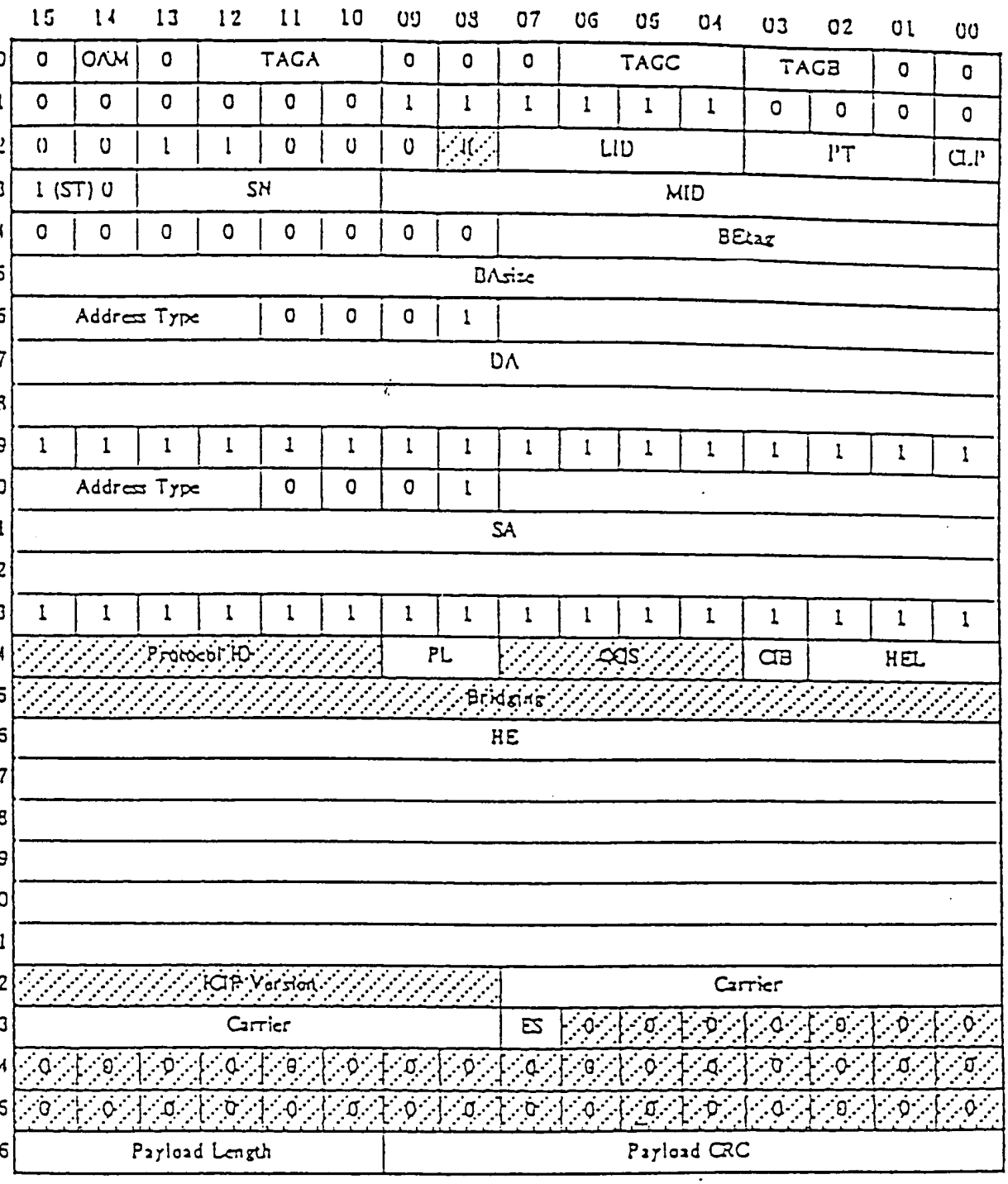
'M': NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 516



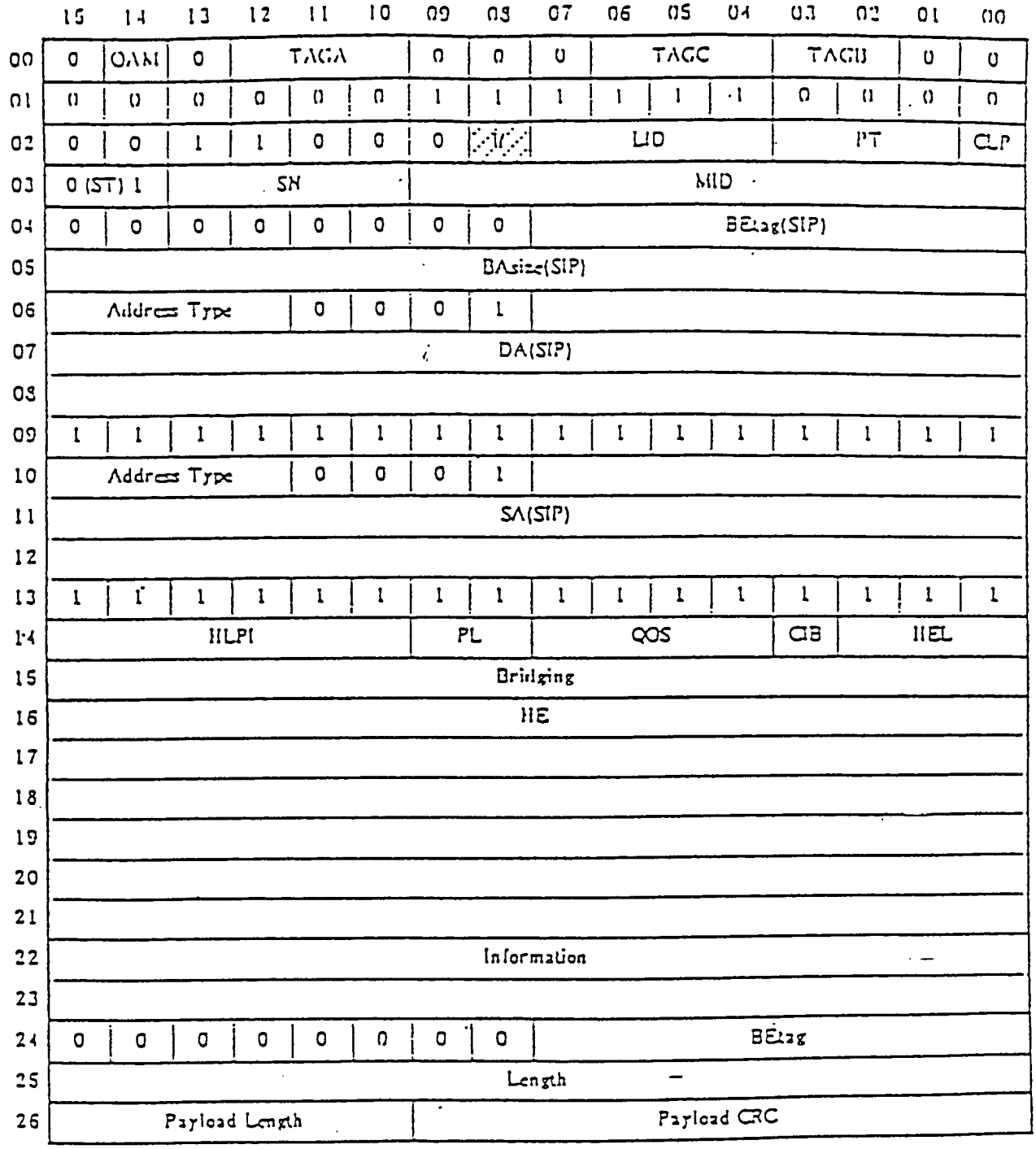
TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
IF: INTERFACE IDENTIFICATION (0=ISSI, 1=ICI)
LID: INPUT LINK NUMBER (0-7)

FIG. 517



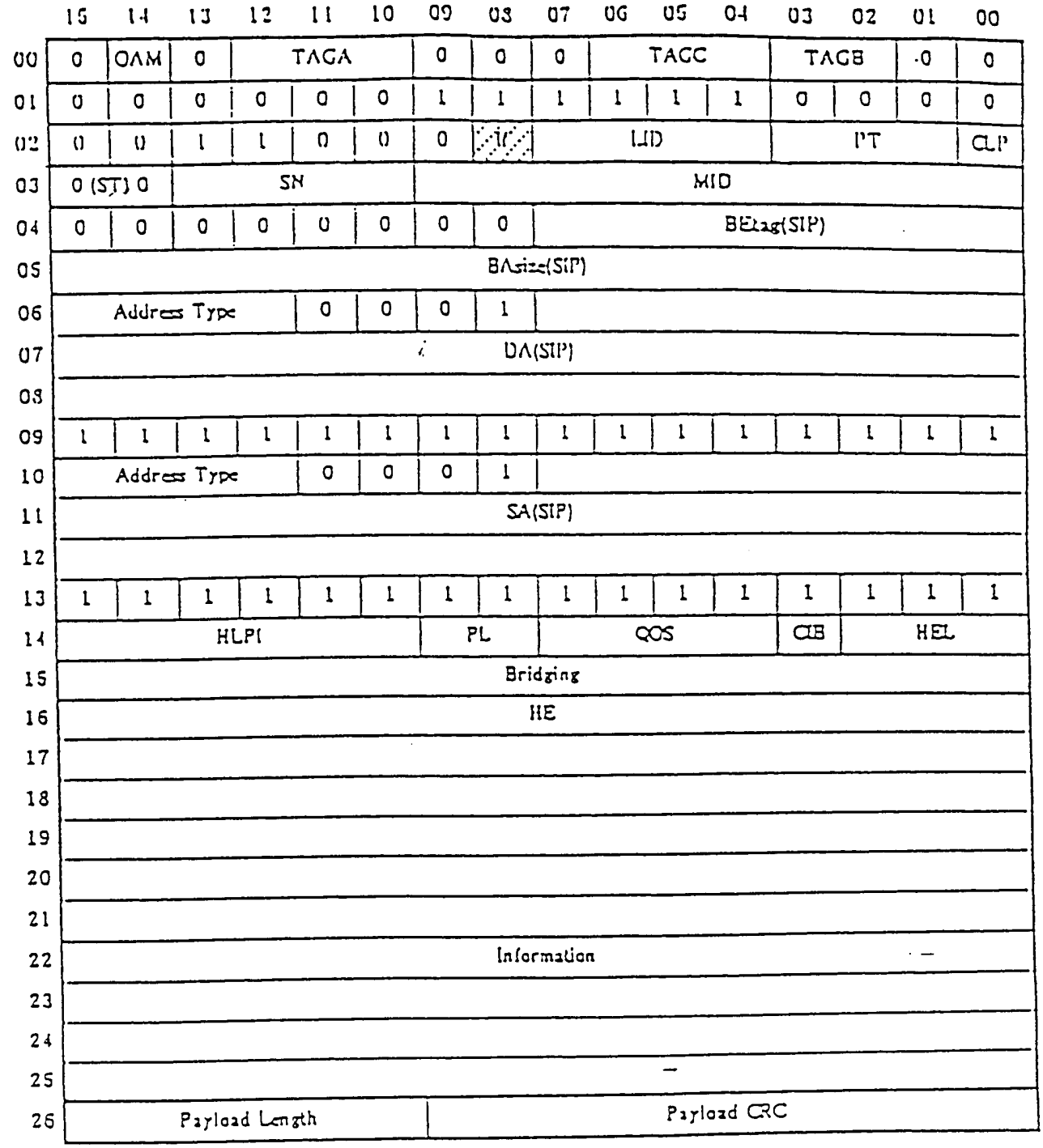
TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)
LID:INPUT LINK NUMBER(0-7)

FIG. 518



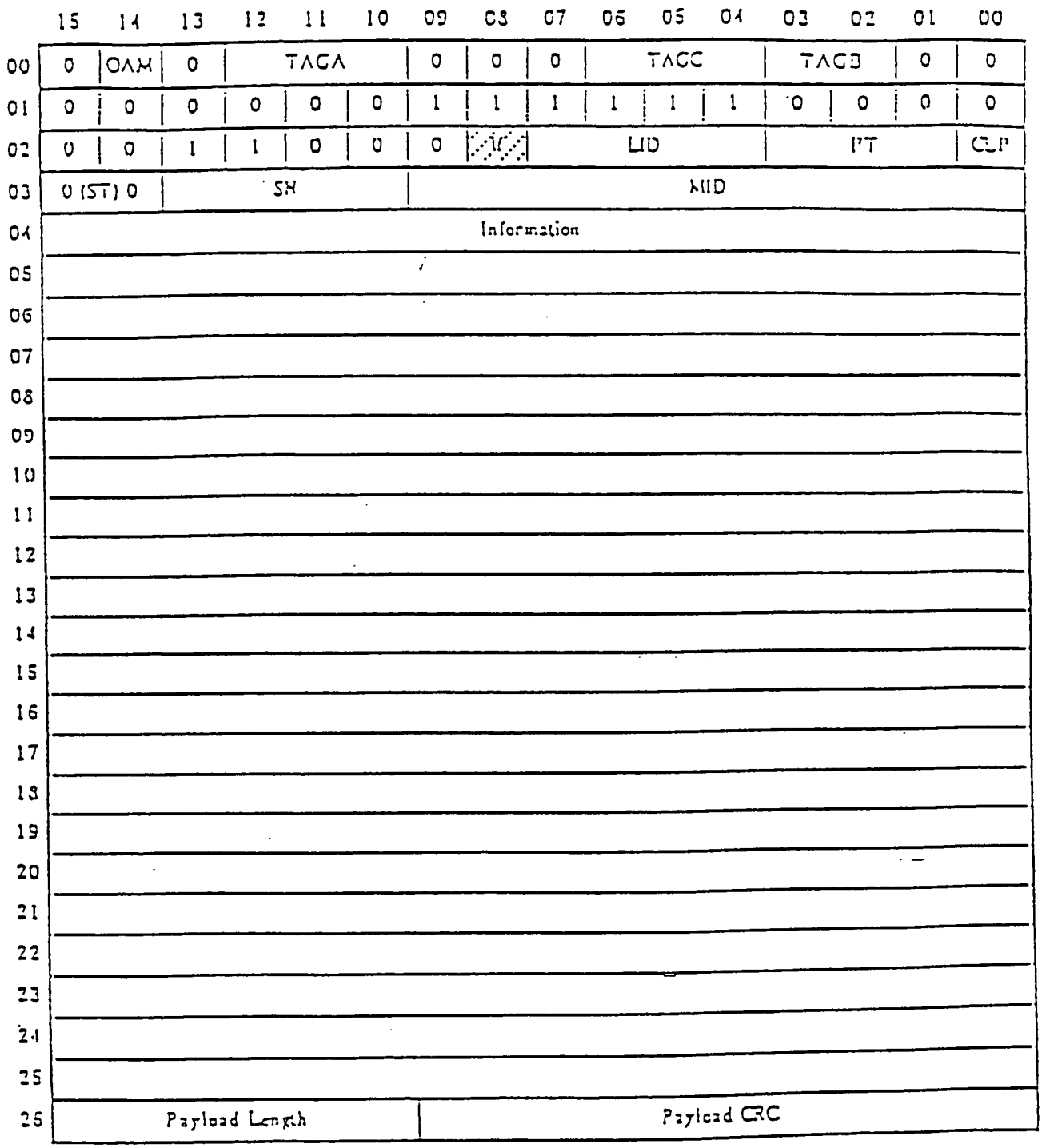
TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
IF:INTERFACE IDENTIFICATION(0=ISSI, 1=ICI)
LID:INPUT LINK NUMBER(0-7)

FIG. 519



TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)
LID:INPUT LINK NUMBER(0-7)

FIG. 520



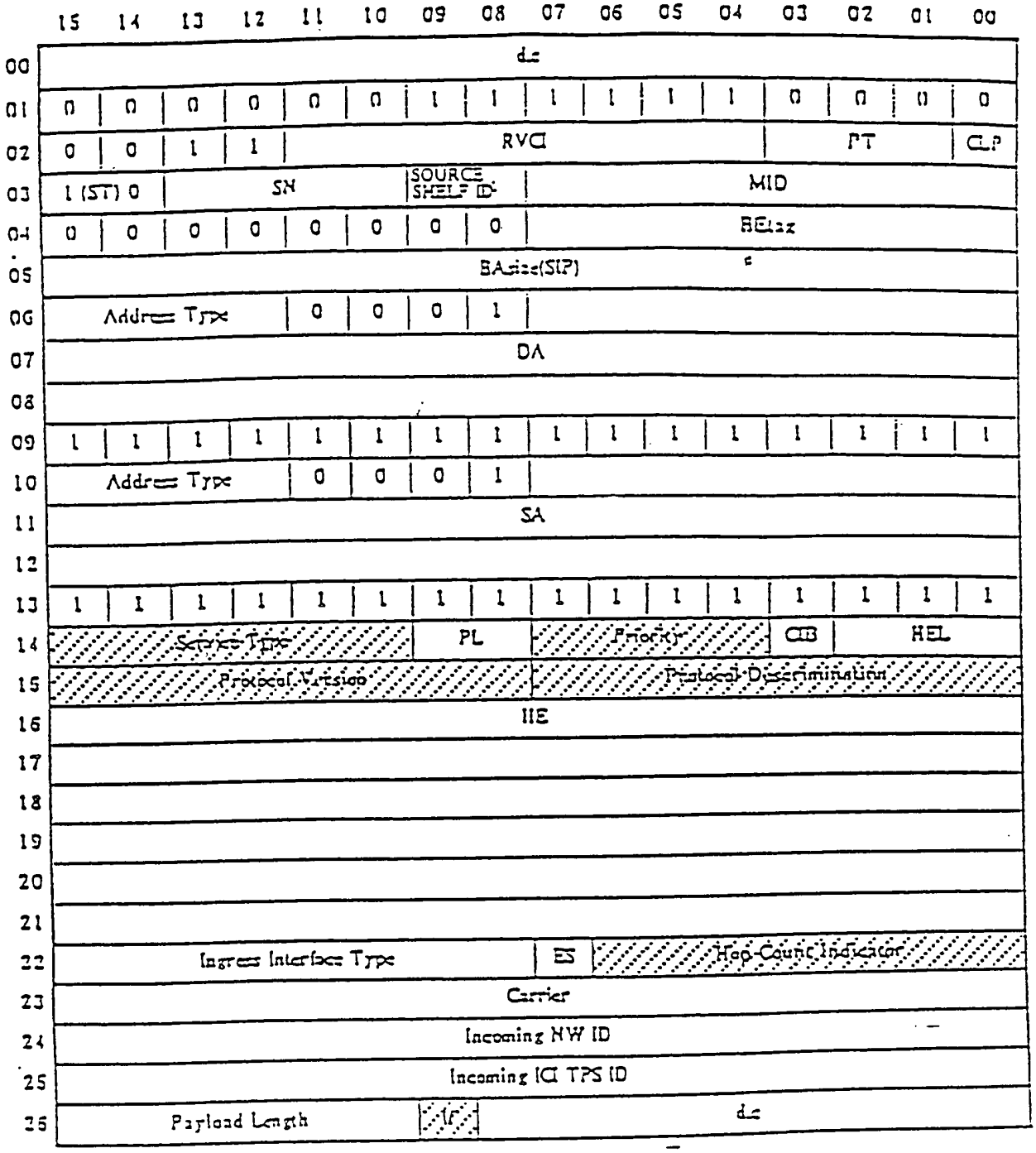
TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
IF:INTERFACE IDENTIFICATION(0=ISSI, 1=ICI)
LID:INPUT LINK NUMBER (0-7)

FIG. 521

	15	14	13	12	11	10	09	03	07	06	05	04	03	02	01	00
00	0	OAM	0	TAGA			0	0	0	TAGC			TAGB		0	0
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	IF	LID				PT			CLP
03	0 (ST) 1		SN				MID									
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
18	0	0	0	0	0	0	0	0	BEtag							
19	Length															
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	Payload Length						Payload CRC									

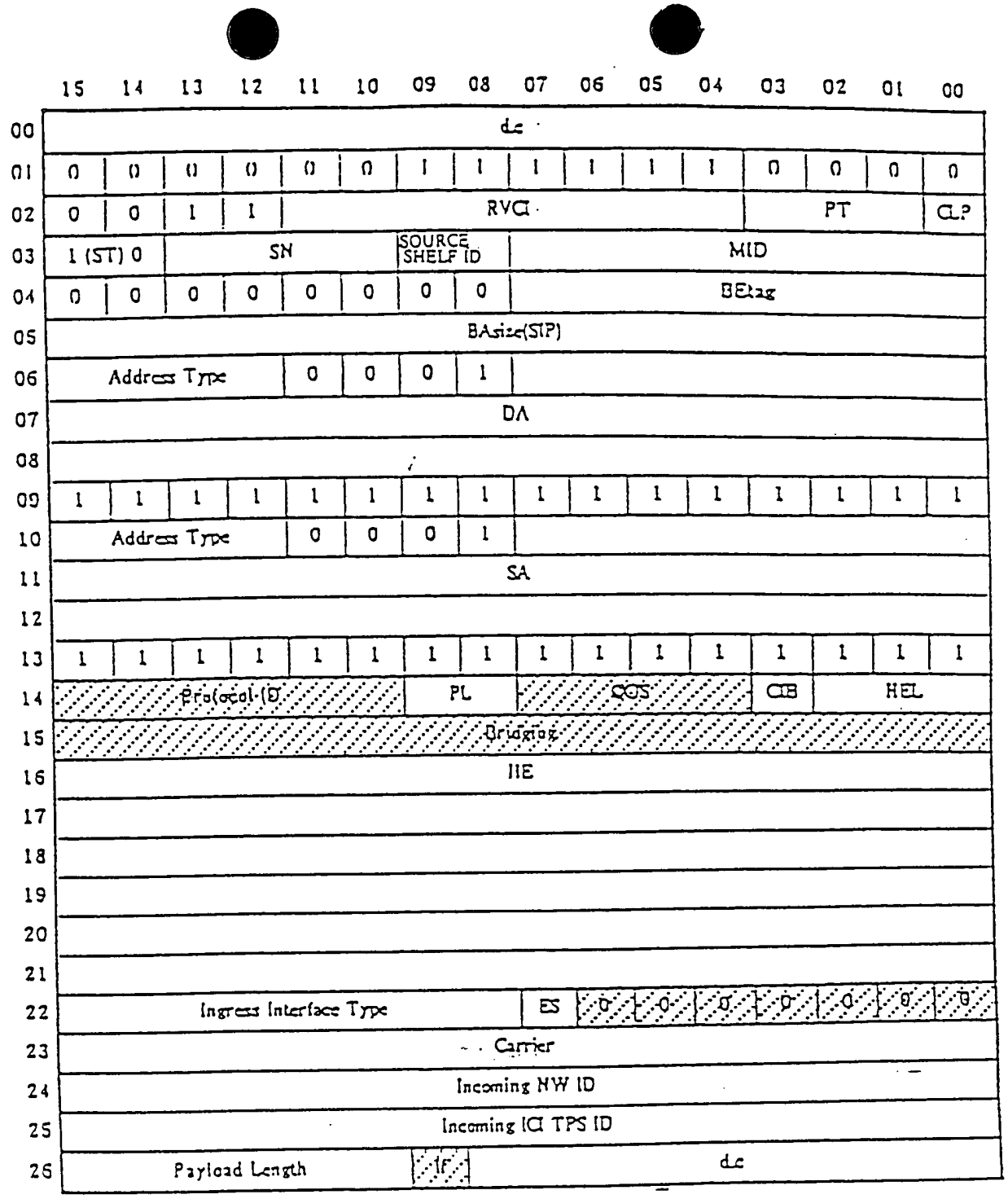
TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)
LID:INPUT LINK NUMBER (0-7)

FIG. 522



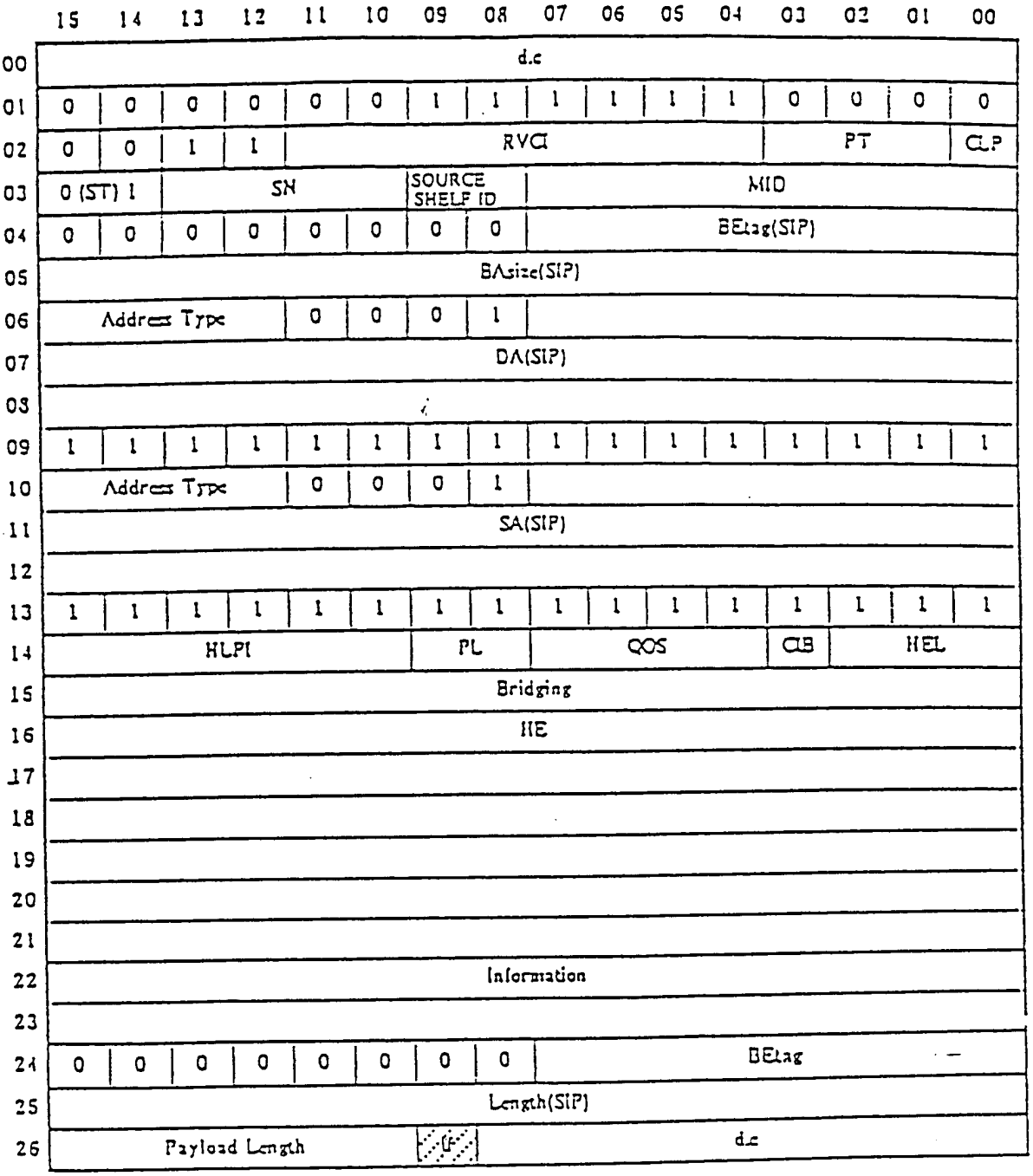
RVCI: DESTINATION MHID=SBMH (00-1Fh) AND GWMH (40-5Fh) FOR USER CELL
RVCI=FFh FOR MESH-MH TEST CELL
SOURCE SHELF ID: 0-3
BASIZE(SIP): ENCAPSULATION BASIZE-44
HOP COUNT INDICATOR: D.C WHEN DIRECTED FOR SBMH
IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)

FIG. 523



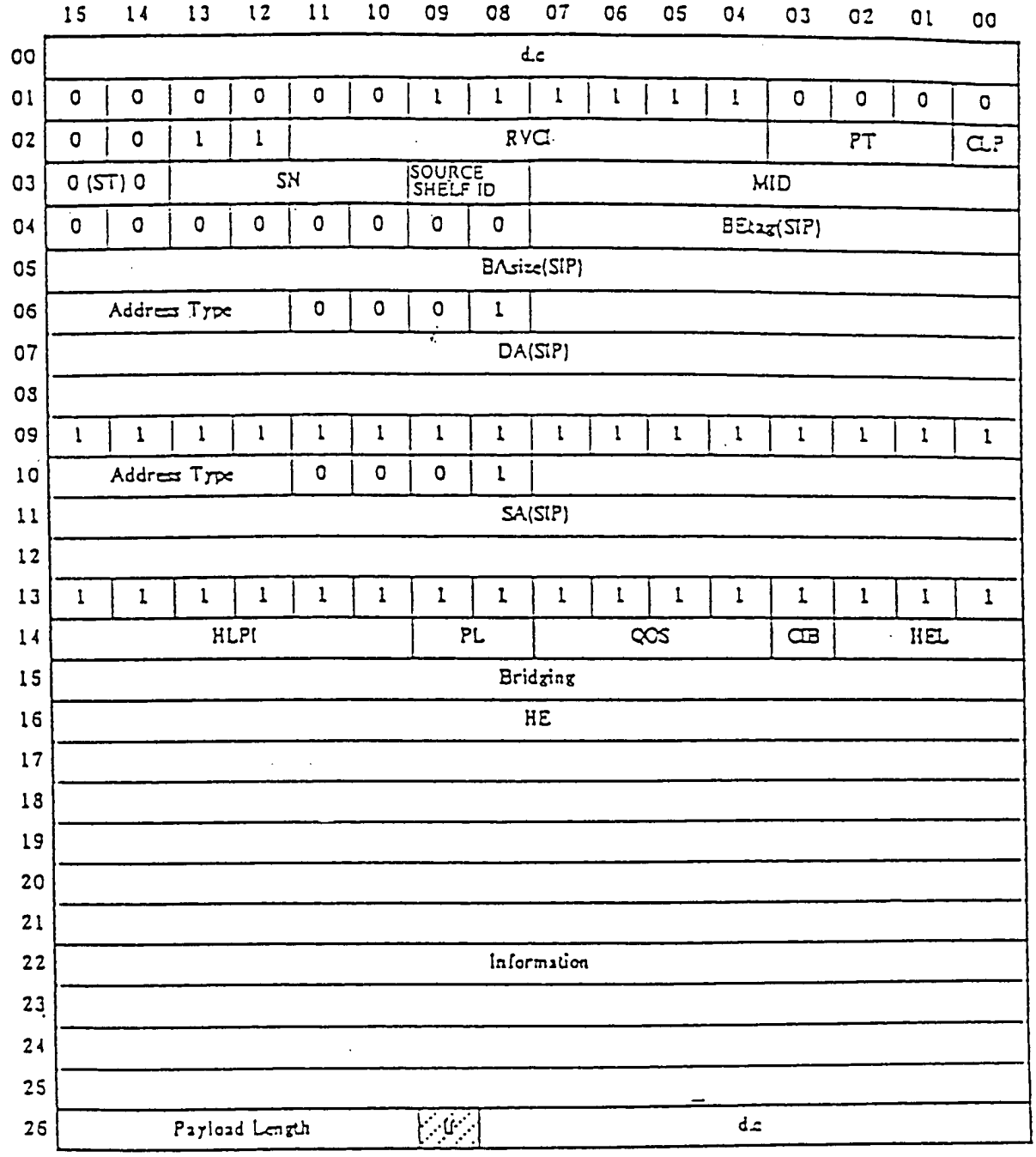
RVCI: DESTINATION MHID=SBMH (00-1Fh) AND GWMH (40-5Fh) FOR USER CELL
RVCI=FFh FOR MESH-MH TEST CELL
SOURCE SHELF ID: 0-3
BASIZE(SIP): ENCAPSULATION BASIZE-44
HOP COUNT INDICATOR: D.C WHEN DIRECTED FOR SBMH
IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)

FIG. 524



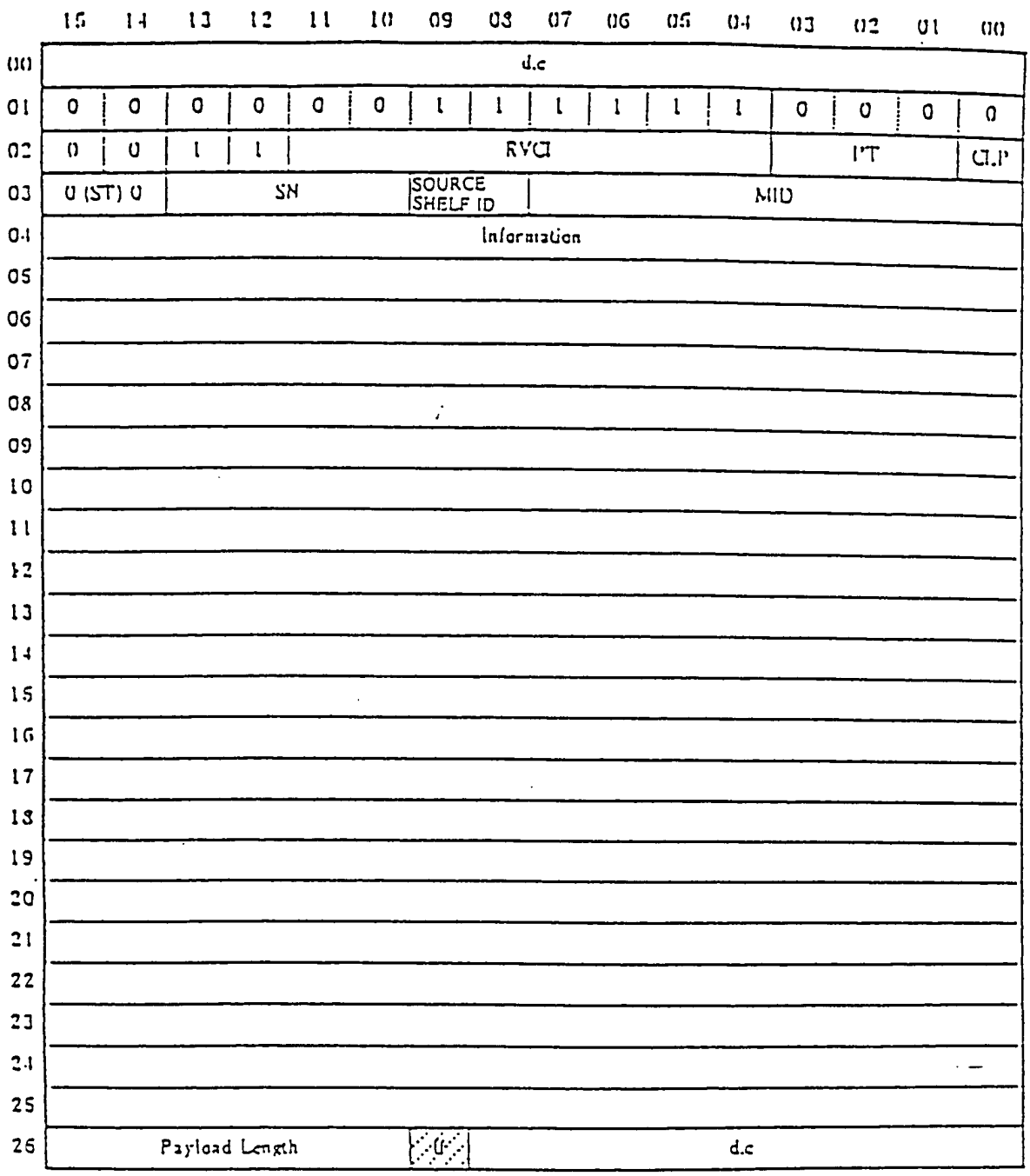
RVCI: DESTINATION MHID=SBMH (00-1Fh) AND GWMH (40-5Fh) FOR USER CELL
RVCI=FFh FOR MESH-MH TEST CELL
SOURCE SHELF ID: 0-3
LENGTH(SIP): ENVCAPSULATION LENGTH-44
IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)

FIG. 525



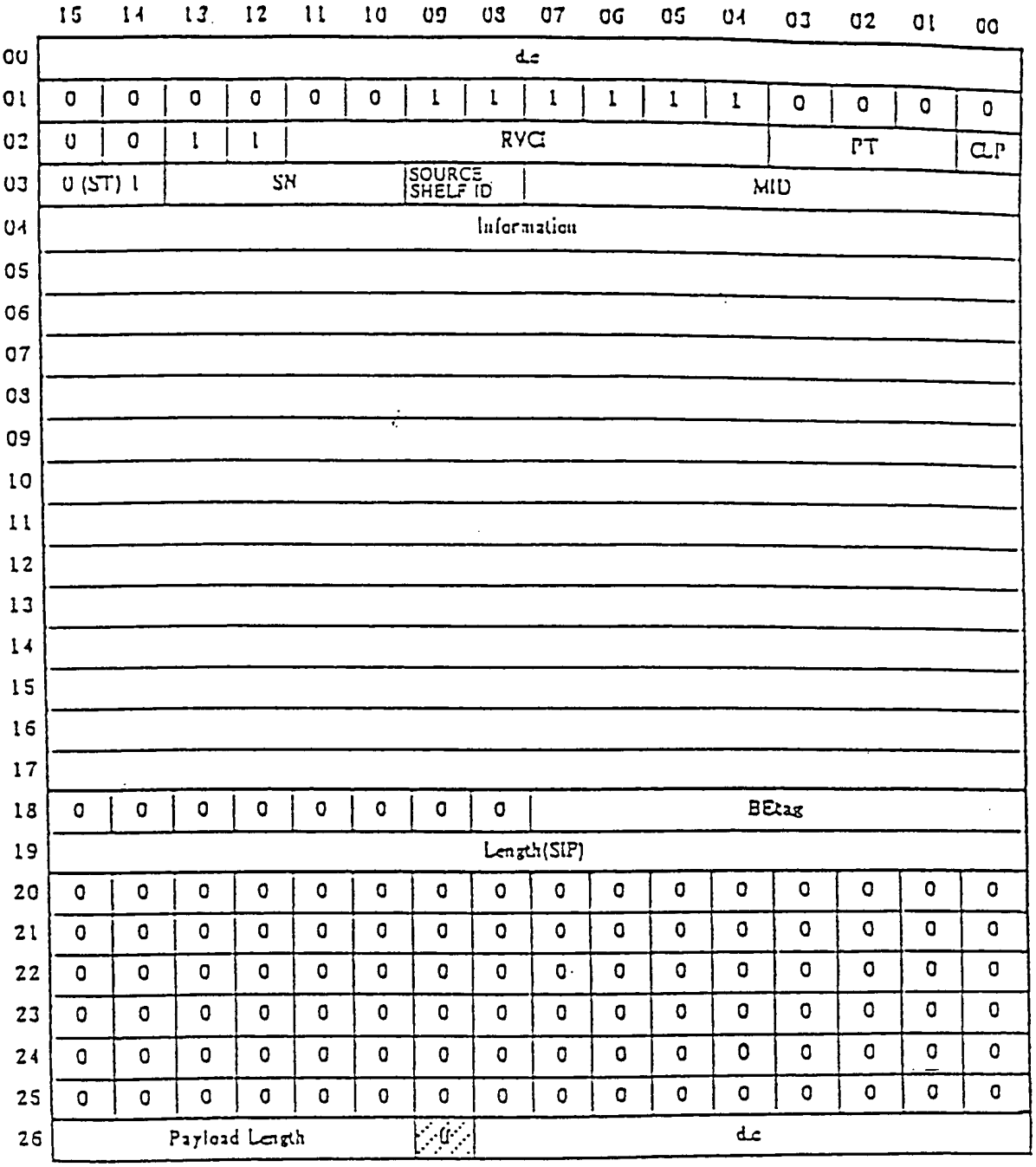
RVCI: DESTINATION MHID=SBMH (00-1Fh) AND GWMH (40-5Fh) FOR USER CELL
RVCI=FFh FOR MESH-MH TEST CELL
SOURCE SHELF ID: 0-3
IF: INTERFACE IDENTIFICATION(0=ISSI, I=ICI)

FIG. 526



RVCI: DESTINATION MHID=SBMH (00-1Fh) AND GWMH (40-5Fh) FOR USER CELL
RVCI=FFh FOR MESH-MH TEST CELL
SOURCE SHELF ID: 0-3
IF:INTERFACE IDENTIFICATION(0=ISSI, 1=ICI)

FIG. 527



RVCI: DESTINATION MHID=SBMH (00-1Fh) AND GWMH (40-5Fh) FOR USER CELL
RVCI=FFh FOR MESH-MH TEST CELL
SOURCE SHELF ID: 0-3
LENGTH(SIP): ENVCAPSULATION LENGTH-44
IF: INTERFACE IDENTIFICATION(0=ISSI, I=ICI)

FIG. 528

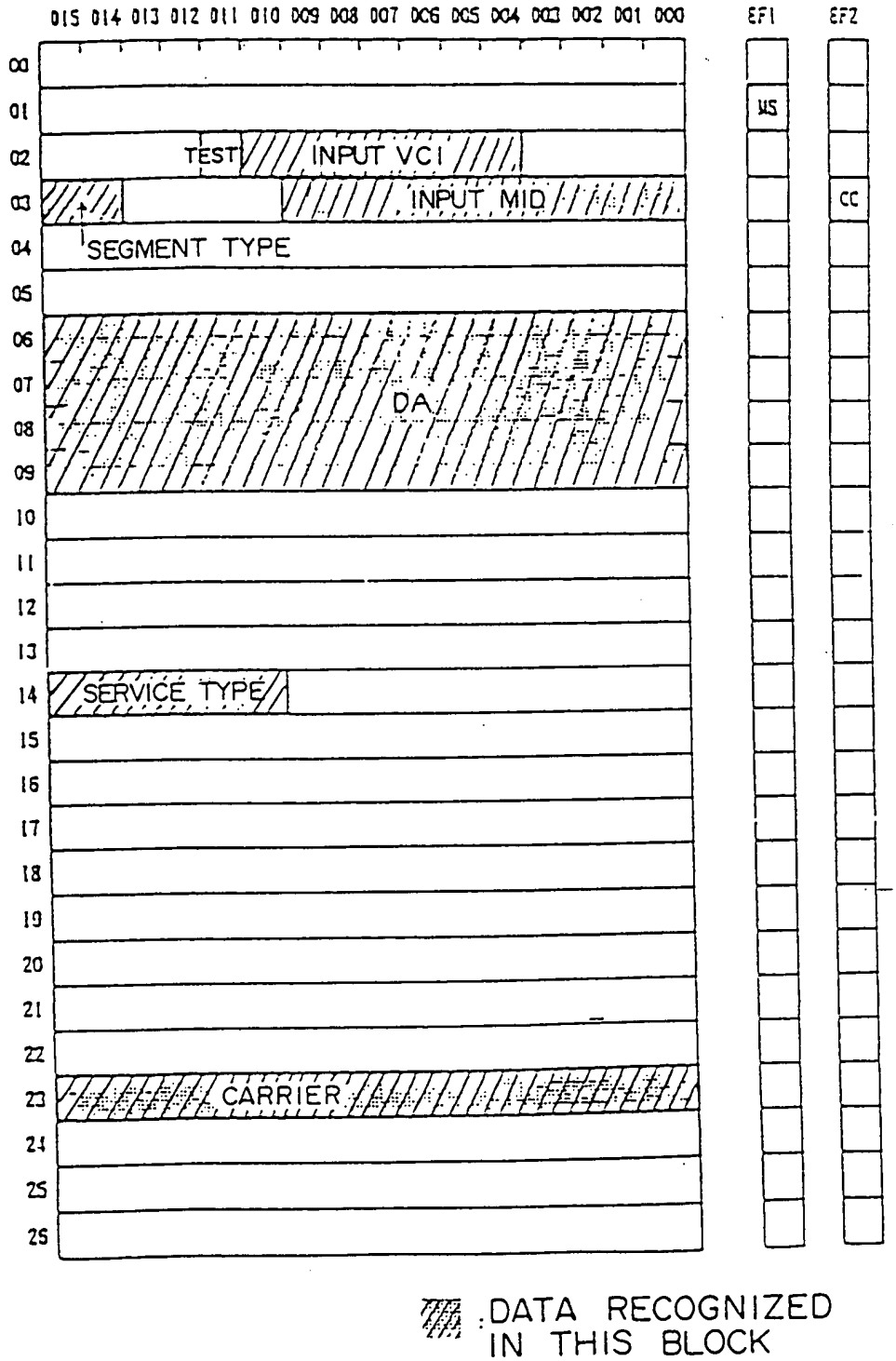

015 014 013 012 011 010 009 008 007 006 005 004 003 002 001 000
EF1
EF2
00
01
02
03
04
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
TEST
INPUT VCI
INPUT MID
SEGMENT TYPE
DA
SERVICE TYPE
CARRIER
MS
CC
: DATA RECOGNIZED IN THIS BLOCK

FIG. 529

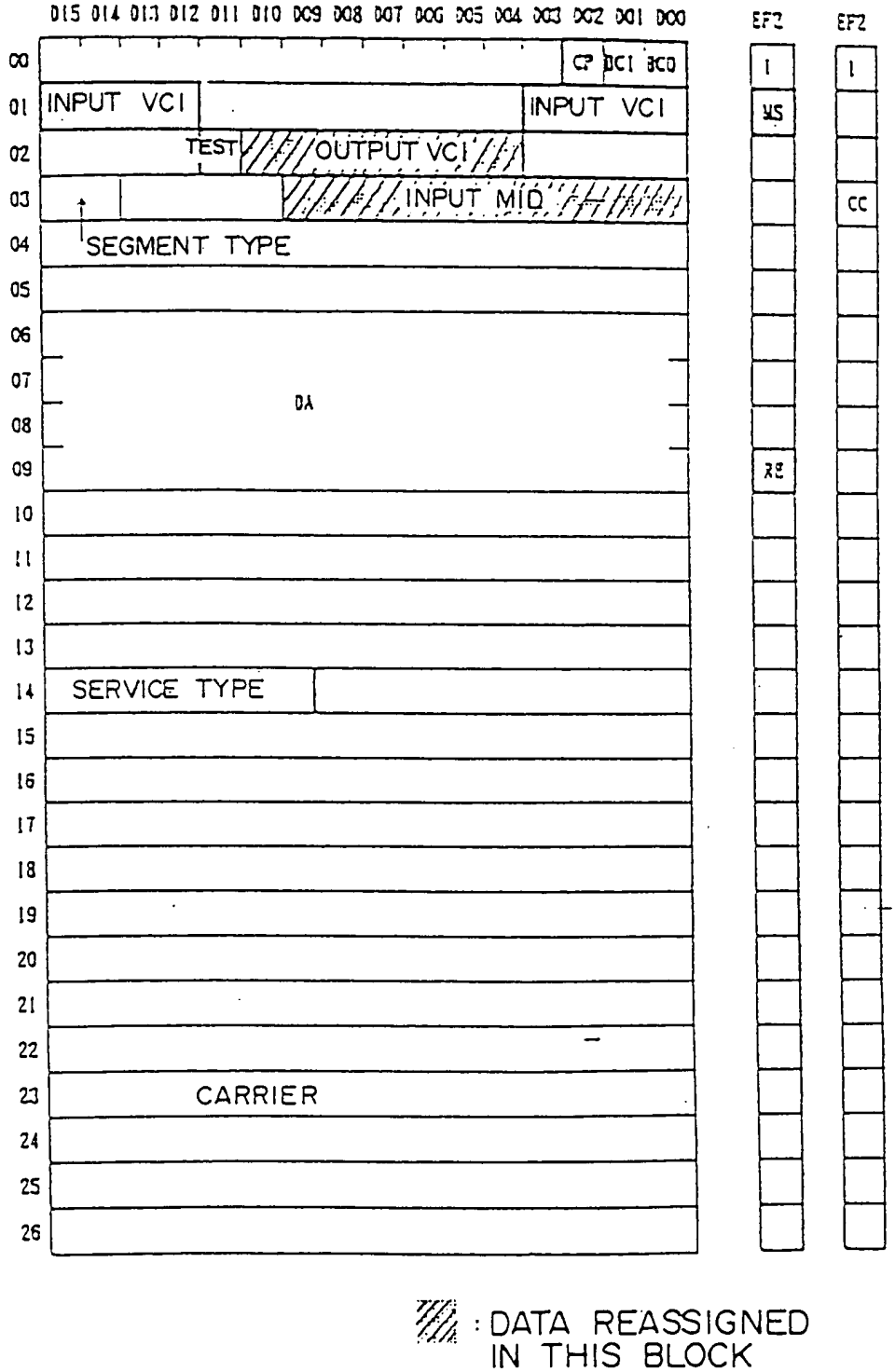

D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00
EF2
EF2
00
01
02
03
04
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
CP
DCI
BCD
I
MS
CC
RE
INPUT VCI
INPUT VCI
TEST
OUTPUT VCI
INPUT MID
SEGMENT TYPE
DA
SERVICE TYPE
CARRIER
: DATA REASSIGNED IN THIS BLOCK

FIG. 530

(BOM)

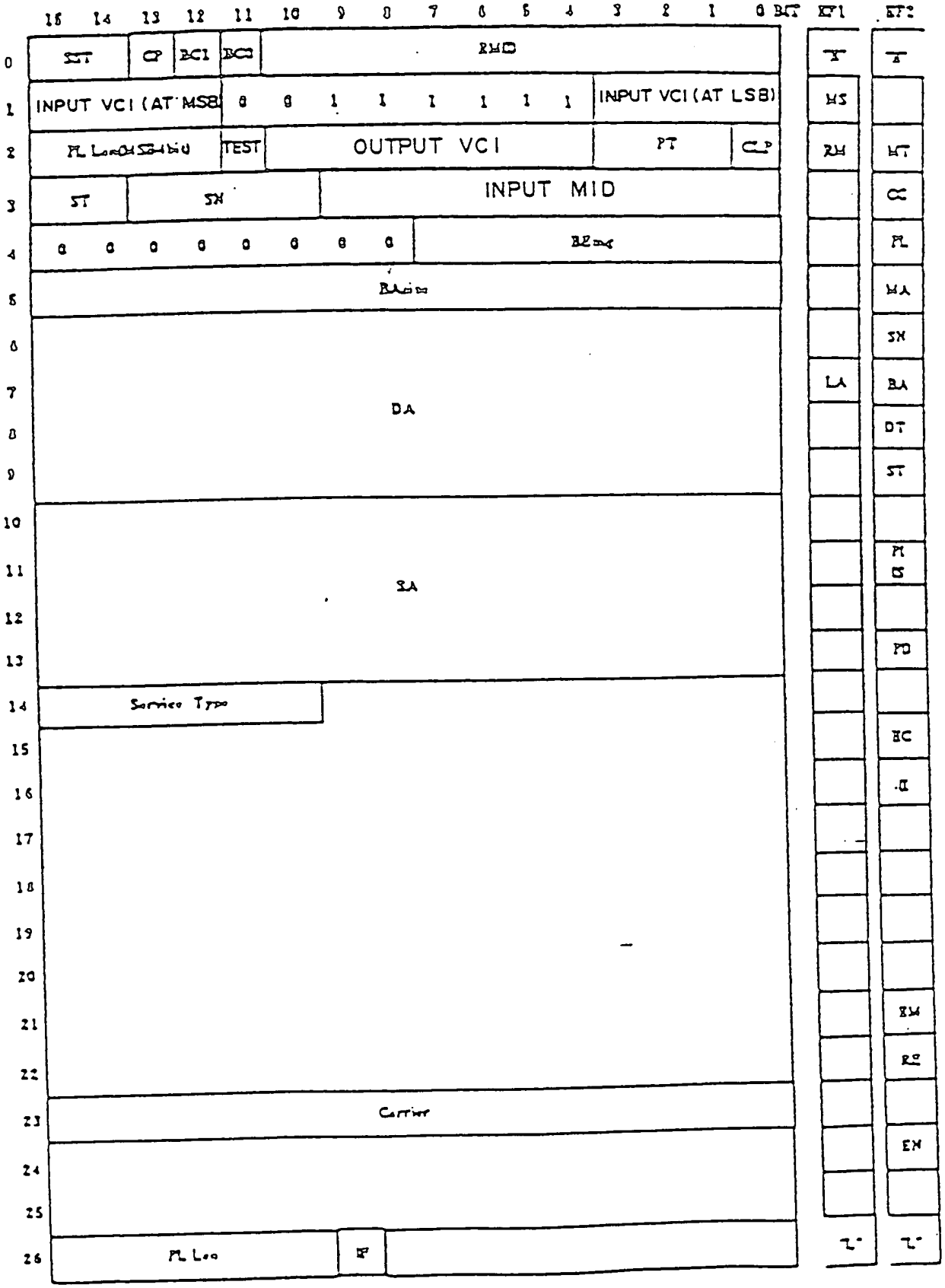

INPUT VCI (AT MSB)
INPUT VCI (AT LSB)
TEST
OUTPUT VCI
INPUT MID
DA
SA
Service Type

FIG. 531

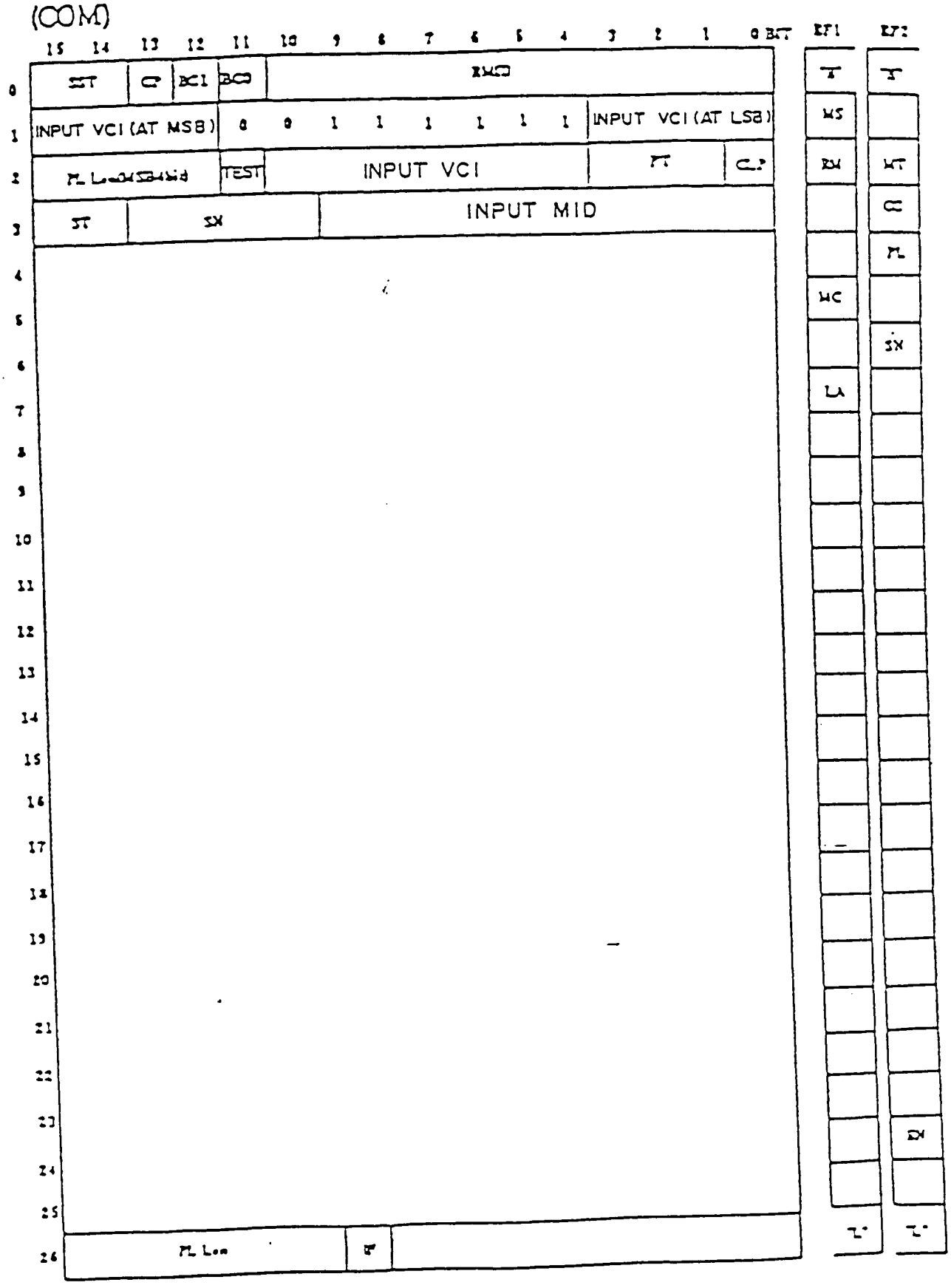

(COM)
INPUT VCI (AT MSB)
INPUT VCI (AT LSB)
TEST
INPUT VCI
INPUT MID
INPUT VCI (AT MSB)
INPUT VCI (AT LSB)
TEST
INPUT VCI
INPUT MID

FIG. 532

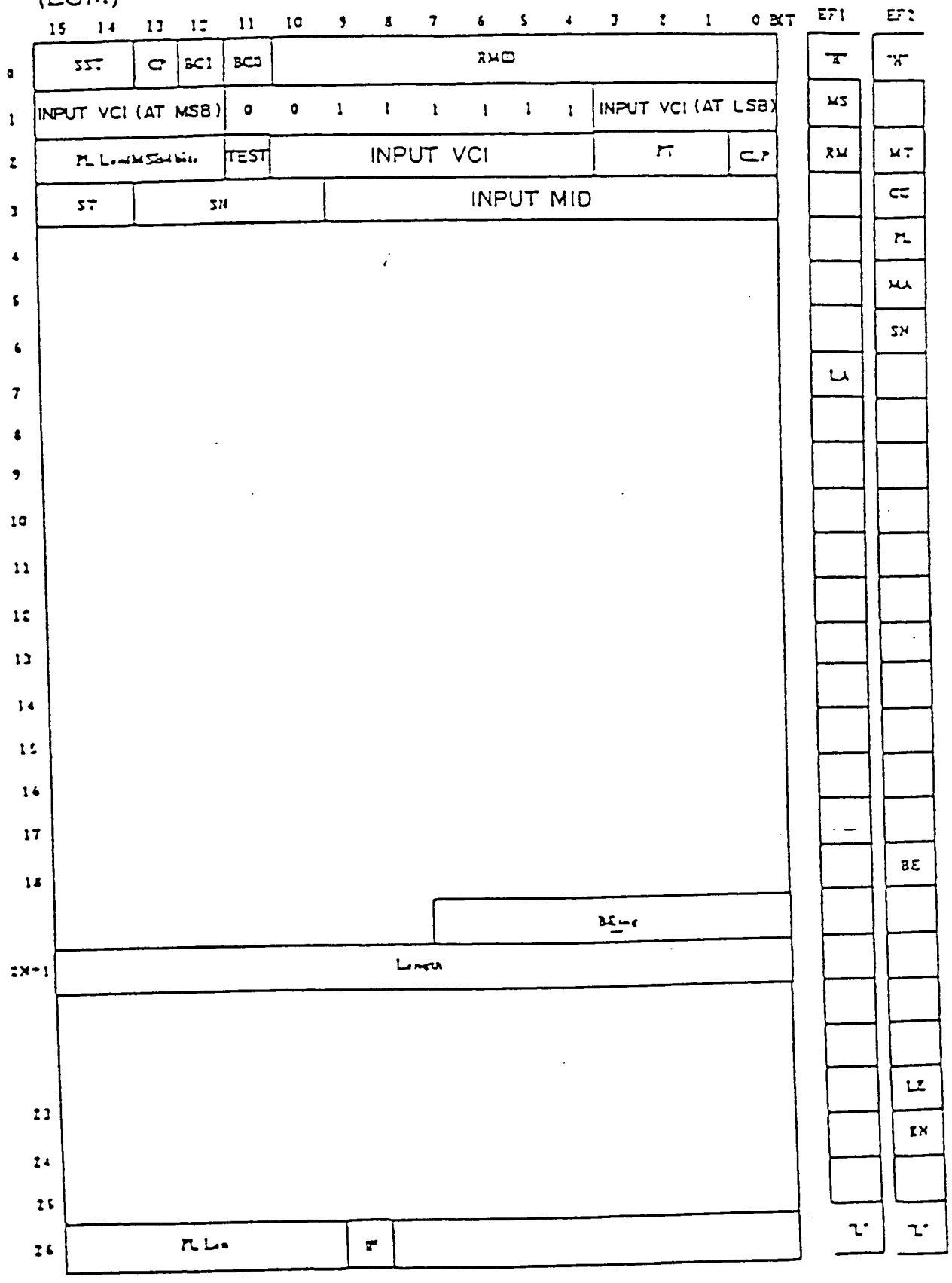

(EOM)
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 BIT
INPUT VCI (AT MSB)
0 0 1 1 1 1 1 1
INPUT VCI (AT LSB)
TEST
INPUT VCI
INPUT MID

FIG. 533

| EF1 |

MS : Master ERROR
RM : CC.PL NG OR
MC: MID not active (COM)
LA : LINK not active
(ODEN=H:not EN)

| EF2 |

MT : MRI time out
CC : Payload CRC violation
PL : Payload length error
MA : MID currently active or EOM with unapproved MID
SN : Invalid sequence number
BA : Invalid BAsize field value
DT : Invalid DA type
ST : Invalid SA type
PI : Invalid Protocol ID
(= IS : Invalid Service Type)
PD : Invalid Protocol Descriminator
HC : Hop Count=0
II : Ingress Interface Type
BE : BEtag mismatch
EM : Exceed maximum number of CDU
RE :Routing Error
LE : BAsize field not equal to length field
EN : Encapsulation error(Segment Type =SSM)

FIG. 534

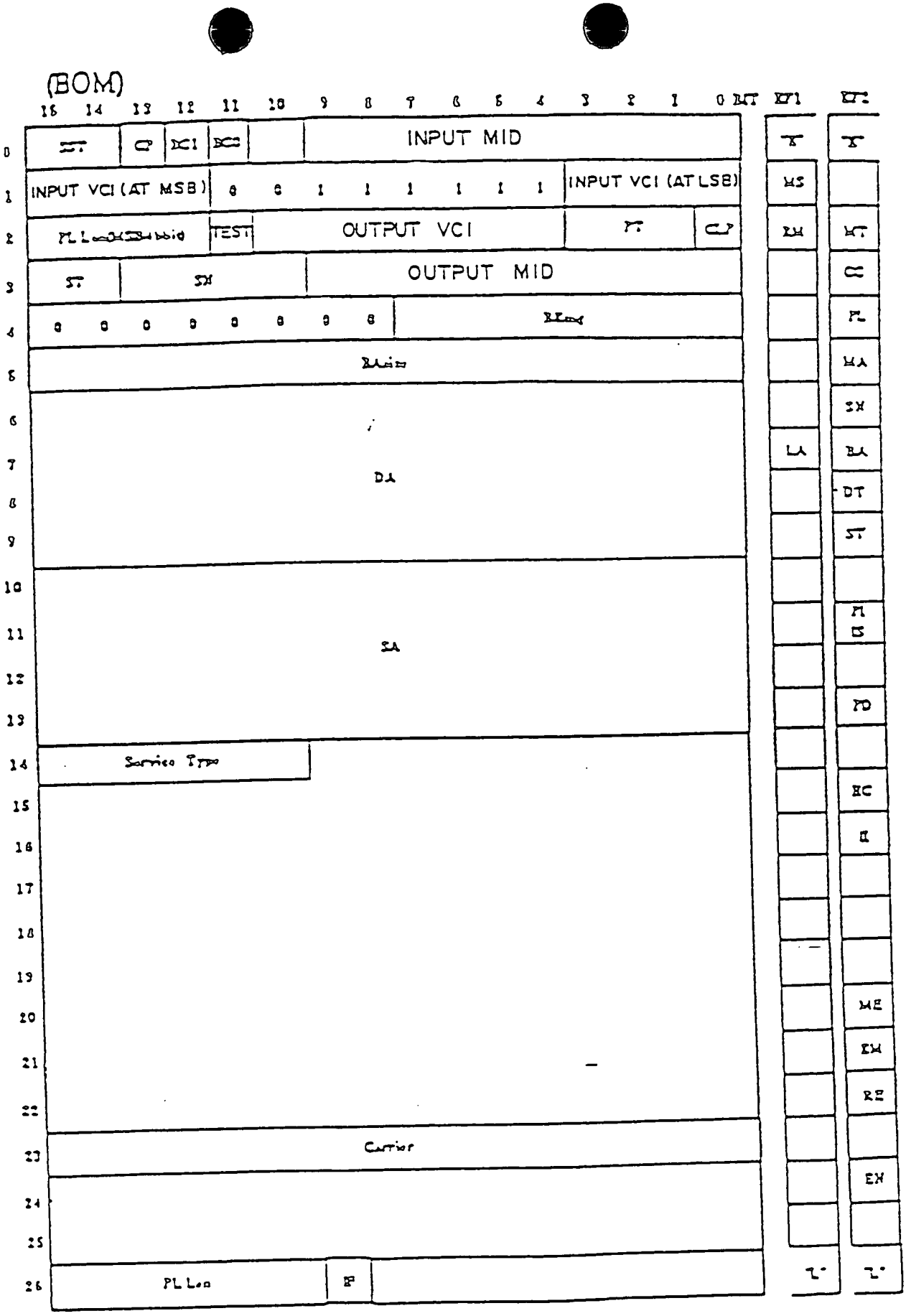

(BOM)
INPUT MID
INPUT VCI (AT MSB)
INPUT VCI (AT LSB)
TEST
OUTPUT VCI
OUTPUT MID
Service Type
Carrier
PL Len

FIG. 535

(COM)

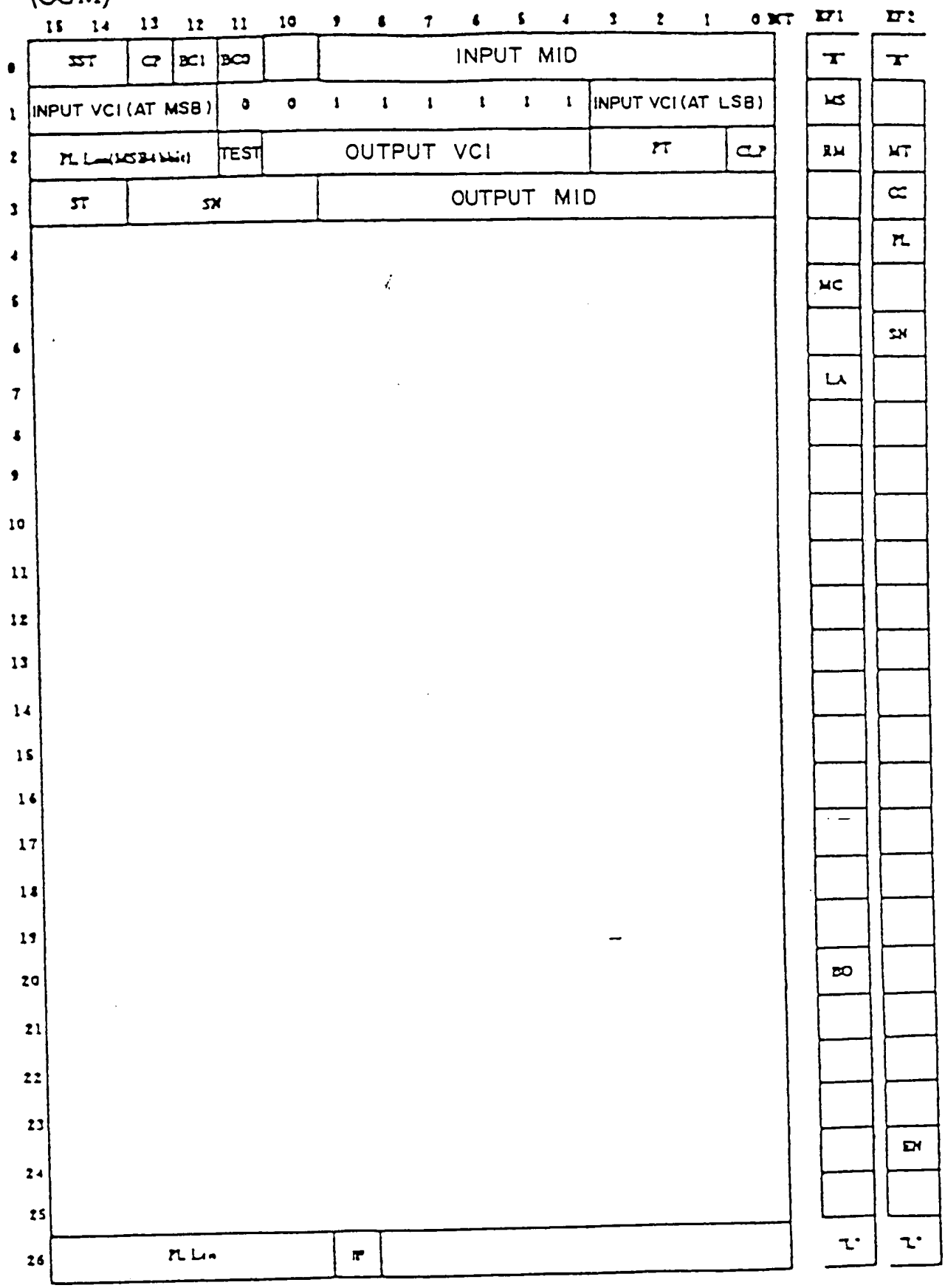

INPUT MID
INPUT VCI (AT MSB)
INPUT VCI (AT LSB)
TEST
OUTPUT VCI
OUTPUT MID

FIG. 536

(EOM)

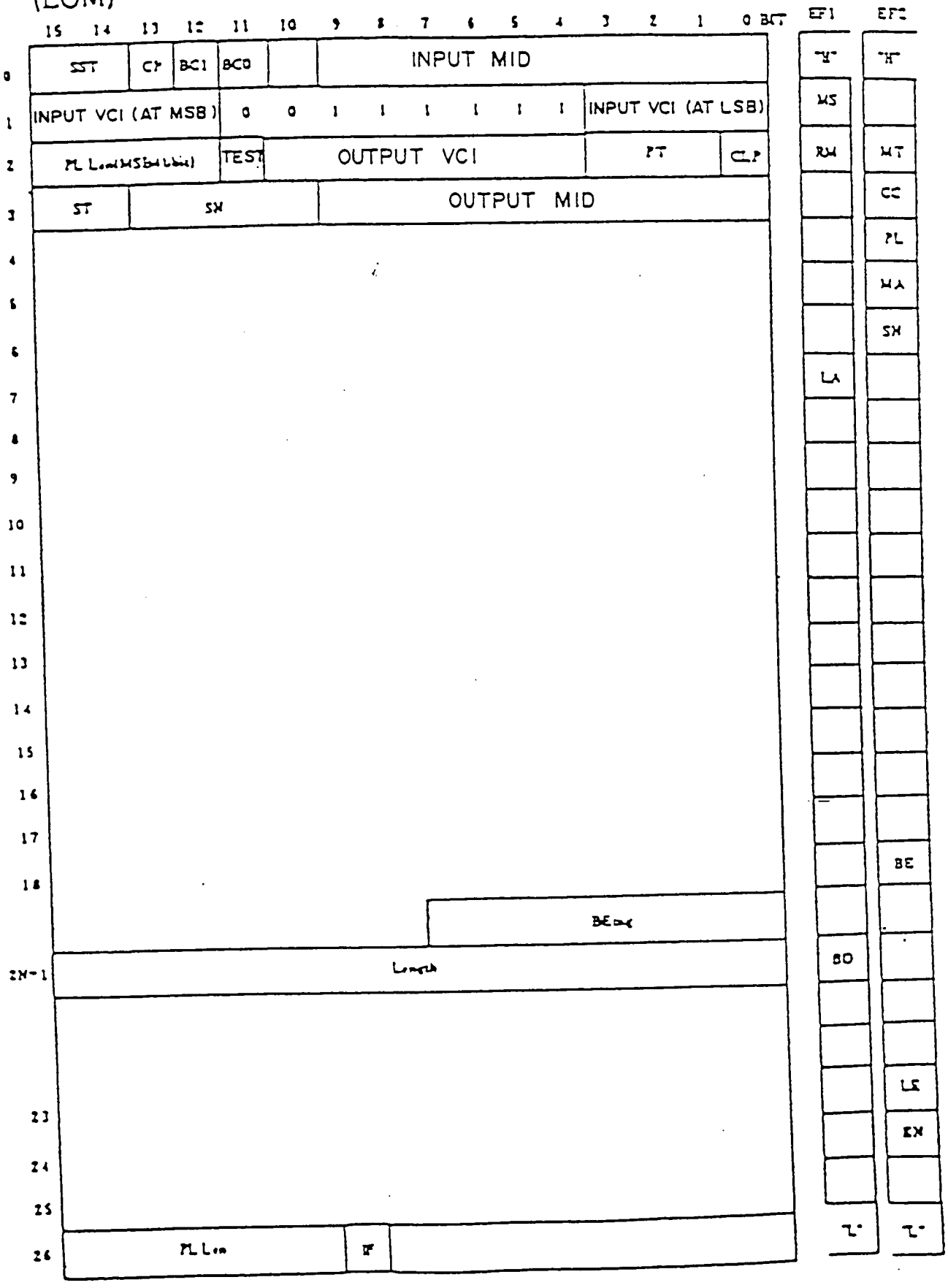

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 BIT
EF1
EF2
SST
CP
BC1
BC0
INPUT MID
INPUT VCI (AT MSB)
0 0 1 1 1 1 1 1
INPUT VCI (AT LSB)
TEST
OUTPUT VCI
PT
CLP
ST
SN
OUTPUT MID
MS
RM
CC
PL
MA
SN
LA
BE
BO
LS
EN
0
0
0
0

FIG 537

| EF1 |

MS : Master ERROR
RM : CC.PL NG OR
MC: MID not active (COM)
LA : LINK not active
(ODEN=H:not EN)
BD : BOM drop

| EF2 |

MT : MRI time out
CC : Payload CRC violation
PL : Payload length error
MA : MID currently active or EOM with unapproved MID
SN : Invalid sequence number
BA : Invalid BAsize field value
DT : Invalid DA type
ST : Invalid SA type
PI : Invalid Protocol ID
(= IS : Invalid Service Type)
PD : Invalid Protocol Descriminator
HC : Hop Count=0
II : Ingress Interface Type
BE : BEtag mismatch
ME:MID assign error
EM : Exceed maximum number of CDU
RE :Routing Error
LE : BAsize field not equal to length field
EN : Encapsulation error(Segment Type =SSM)

FIG. 538

(BOM)

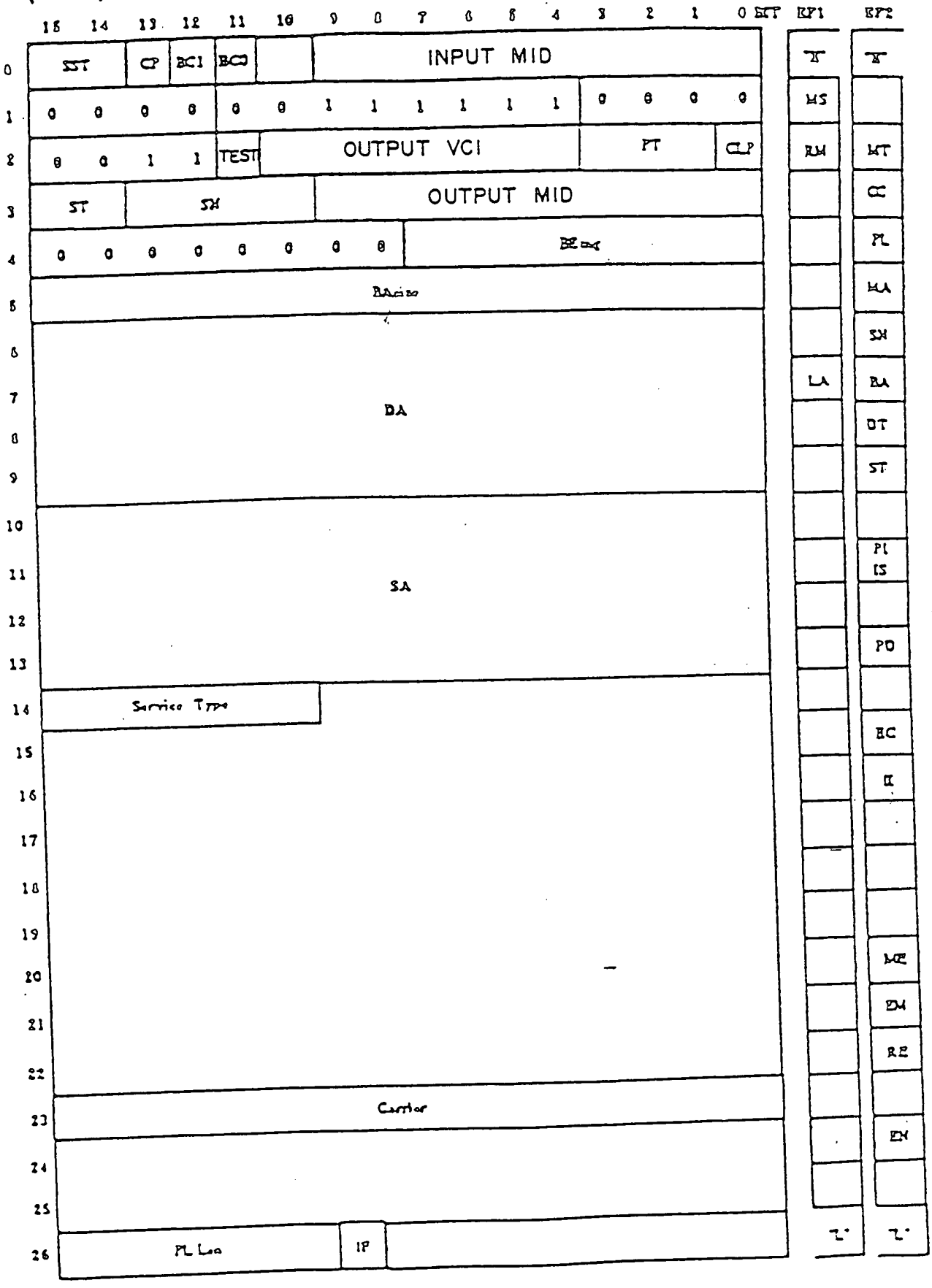

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 BIT
INPUT MID
OUTPUT VCI
TEST
OUTPUT MID
DA
SA
Service Type
Carrier
PL Len
IP

FIG. 539

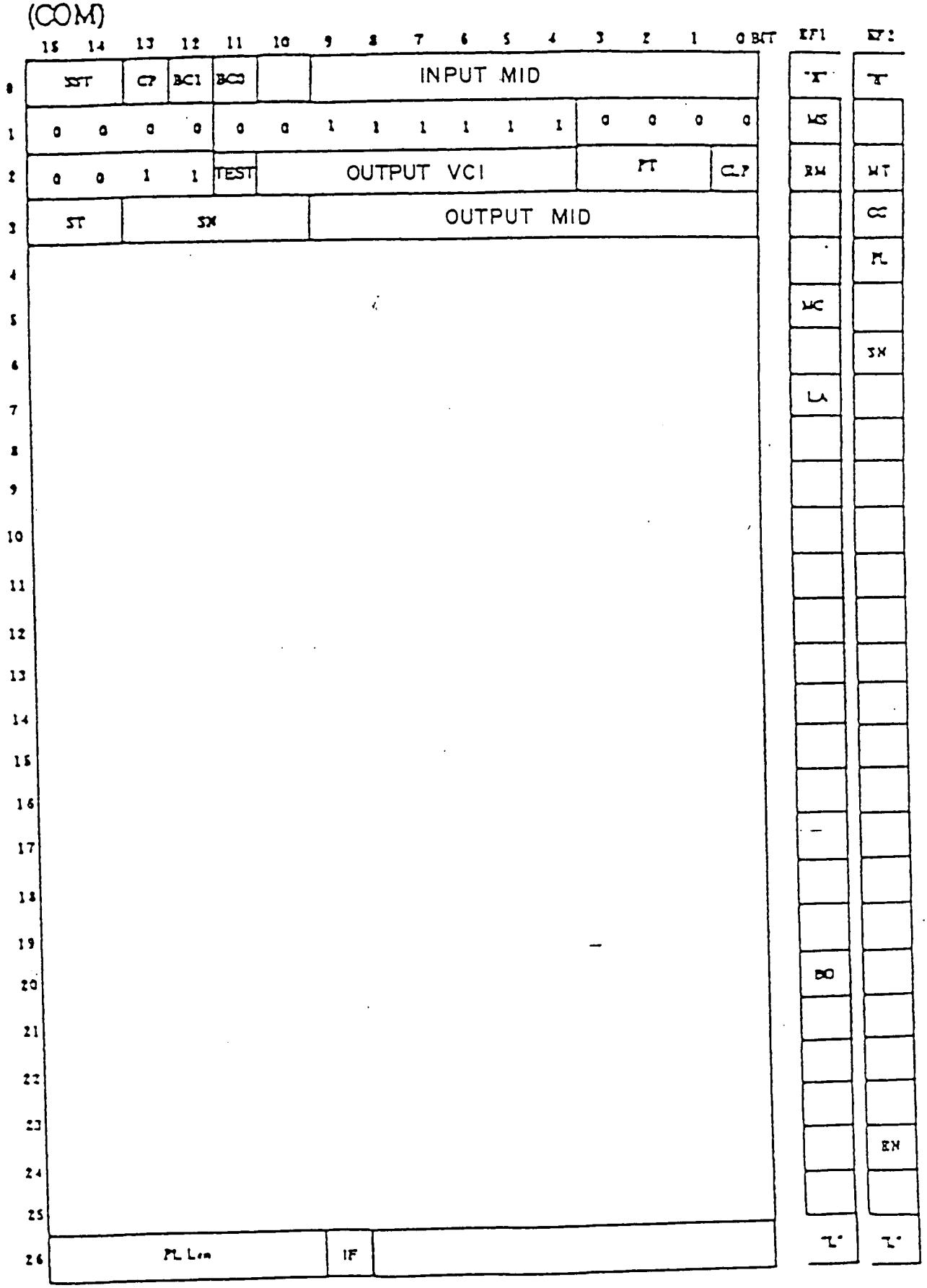

(COM)
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 BIT
INPUT MID
0 0 0 0 0 0 1 1 1 1 1 1 0 0 0 0
0 0 1 1 TEST OUTPUT VCI
OUTPUT MID
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

FIG. 540

(EOM)

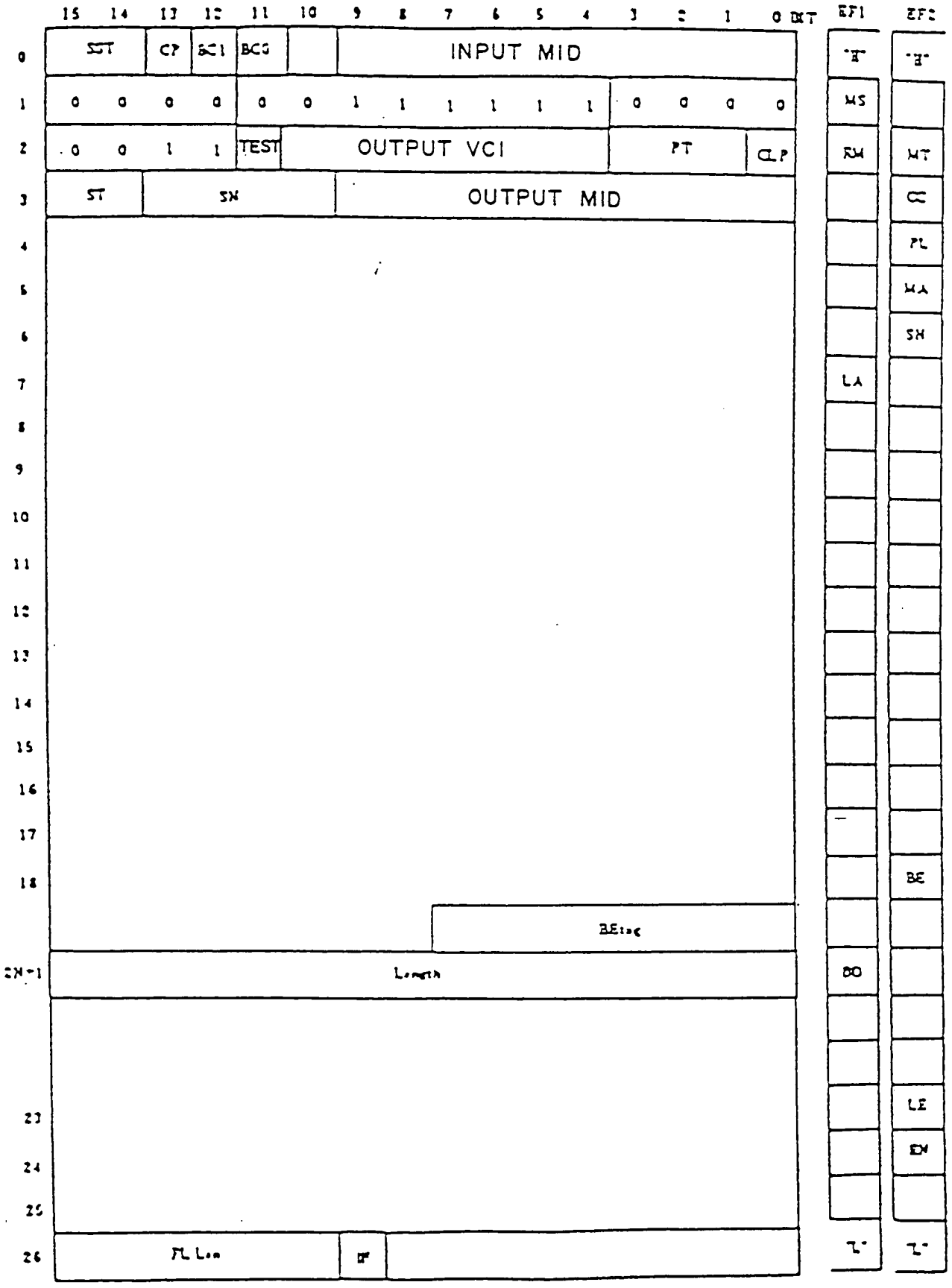

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 BIT
EFI
EFO
SST
CP
BCI
BCO
INPUT MID
TEST
OUTPUT VCI
PT
CLP
ST
SN
OUTPUT MID
Length
CRC

FIG. 541

| EF1 |

MS : Master ERROR
RM : CC,PL NG OR
MC: MID not active (COM)
LA : LINK not active
(ODEN=H:not EN)
BD : BOM drown

| EF2 |

MT : MRI time out
CC : Payload CRC violation
PL : Payload length error
MA : MID currently active or EOM with unapproved MID
SN : Invalid sequence number
BA : Invalid BAsize field value
DT : Invalid DA type
ST : Invalid SA type
PI : Invalid Protocol ID
(= IS : Invalid Service Type)
PD : Invalid Protocol Descriminator
HC : Hop Count=0
II : Ingress Interface Type
BE : BEtag mismatch
ME:MID assign error
EM : Exceed maximum number of CDU
RE :Routing Error
LE : BAsize field not equal to length field
EN : Encapsulation error(Segment Type =SSM)

FIG. 542

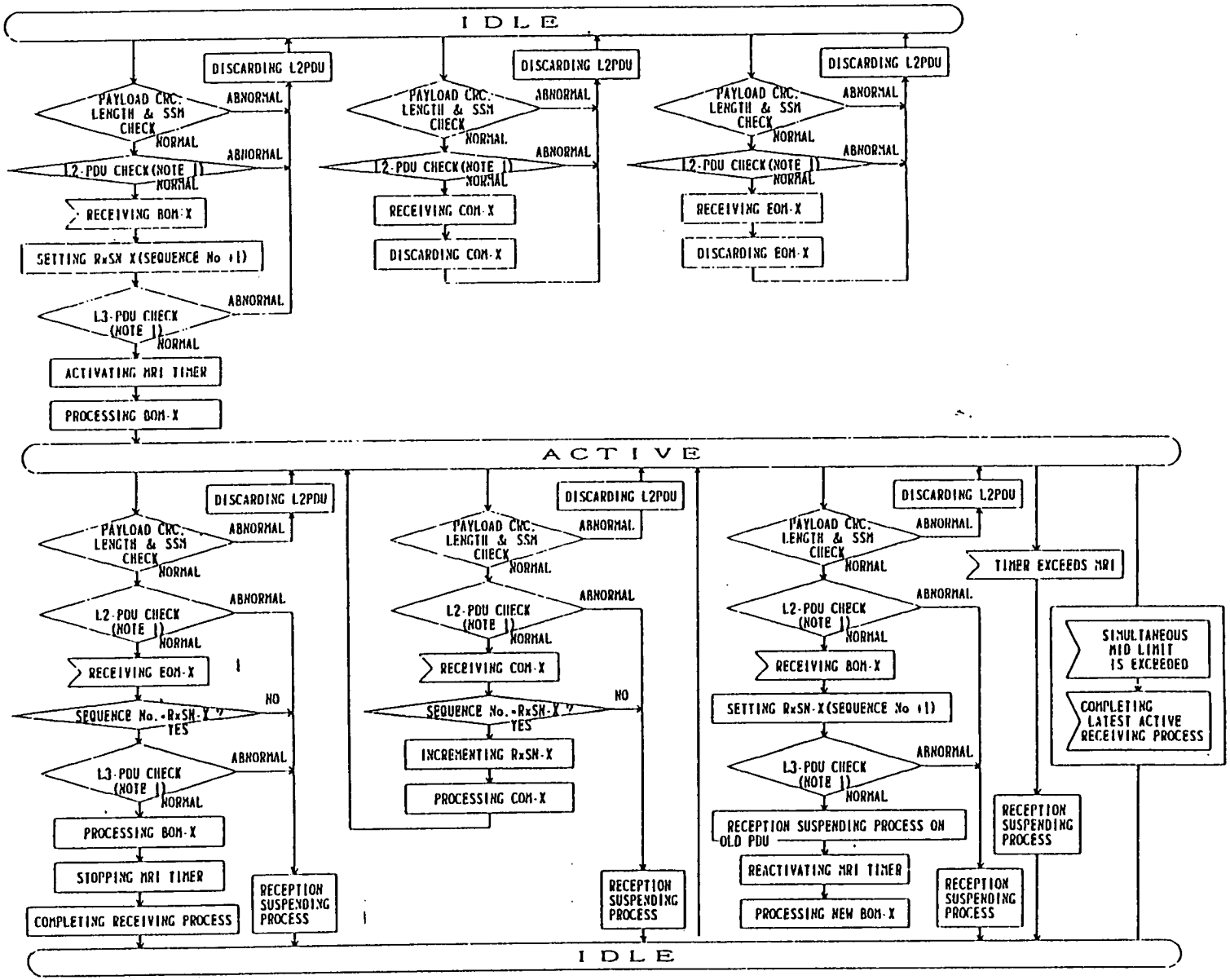

IDLE
DISCARDING L2PDU
PAYLOAD CRC, LENGTH & SSM CHECK
ABNORMAL
NORMAL
L2-PDU CHECK (NOTE 1)
RECEIVING BOM-X
SETTING RxSN-X (SEQUENCE No +1)
L3-PDU CHECK (NOTE 1)
ACTIVATING MRI TIMER
PROCESSING BOM-X
RECEIVING COM-X
DISCARDING COM-X
RECEIVING EOM-X
DISCARDING EOM-X
ACTIVE
SEQUENCE No.=RxSN-X ?
NO
YES
RECEPTION SUSPENDING PROCESS
PROCESSING COM-X
INCREMENTING RxSN-X
STOPPING MRI TIMER
COMPLETING RECEIVING PROCESS
TIMER EXCEEDS MRI
SIMULTANEOUS MID LIMIT IS EXCEEDED
COMPLETING LATEST ACTIVE RECEIVING PROCESS
RECEPTION SUSPENDING PROCESS ON OLD PDU
REACTIVATING MRI TIMER
PROCESSING NEW BOM-X

FIG. 543

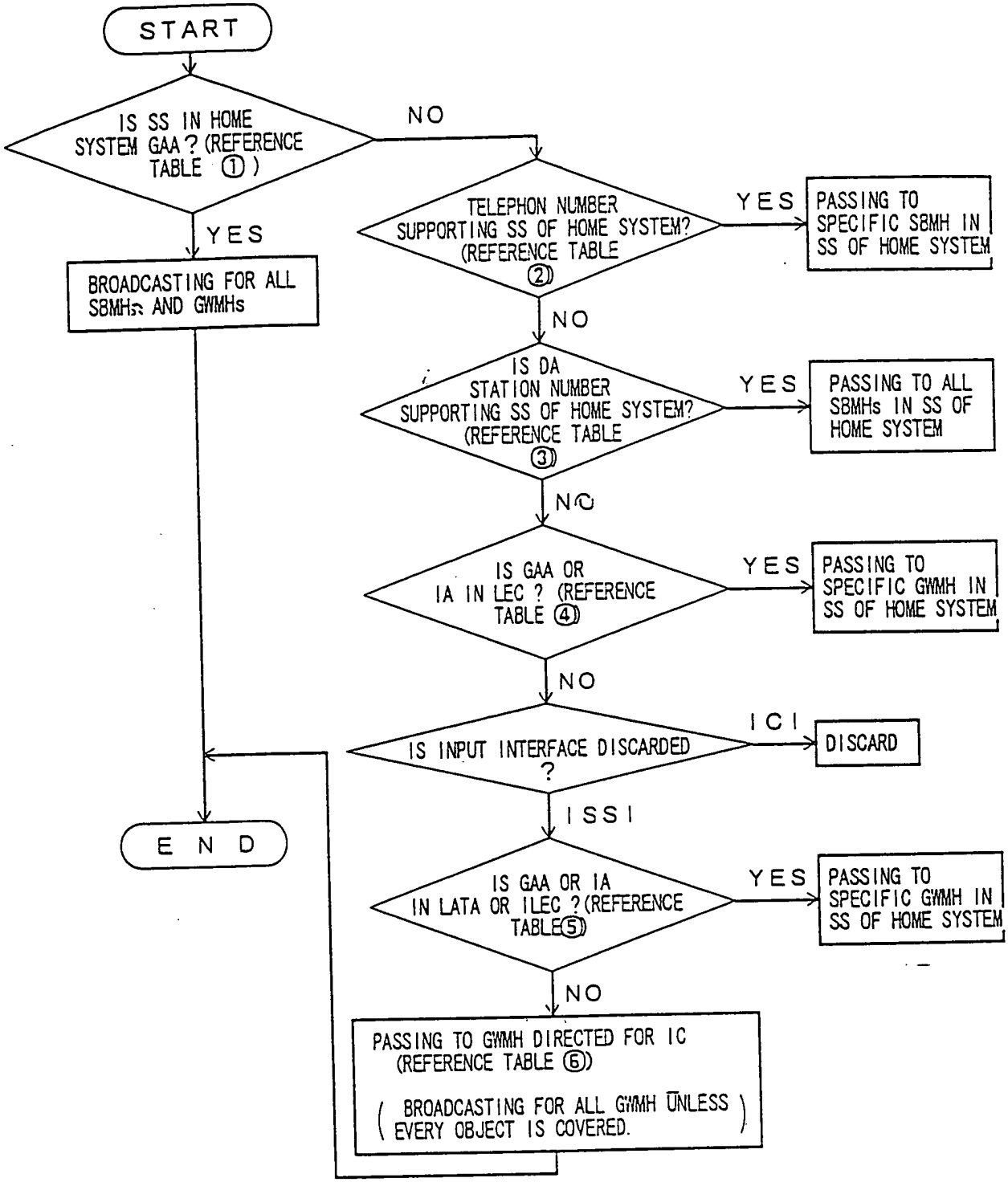

START
IS SS IN HOME SYSTEM GAA ? (REFERENCE TABLE ①)
NO
YES
BROADCASTING FOR ALL SBMHs AND GWMHs
TELEPHON NUMBER SUPPORTING SS OF HOME SYSTEM? (REFERENCE TABLE ②)
YES
PASSING TO SPECIFIC SBMH IN SS OF HOME SYSTEM
NO
IS DA STATION NUMBER SUPPORTING SS OF HOME SYSTEM? (REFERENCE TABLE ③)
YES
PASSING TO ALL SBMHs IN SS OF HOME SYSTEM
NO
IS GAA OR IA IN LEC ? (REFERENCE TABLE ④)
YES
PASSING TO SPECIFIC GWMH IN SS OF HOME SYSTEM
NO
IS INPUT INTERFACE DISCARDED ?
ICI
DISCARD
ISSI
IS GAA OR IA IN LATA OR ILEC ? (REFERENCE TABLE ⑤)
YES
PASSING TO SPECIFIC GWMH IN SS OF HOME SYSTEM
NO
PASSING TO GWMH DIRECTED FOR IC (REFERENCE TABLE ⑥)
(BROADCASTING FOR ALL GWMH UNLESS EVERY OBJECT IS COVERED.)
END

FIG. 544

① DETERMINING WHETEHR OR NOT SS IN HOME SYSTEM IS GAA ACCORDING TO GAA LIST.

	GAA LIST (64 bit)
1024 (W)	.....

② DETERMINING WHETEHR OR NOT THERE IS SBMH FOR SUPPORTING SNI OF HOME SYSTEM ACCORDING TO DA (TELEPHONE NUMBER).

	DA (64 bit)	SBMH No (5 bit)
2048 (W)	.....	.....

③ DETERMINING WHETHER OR NOT STATION NUMBER REFERS TO SS IN HOME SYSTEM ACCORDING TO STATION NUMBER OF DA.

	STATION NUMBER (32 bit)
64 (W)	.....

④ AT GA : DETERMINING WHETHER OR NOT THERE IS SS IN LEC OF HOME SYSTEM FOR SUPPORTING GAA ACCORDING TO (STATION NUMBER) OF DA.

	GAA STATION NUMBER IN LEC (32 bit)	GWMH No (5 bit)
1024 (W)	.....	.....

AT IA : DETERMINING WHETHER OR NOT THERE IS SS IN LEC OF HOME SYSTEM FOR SUPPORTING IA ACCORDING TO (STATION NUMBER) OF DA.

	IA STATION NUMBER IN LEC (32 bit)	GWMH No (5 bit)
1024 (W)	.....	.....

⑤ AT GA : DETERMINING WHETHER OR NOT THERE IS SS IN LATA FOR SUPPORTING GAA ACCORDING TO (STATION NUMBER) OF DA.

	ILEC GAA STATION NUMBER (32 bit)	GWMH No (5 bit)
1024 (W)	.....	.....

AT IA : DETERMINING WHETHER OR NOT THERE IS SS IN LATA FOR SUPPORTING IA ACCORDING TO (STATION NUMBER) OF DA.

	ILEC IA STATION NUMBER (32 bit)	GWMH No (5 bit)
1024 (W)	.....	.....

TOTAL STATION NUMBER OF TABLES ③~⑤ IS 512.

⑥ DETERMINING GWMH No. FOR SUPPORTING ICI TO IC ACCORDING TO SMDS CIC.

	SMDS CIC (16 bit)	GWMH No (5 bit)
256 (W)	.....	.....

FIG. 545

6,592,260 B1

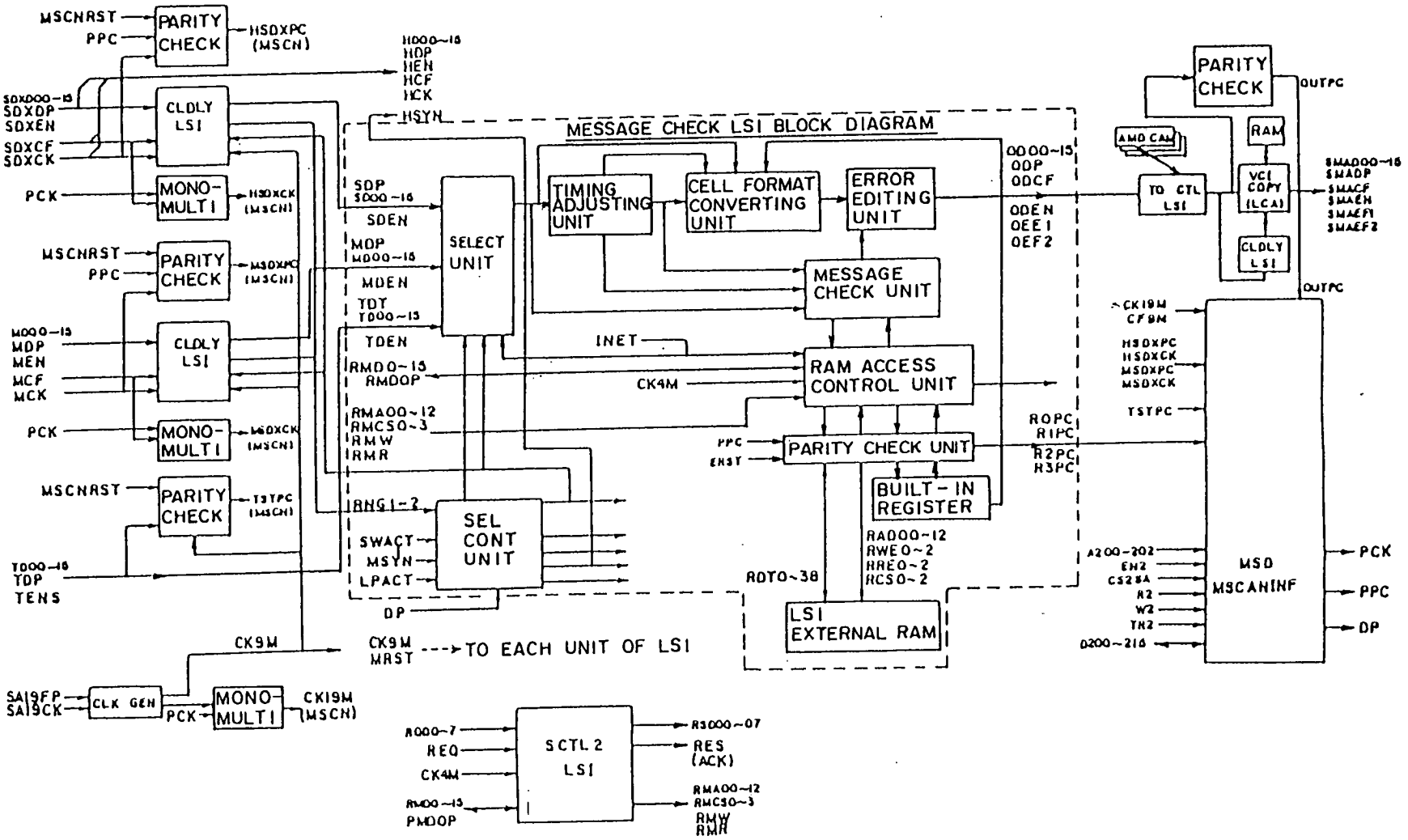


FIG. 546

NAME	POLARITY	LEVEL	POSITION	EXPLANATION OF FUNCTION	REMARKS
SDXD00～15	P	TTL	BWB	HIGHWAY DATA OF SDMX →ICLP. MSB FOR SDXD15, AND LSB FOR SDXD00	
SDXDP	P	TTL	BWB	ODD PARITY FOR SDXDxx AND SDXEN	
SDXEN	N	TTL	BWB	ENABLE OF SDSMX→ ICLP	
SDXCF	N	TTL	BWB	CELL FRAME OF SDMX →ICLP	
SDXCK	CLK	TTL	BWB	9MHZ CLK IN PARALLEL TO HIGHWAY DATA OF SDMX → ICLP	
MD00～15	P	TTL	FCN	HIGHWAY DATA OF MATE ICLP. MSB FOR MD15, AND LSB FOR MD00	
MDP	P	TTL	FCN	ODD PARITY FOR MDxx AND MEN	
MEN	N	TTL	FCN	ENABLE OF MATE ICLP	
MCF	N	TTL	FCN	CELL FRAME OF MATE ICLP	
MCK	CLK	TTL	FCN	9MHZ CLK IN PARALLEL TO HIGHWAY DATA OF MATE ICLP	
TD00～15	P	TTL	BWB	TEST DATA OF HLP07 →ICLP. MSB FOR TD15, AND LSB FOR TD00	
TDP	P	TTL	BWB	ODD PARITY FOR TDxx AND TENS	
TENS	N	TTL	BWB	TEST CELL ENABLE	
TS00	N	TTL	BWB	ICLP CELL FRAME	
TS01	N	TTL	BWB	TEST CELL SEND OK/NG	
SMAD00～15	P	TTL	BWB	HIGHWAY DATA OF HMH11A →HMH09A. MSB FOR SMAD15, AND LSB FOR SMAD00	
SMADP	P	TTL	BWB	ODD PARITY FOR SMADxx AND SMAEN	
SMAEN	N	TTL	BWB	ENABLE OF HMH11A →HMH09A	
SMACF	N	TTL	BWB	CELL FRAME OF HMH11A →HMH09A	
SMAEF1	N	TTL	BWB	ERROR FLAG OF HMH11A →HMH09A (PROTECTION AGAINST STACK FOR 0, 26WORD) NG:L, GOOD:H	
SMAEF2	N	TTL	BWB	ERROR FLAG OF HMH11A →HMH09A (PROTECTION AGAINST STACK FOR 0, 26WORD) NG:L, GOOD:H	
SWACTA	—	TTL	BWB	INDICATES ACTIVE SW UNIT (HOME SW ACT(L)/MATE SW ACT(H))	
LPACTA	—	TTL	BWB	INDICATES ACTIVE LP UNIT (HOME LP ACT(L)/MATE LP ACT(H))	
MSTCF	N	TTL	BWB	SYNCHRONIZATION FRAME PULSE FROM ICLP TO OGLP	
SA19CK	CLK	TTL	BWB	HLP02A → ALL LP UNITS 19MHz CLK	
SA19FP	N	TTL	BWB	HLP02A → ALL LP UNITS 19MHz FRAME PULSE	
RQD00 ～07	P	TTL	BWB	HLP07A → ALL LP UNIT 8BIT COMMAND BUS. MSB FOR RQD07, AND LSB FOR RQD00	
REQ	N	TTL	BWB	HLP07A → ALL LP UNITS REQUEST ENABLE	
CK4M	CLK	TTL	BWB	HLP07A → ALL LP UNITS 4MHz CLK	
RSD00～07	P	TTL	BWB	HLP07A ← ALL LP UNIT 8BIT COMMAND BUS. MSB FOR RSD07, AND LSB FOR RSD00	
RES	N	TTL	BWB	HLP07A ← ALL LP UNITS RESPONSE ENABLE	

FIG. 547

6892E0 ET2728O

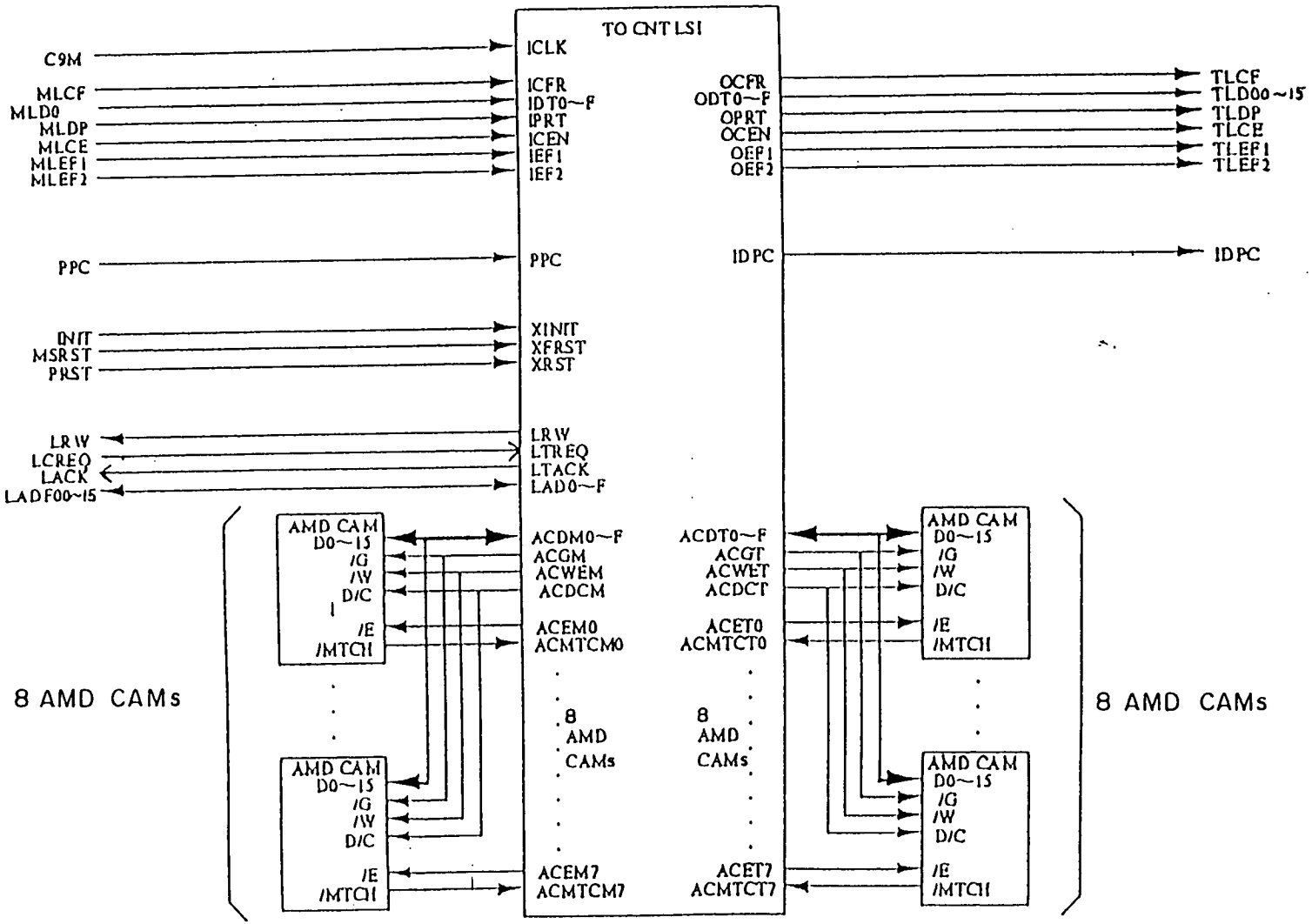


FIG. 548

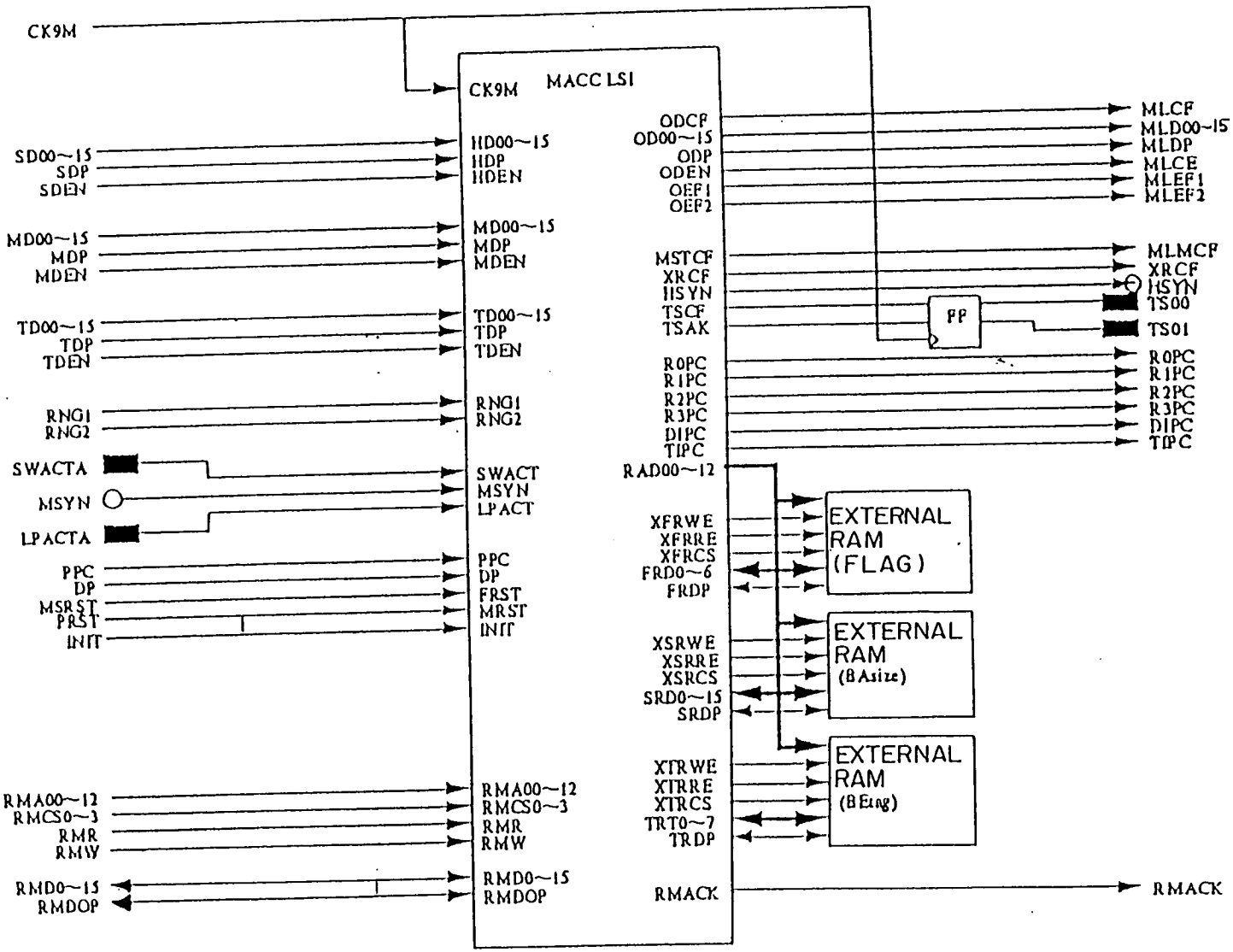

CK9M
CK9M
MACC LSI
SD00~15
SDP
SDEN
HD00~15
HDP
HDEN
MD00~15
MDP
MDEN
TD00~15
TDP
TDEN
RNG1
RNG2
SWACTA
MSYN
LPACTA
SWACT
MSYN
LPACT
PPC
DP
MSRST
PRST
INIT
FRST
MRST
INIT
RMA00~12
RMCS0~3
RMR
RMW
RMD0~15
RMDOP
ODCP
OD00~15
ODP
ODEN
OEF1
OEF2
MSTCP
XRCP
HSYN
TSCP
TSAK
R0PC
R1PC
R2PC
R3PC
DIPC
TIPC
RAD00~12
XFRWE
XFRRE
XFRCS
FRD0~6
FRDP
XSRWE
XSRRE
XSRCS
SRD0~15
SRDP
XTRWE
XTRRE
XTRCS
TRT0~7
TRDP
RMACK
MLCP
MLD00~15
MLDP
MLCE
MLEF1
MLEF2
MLMCP
XRCP
HSYN
TS00
TS01
PP
R0PC
R1PC
R2PC
R3PC
DIPC
TIPC
EXTERNAL RAM (FLAG)
EXTERNAL RAM (BAsize)
EXTERNAL RAM (BEtag)
RMACK

FIG. 549

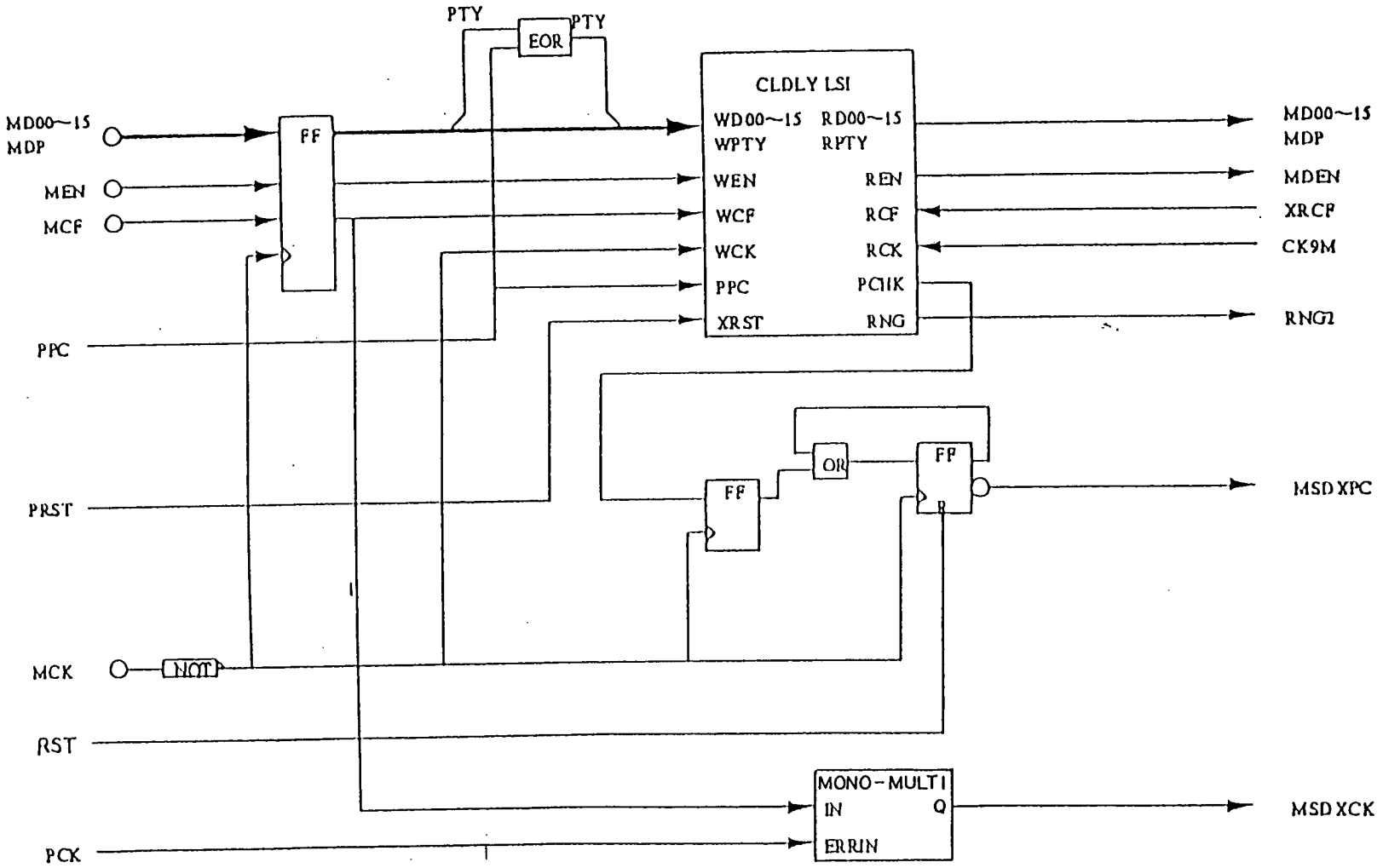

PTY
EOR
PTY
CLDLY LSI
WD00~15
WPTY
RD00~15
RPTY
WEN
REN
WCF
RCF
WCK
RCK
PPC
PCIK
XRST
RNG
MD00~15
MDP
MDEN
XRCF
CK9M
RNG2
MSDXPC
MSDXCK
MD00~15
MDP
MEN
MCF
FF
PPC
PRST
FF
OR
FF
R
MCK
NOT
RST
MONO-MULTI
IN
Q
ERRIN
PCK

FIG. 550

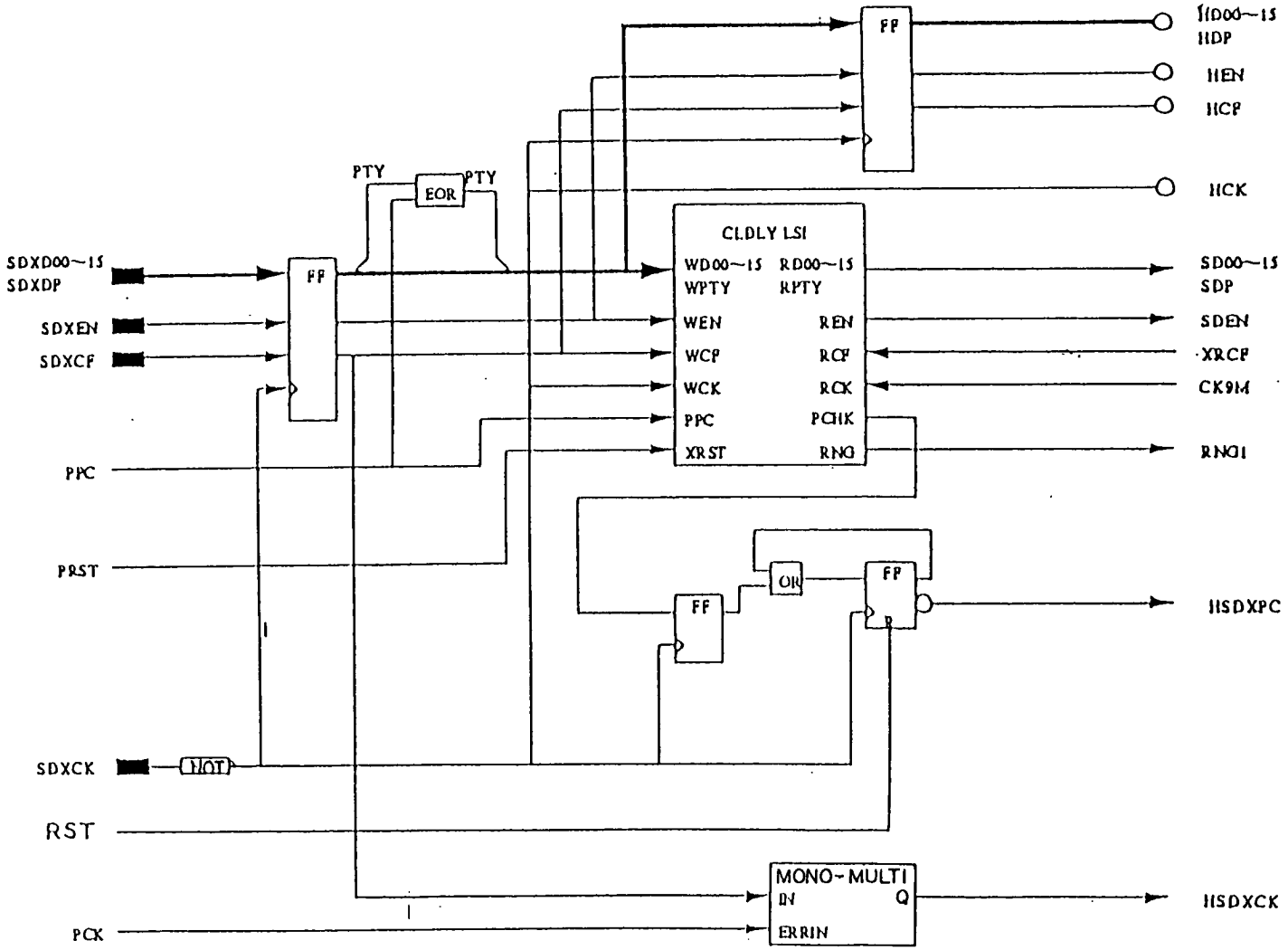

FF
IIDD0~15
IIDP
IIEN
IICP
IICK
PTY
EOR
PTY
CLDLY LSI
WD00~15
WPTY
RD00~15
RPTY
WEN
REN
WCP
RCP
WCK
RCK
PPC
PCIIK
XRST
RNG
SDXD00~15
SDXDP
SDXEN
SDXCF
SD00~15
SDP
SDEN
XRCF
CK9M
RNG1
PPC
PRST
OR
FF
FF
IISDXPC
SDXCK
INOT
RST
MONO-MULTI
IN
Q
ERRIN
IISDXCK
PCK

FIG. 551

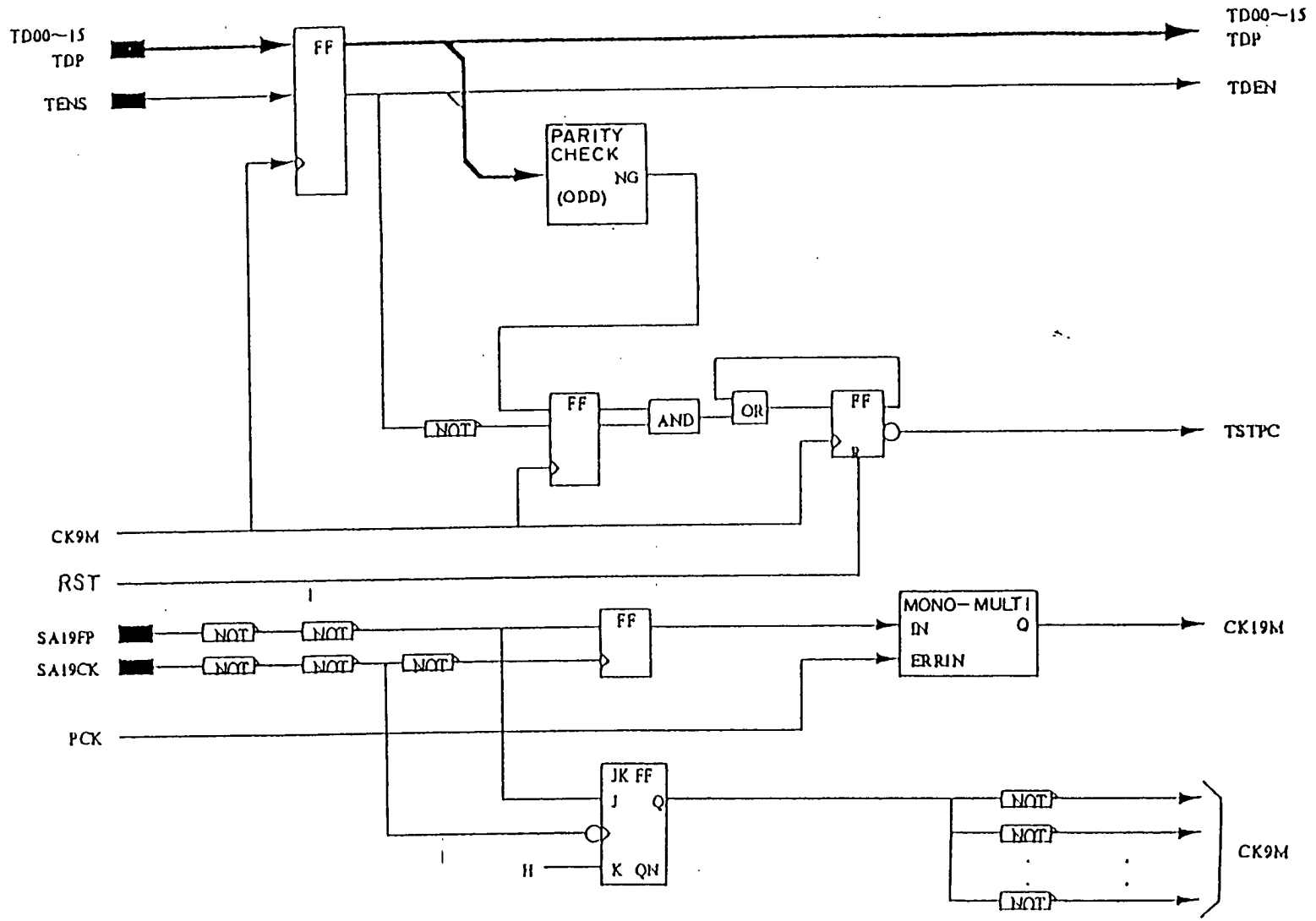

TD00~15
TDP
TENS
FF
TD00~15
TDP
TDEN
PARITY
CHECK
NG
(ODD)
NOT
FF
AND
OR
FF
R
TSTPC
CK9M
RST
SA19FP
SA19CK
NOT
NOT
NOT
NOT
NOT
FF
MONO-MULTI
IN
Q
ERRIN
CK19M
PCK
JK FF
J
Q
K
QN
H
NOT
NOT
NOT
CK9M

FIG. 552

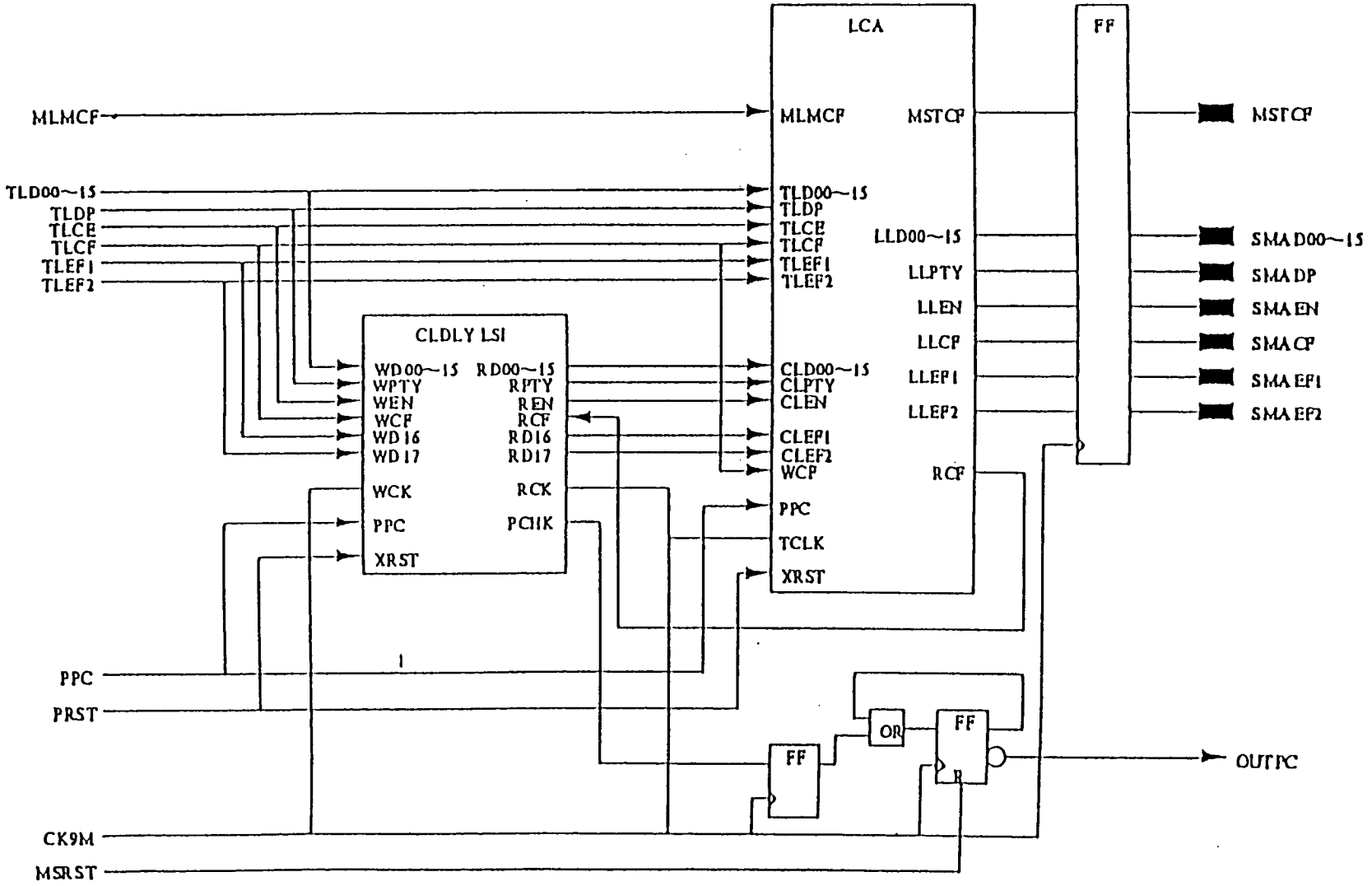
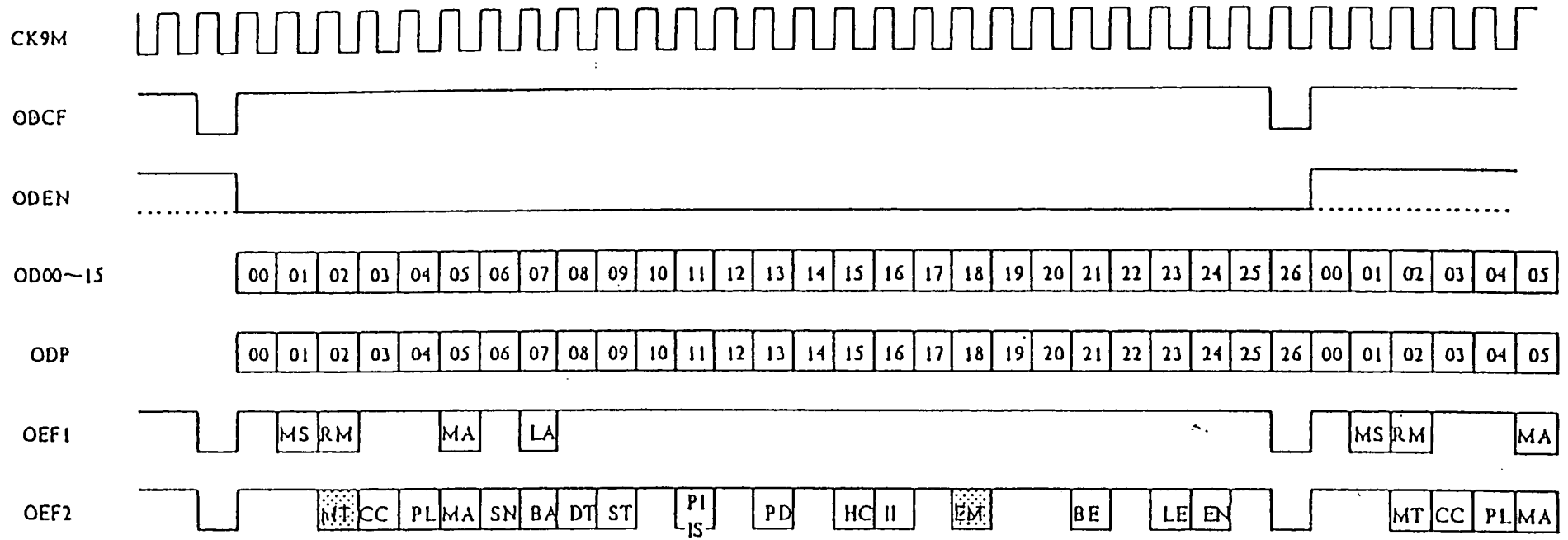

LCA
FF
MLMCP
MSTCP
TLD00~15
TLDP
TLCE
TLCF
TLEF1
TLEF2
LLD00~15
LLPTY
LLEN
LLCP
LLEF1
LLEF2
RCP
CLD00~15
CLPTY
CLEN
CLEF1
CLEF2
WCP
PPC
TCLK
XRST
SMAD00~15
SMADP
SMAEN
SMACP
SMAEF1
SMAEF2
CLDLY LSI
WD00~15
WPTY
WEN
WCP
WD16
WD17
WCK
PPC
XRST
RD00~15
RPTY
REN
RCP
RD16
RD17
RCK
PCLK
PRST
OR
FF
OUTPC
CK9M
MSRST

FIG. 553



[OEF1]

MS : Master ERROR
RM : CCPLNGOR
MA : MID not active (COM)
LA : LINK not active
(ODEN=H:not EN)

[OEF2]

MT : MRI time out
CC : Payload CRC violation
PL : Payload length error
MA : MID currently active or EOM with unapproved MID
SN : Invalid sequence number
BA : Invalid BAsize field value
DT : Invalid DA type
ST : Invalid SA type

[OEF2]

PI : Invalid Protocol ID
(= IS : Invalid Service Type)
PD : Invalid Protocol Descriminator
HC : Hop Count=0
II : Ingress Interface Type
EM : Exceed maximum number of CDU
BE : BEtag mismatch
LE : BAsize field not equal to length field
EN : Encapsulation error (Segment Type = SSM)

NOTE: SHADOWED PORTION AND UNDERLINED FLAGS ARE NOT USED IN MESSAGE CHECK LSI.

FIG. 554

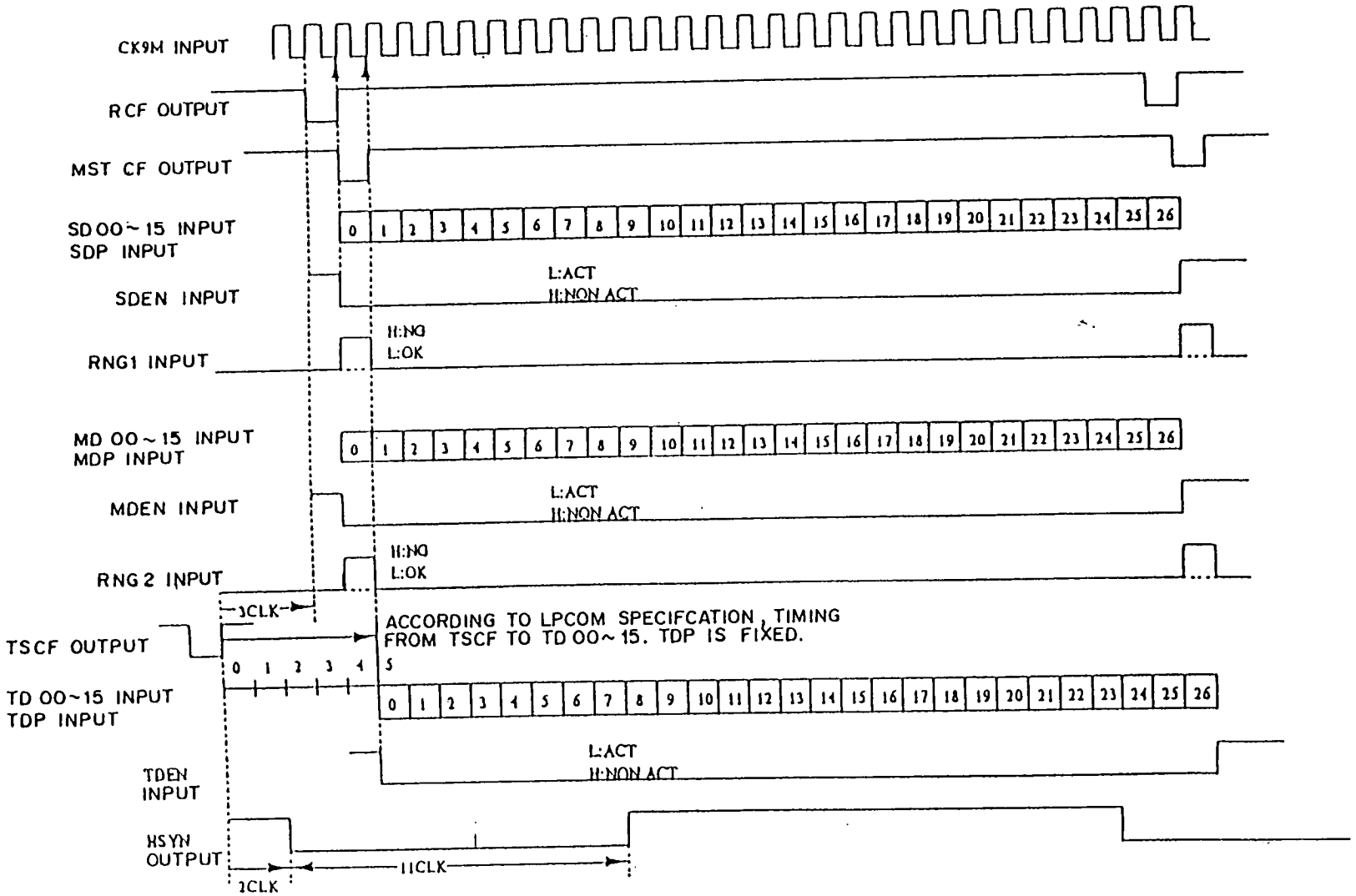

CK9M INPUT
RCF OUTPUT
MST CF OUTPUT
SD 00~15 INPUT
SDP INPUT
SDEN INPUT
L:ACT
H:NON ACT
H:NG
L:OK
RNG1 INPUT
MD 00~15 INPUT
MDP INPUT
MDEN INPUT
L:ACT
H:NON ACT
H:NG
L:OK
RNG2 INPUT
3CLK
ACCORDING TO LPCOM SPECIFCATION, TIMING
FROM TSCF TO TD 00~15. TDP IS FIXED.
TSCF OUTPUT
TD 00~15 INPUT
TDP INPUT
TDEN INPUT
L:ACT
H:NON ACT
HSYN OUTPUT
11CLK
3CLK

FIG. 555

6693E0 "ET2726O

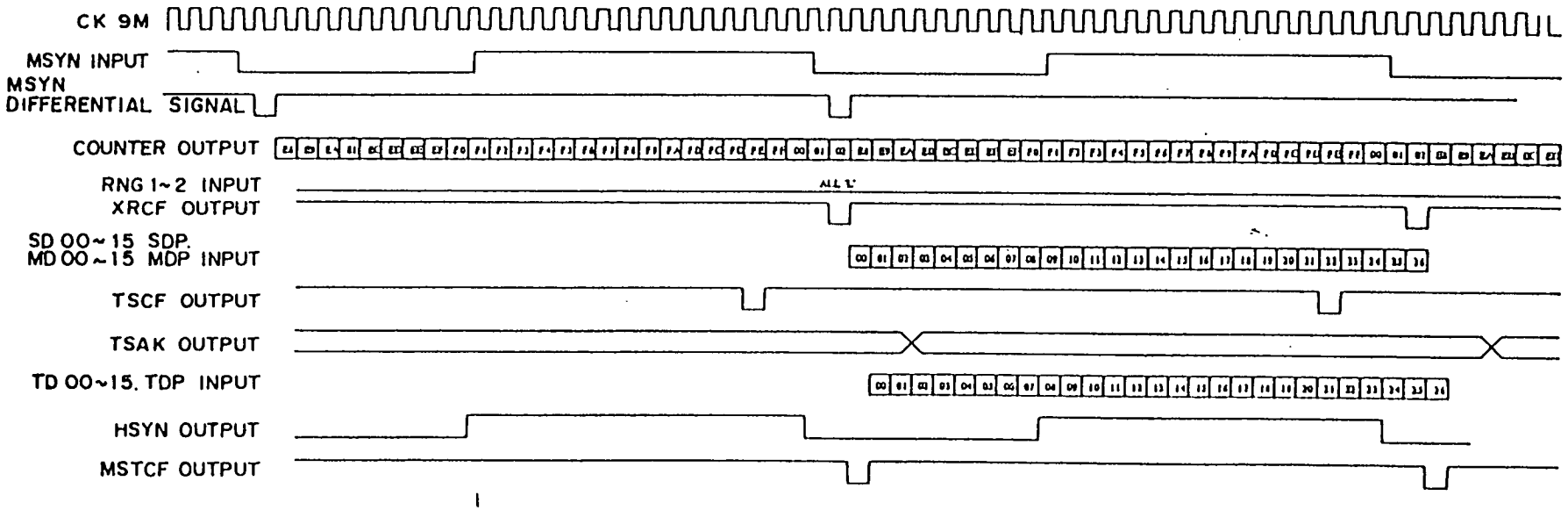


FIG. 556

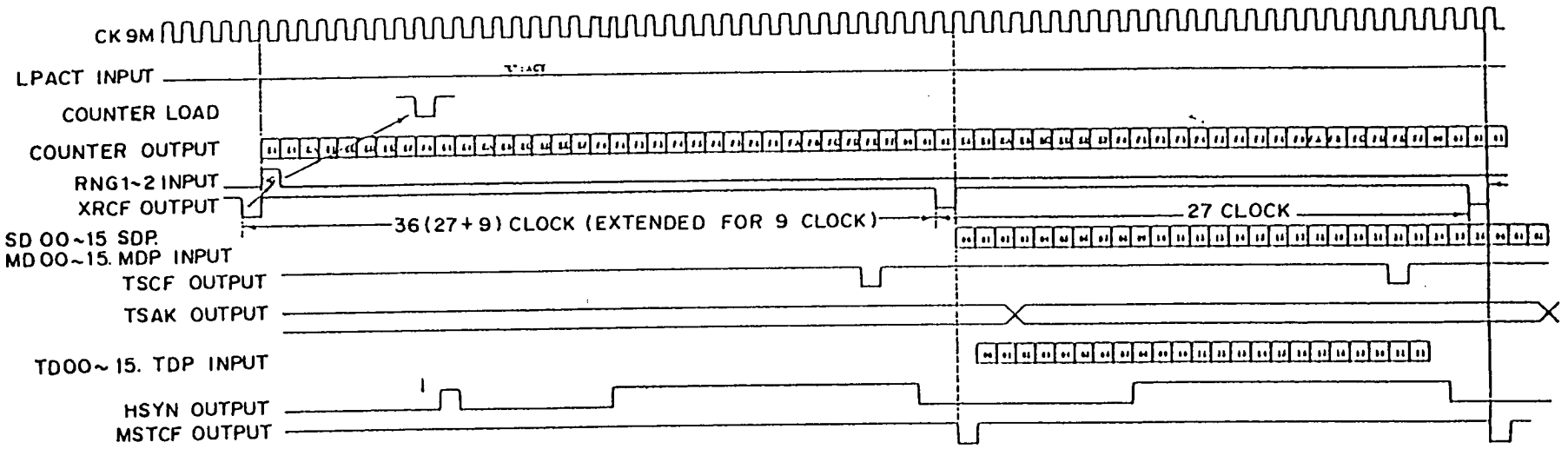

CK 9M
LPACT INPUT
COUNTER LOAD
COUNTER OUTPUT
RNG1~2 INPUT
XRCF OUTPUT
SD 00~15 SDP
MD 00~15 MDP INPUT
TSCF OUTPUT
TSAK OUTPUT
TD00~15 TDP INPUT
HSYN OUTPUT
MSTCF OUTPUT
36 (27+9) CLOCK (EXTENDED FOR 9 CLOCK)
27 CLOCK

FIG. 557

6692E0*ET2Z260

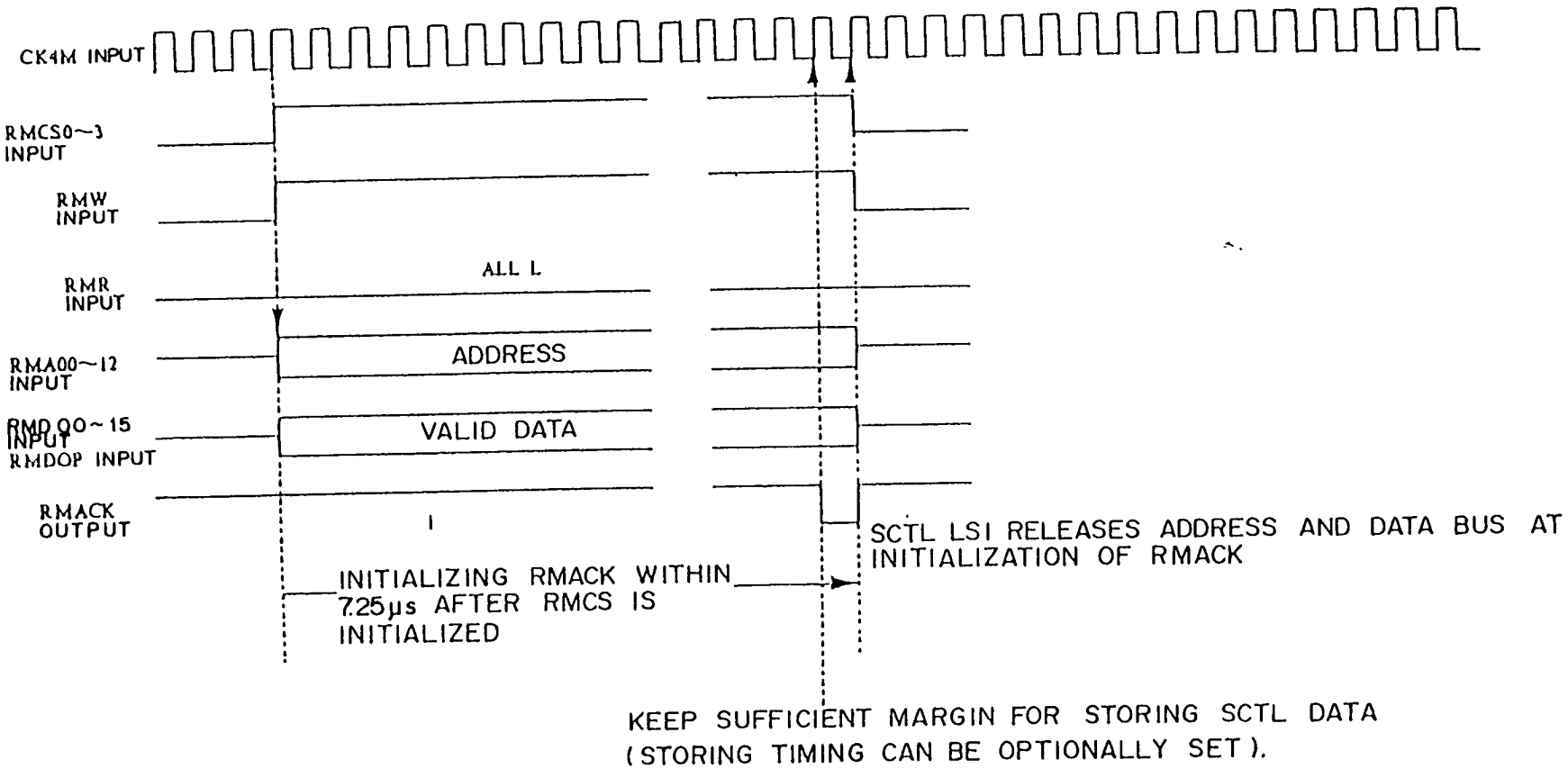


FIG. 558

6692E0 ET27260

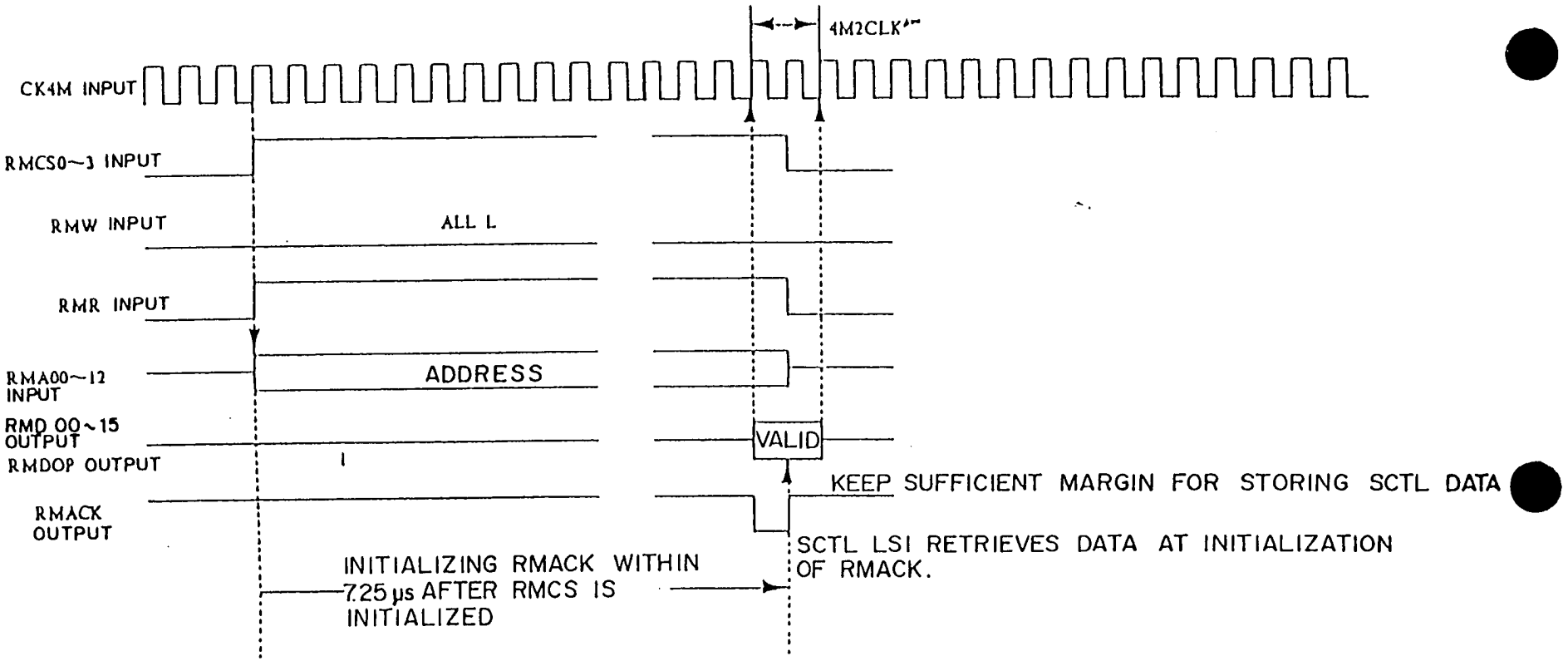


FIG. 559

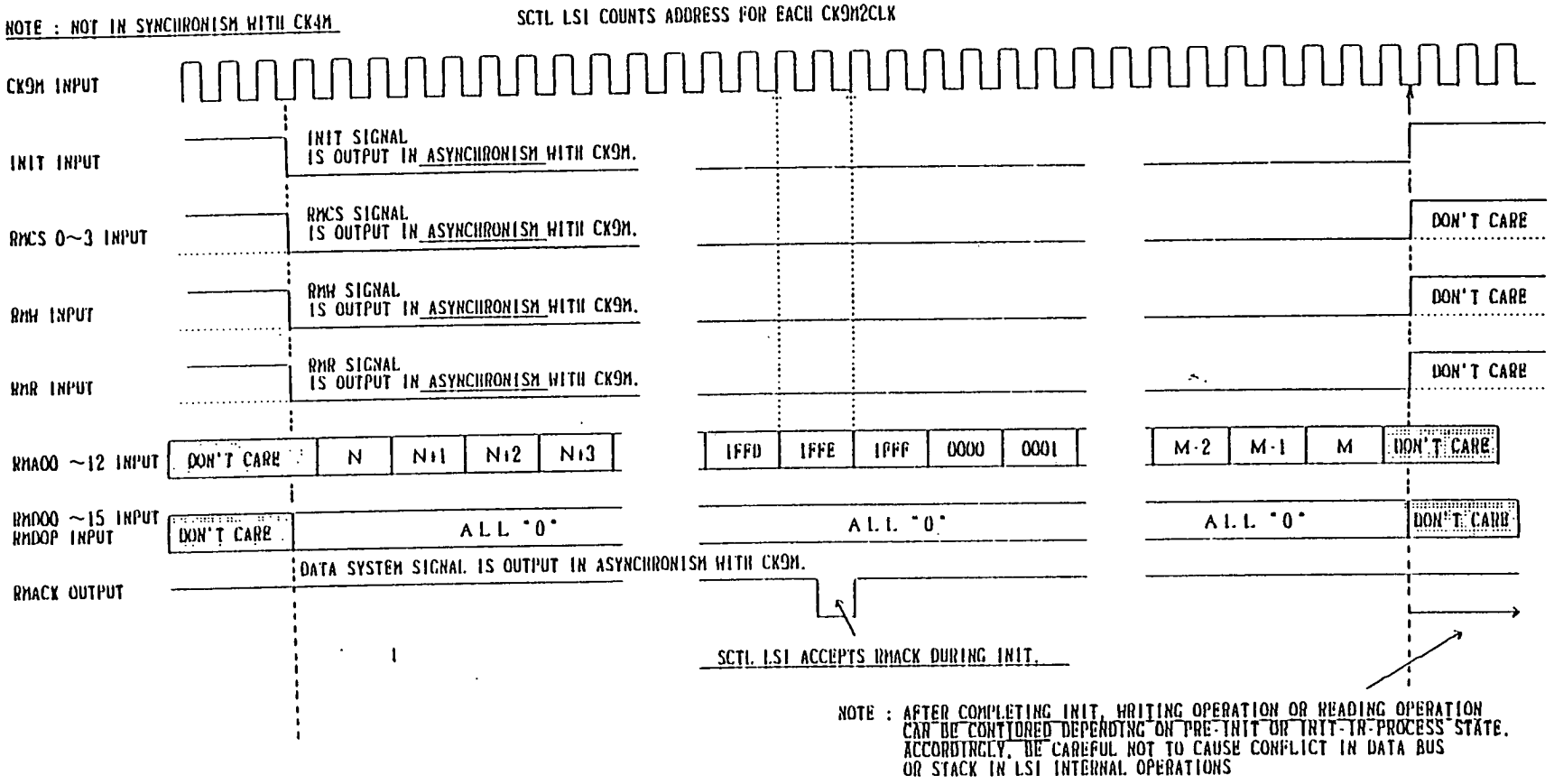

NOTE : NOT IN SYNCHRONISM WITH CK9M
SCTL LSI COUNTS ADDRESS FOR EACH CK9M2CLK
CK9M INPUT
INIT INPUT
INIT SIGNAL IS OUTPUT IN ASYNCHRONISM WITH CK9M.
RMCS 0~3 INPUT
RMCS SIGNAL IS OUTPUT IN ASYNCHRONISM WITH CK9M.
RMW INPUT
RMW SIGNAL IS OUTPUT IN ASYNCHRONISM WITH CK9M.
RMR INPUT
RMR SIGNAL IS OUTPUT IN ASYNCHRONISM WITH CK9M.
RMA00 ~12 INPUT
DON'T CARE
N
N+1
N+2
N+3
1FFD
1FFE
1FFF
0000
0001
M-2
M-1
M
DON'T CARE
RMD00 ~15 INPUT
RMDOP INPUT
DON'T CARE
ALL "0"
ALL "0"
ALL "0"
DON'T CARE
DON'T CARE
DON'T CARE
DON'T CARE
DATA SYSTEM SIGNAL IS OUTPUT IN ASYNCHRONISM WITH CK9M.
RMACK OUTPUT
SCTL LSI ACCEPTS RMACK DURING INIT.
NOTE : AFTER COMPLETING INIT, WRITING OPERATION OR READING OPERATION CAN BE CONTIORED DEPENDING ON PRE-INIT OR INIT-IN-PROCESS STATE. ACCORDINGLY, BE CAREFUL NOT TO CAUSE CONFLICT IN DATA BUS OR STACK IN LSI INTERNAL OPERATIONS

FIG. 560

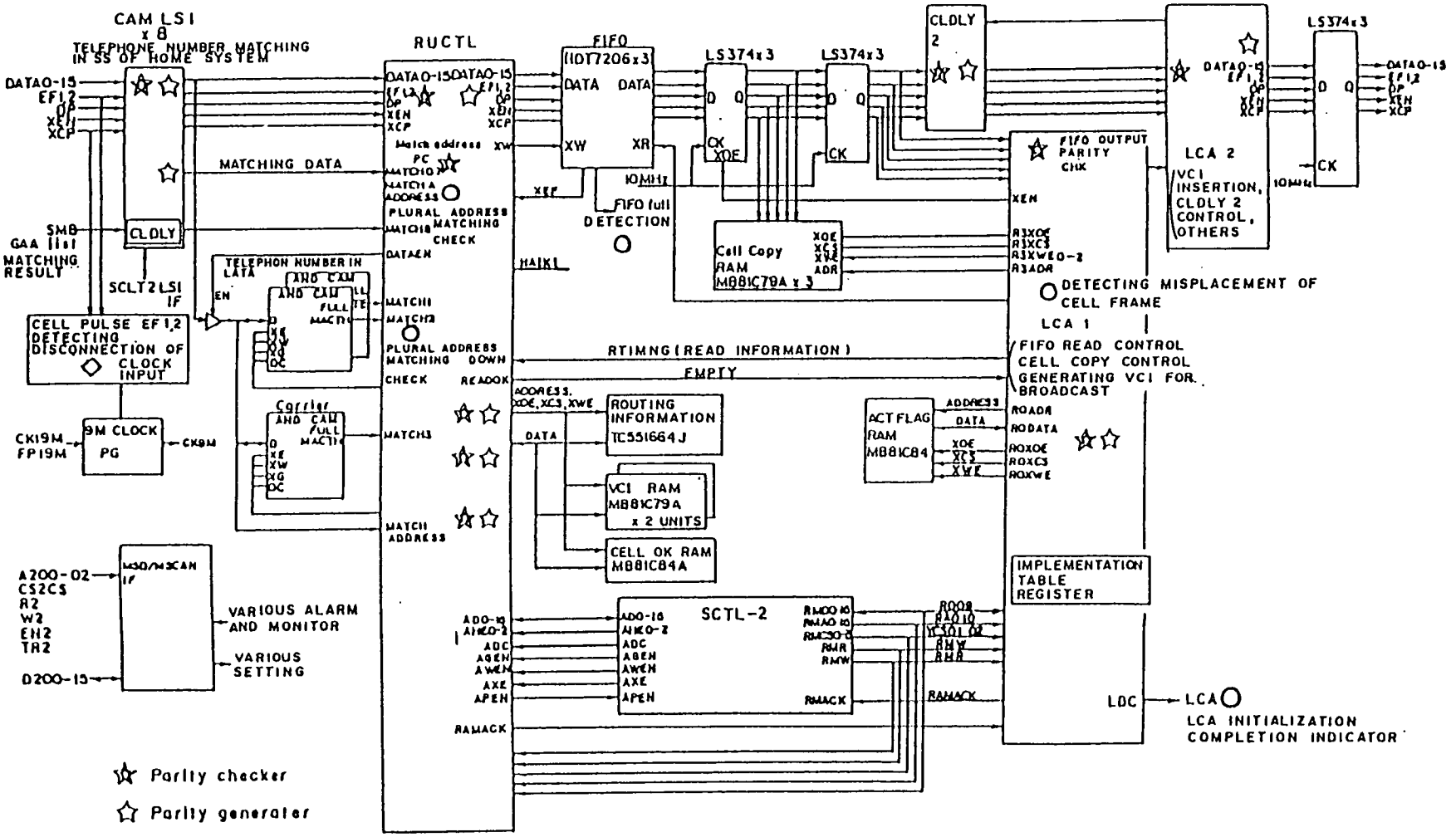

CAM LSI x 8
TELEPHONE NUMBER MATCHING IN SS OF HOME SYSTEM
RUCTL
FIFO
LS374x3
LS374x3
CLDLY 2
LS374x3
DATA0-15
EF1,2
OP
XEN
XCP
MATCHING DATA
SMB
GAA
MATCHING RESULT
CLDLY
SCLT2 LSI IF
CELL PULSE EF1,2 DETECTING DISCONNECTION OF CLOCK INPUT
TELEPHON NUMBER IN LATA
PLURAL ADDRESS MATCHING CHECK
MATCH1
MATCH2
MATCH3
MATCH ADDRESS
Carrier
9M CLOCK PG
CK19M
FP19M
CK9M
10MHz
FIFO full DETECTION
HAIKL
Cell Copy RAM M881C79A x 3
FIFO OUTPUT PARITY CHK
LCA 2
VCI INSERTION, CLDLY 2 CONTROL, OTHERS
DETECTING MISPLACEMENT OF CELL FRAME
LCA 1
FIFO READ CONTROL
CELL COPY CONTROL
GENERATING VCI FOR BROADCAST
RTIMNG (READ INFORMATION)
EMPTY
ROUTING INFORMATION TC5516641J
VCI RAM M881C79A x 2 UNITS
CELL OK RAM M881C84A
ACT FLAG RAM M881C84
IMPLEMENTATION TABLE REGISTER
SCTL-2
A200-02
CS2CS
R2
W2
EN2
TR2
D200-15
VARIOUS ALARM AND MONITOR
VARIOUS SETTING
LDC
LCA
LCA INITIALIZATION COMPLETION INDICATOR
Parity checker
Parity generater
DETECTING DISCONNECTIONS OF CLOCK CELL FRAME
OTHER ALARMS

FIG. 561

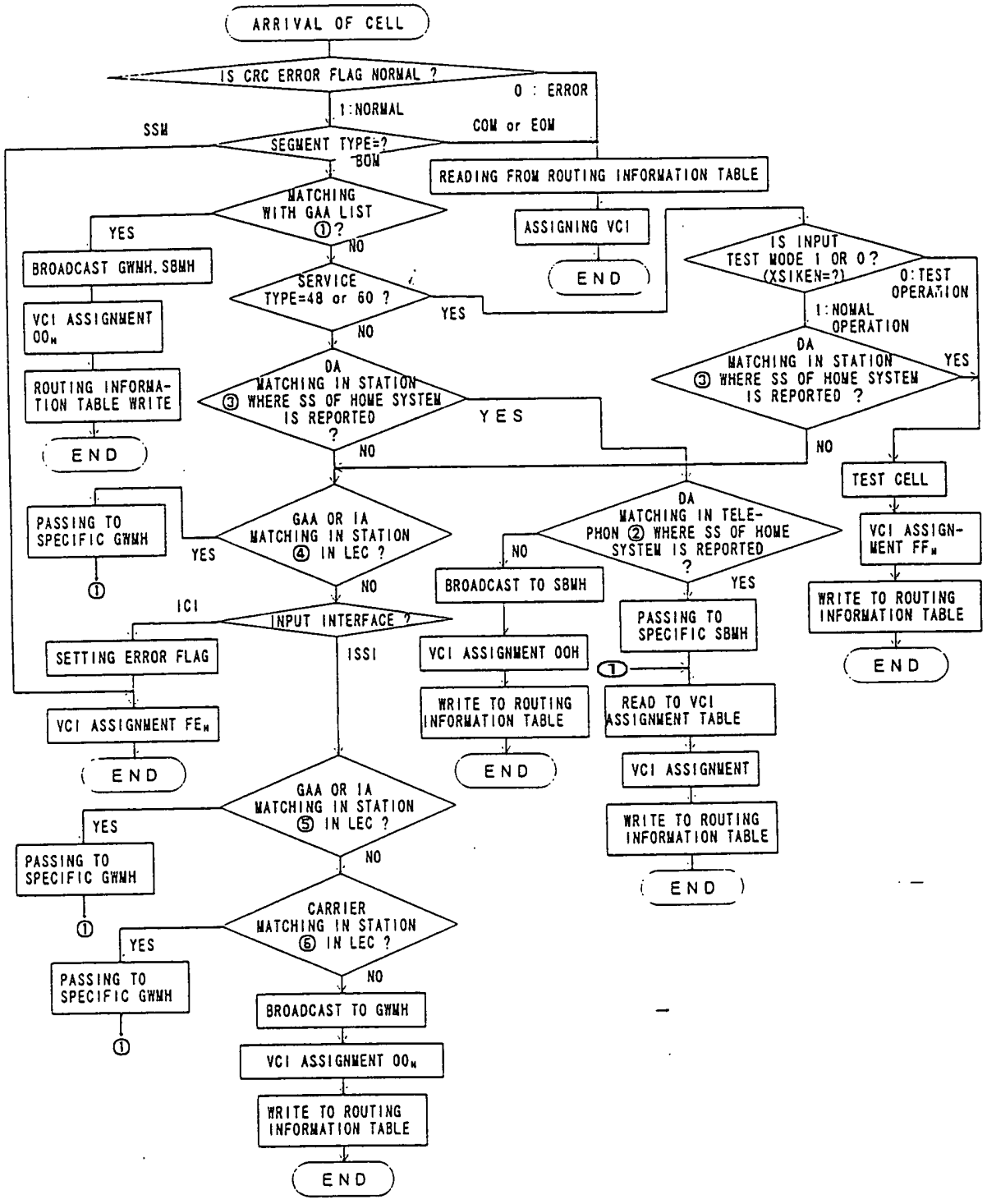
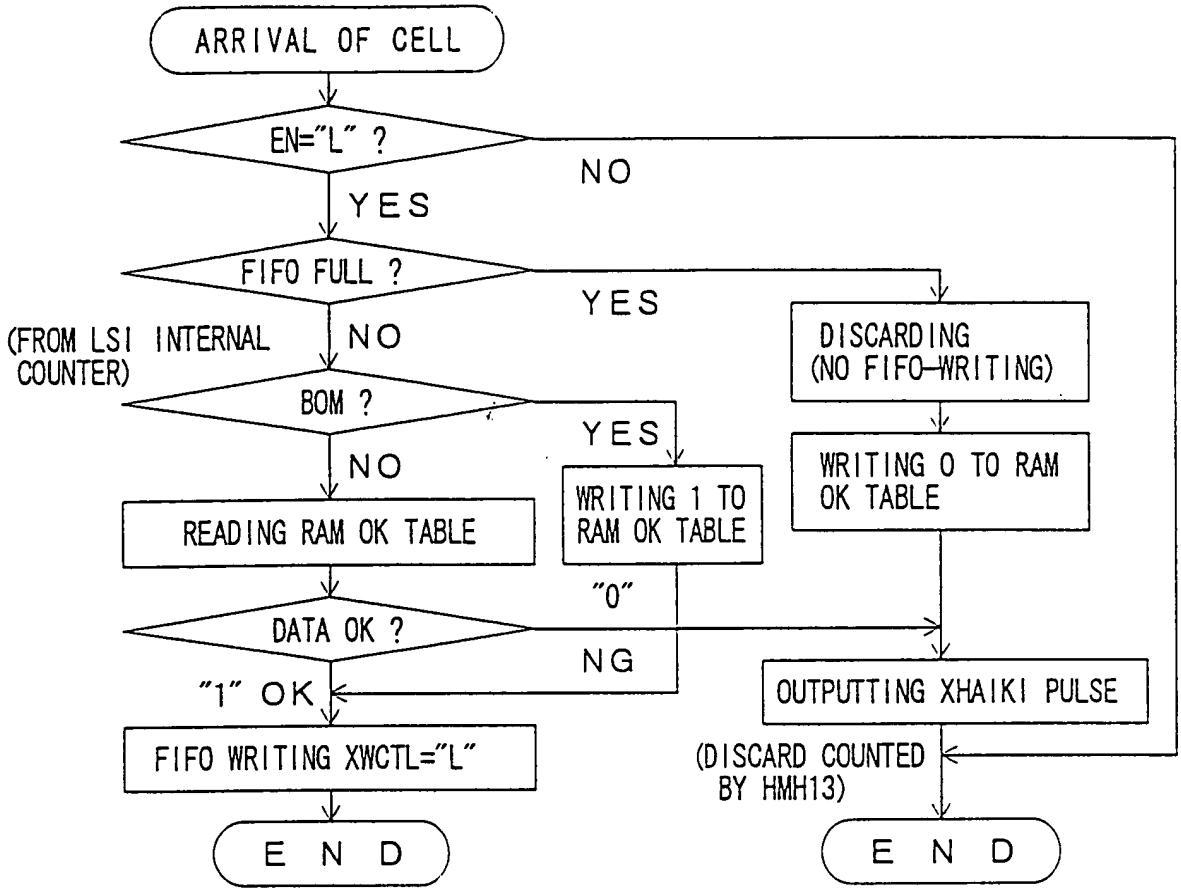

ARRIVAL OF CELL
IS CRC ERROR FLAG NORMAL ?
0 : ERROR
1:NORMAL
SSM
SEGMENT TYPE=?
COM or EOM
BOM
READING FROM ROUTING INFORMATION TABLE
MATCHING WITH GAA LIST ①?
YES
NO
ASSIGNING VCI
END
BROADCAST GWMH, SBMH
SERVICE TYPE=48 or 60 ?
YES
NO
IS INPUT TEST MODE 1 OR 0? (XSIKEN=?)
0:TEST OPERATION
1:NOMAL OPERATION
VCI ASSIGNMENT 00H
DA MATCHING IN STATION ③ WHERE SS OF HOME SYSTEM IS REPORTED ?
YES
ROUTING INFORMATION TABLE WRITE
END
YES
NO
NO
TEST CELL
PASSING TO SPECIFIC GWMH
GAA OR IA MATCHING IN STATION ④ IN LEC ?
YES
DA MATCHING IN TELEPHON ② WHERE SS OF HOME SYSTEM IS REPORTED ?
NO
YES
VCI ASSIGNMENT FFH
①
NO
ICI
INPUT INTERFACE ?
BROADCAST TO SBMH
PASSING TO SPECIFIC SBMH
WRITE TO ROUTING INFORMATION TABLE
SETTING ERROR FLAG
ISSI
VCI ASSIGNMENT 00H
①
END
VCI ASSIGNMENT FEH
WRITE TO ROUTING INFORMATION TABLE
READ TO VCI ASSIGNMENT TABLE
END
END
VCI ASSIGNMENT
GAA OR IA MATCHING IN STATION ⑤ IN LEC ?
YES
WRITE TO ROUTING INFORMATION TABLE
PASSING TO SPECIFIC GWMH
NO
①
END
CARRIER MATCHING IN STATION ⑥ IN LEC ?
YES
PASSING TO SPECIFIC GWMH
NO
①
BROADCAST TO GWMH
VCI ASSIGNMENT 00H
WRITE TO ROUTING INFORMATION TABLE
END

FIG. 562

(1) FLOWCHART OF FIFO WRITING UNIT (REALIZED BY RU CTL LSI)



(1) FLOWCHART OF FIFO READ CLOCK GENERATING UNIT (REALIZED BY BROAD CAST LCA)

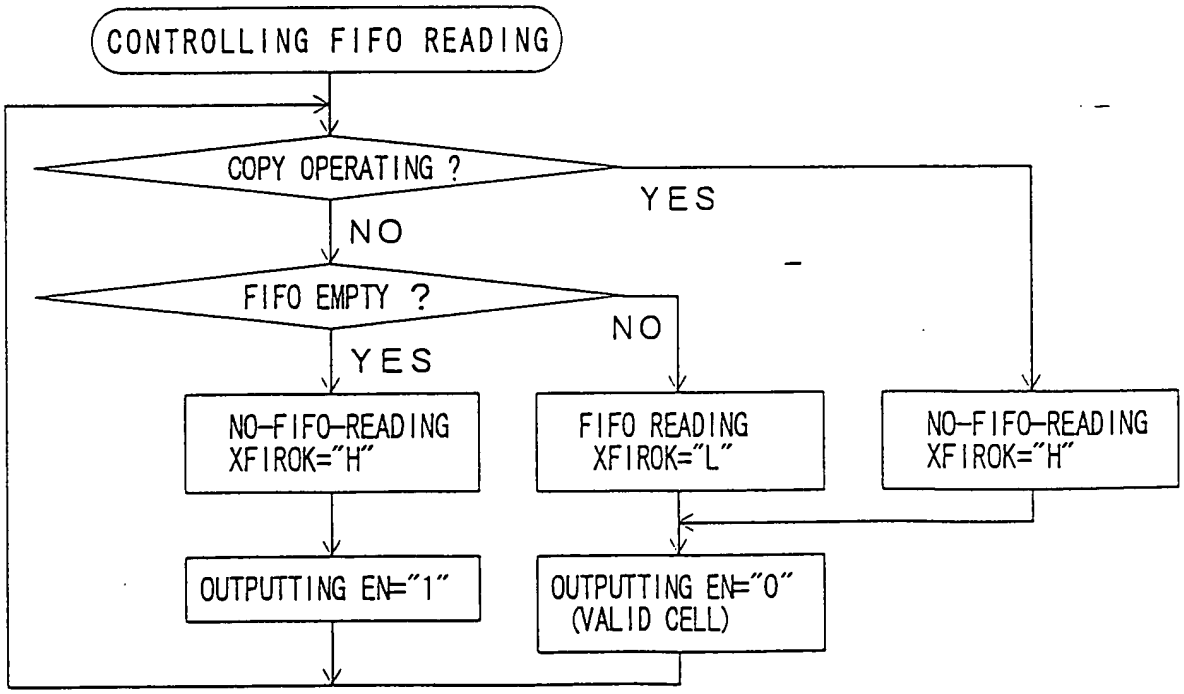


FIG. 563

(3) FLOWCHART OF COPY CONTROL UNIT (REALIZED BY BROADCAST LCA)

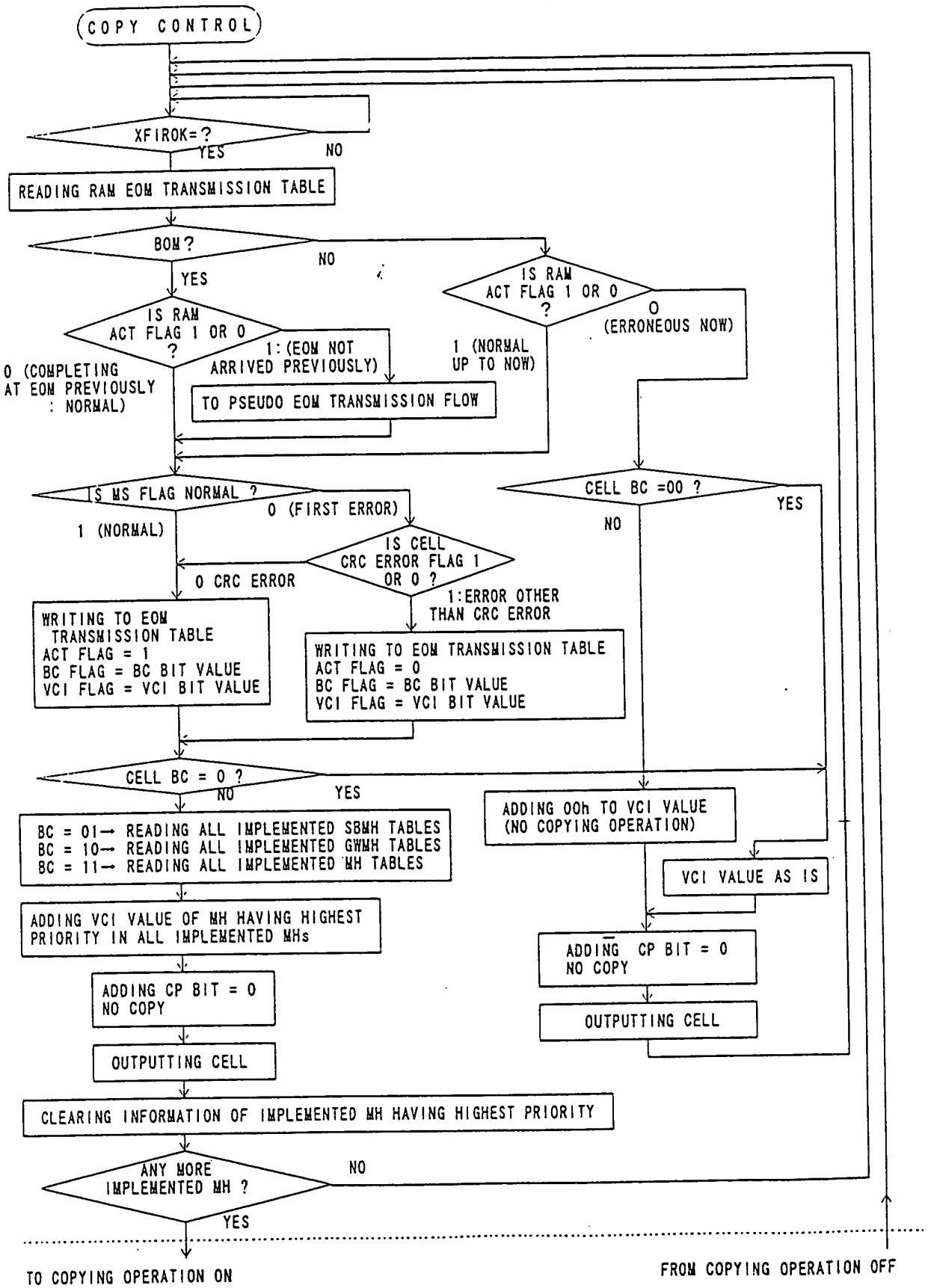


FIG. 564

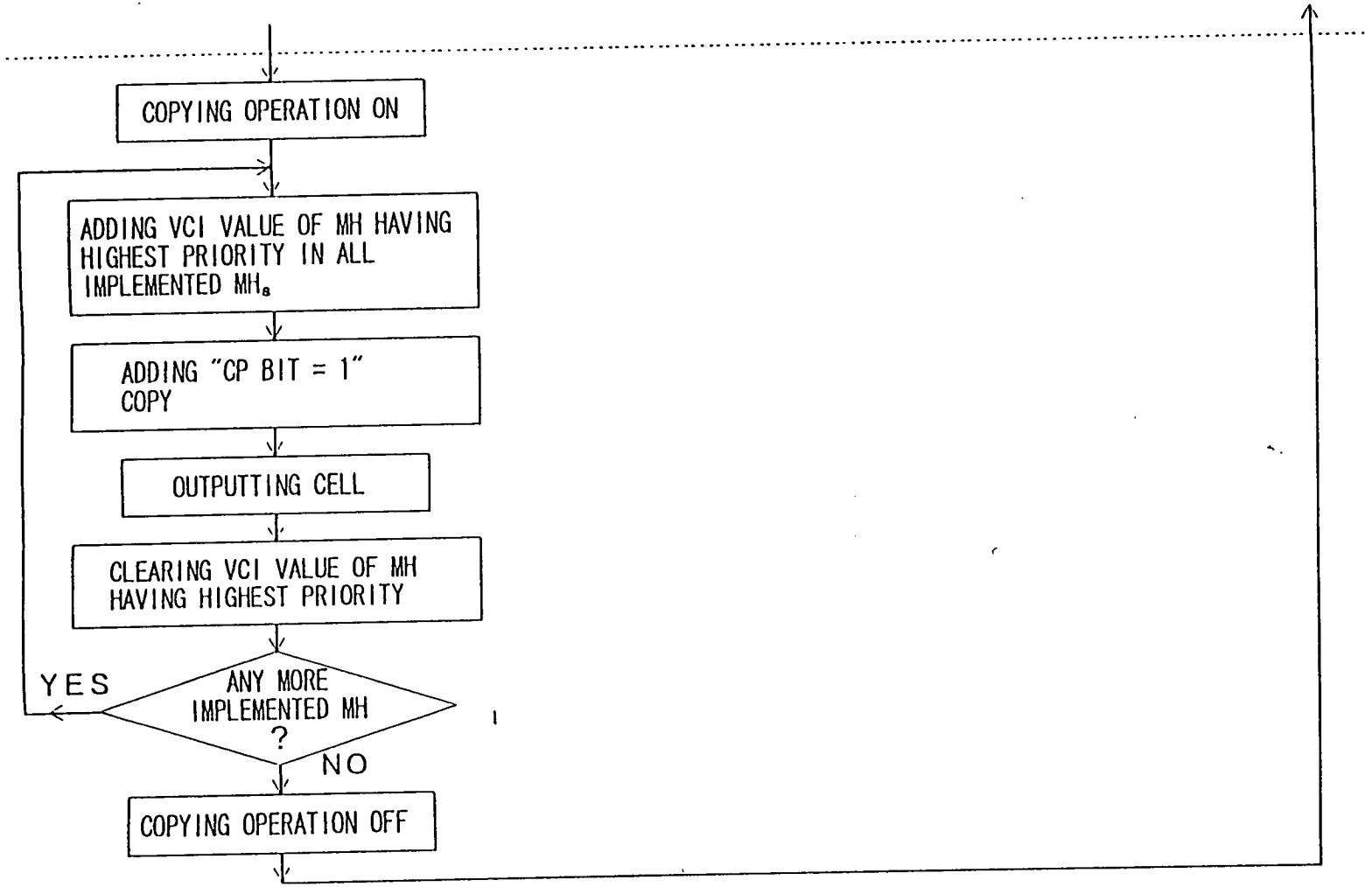
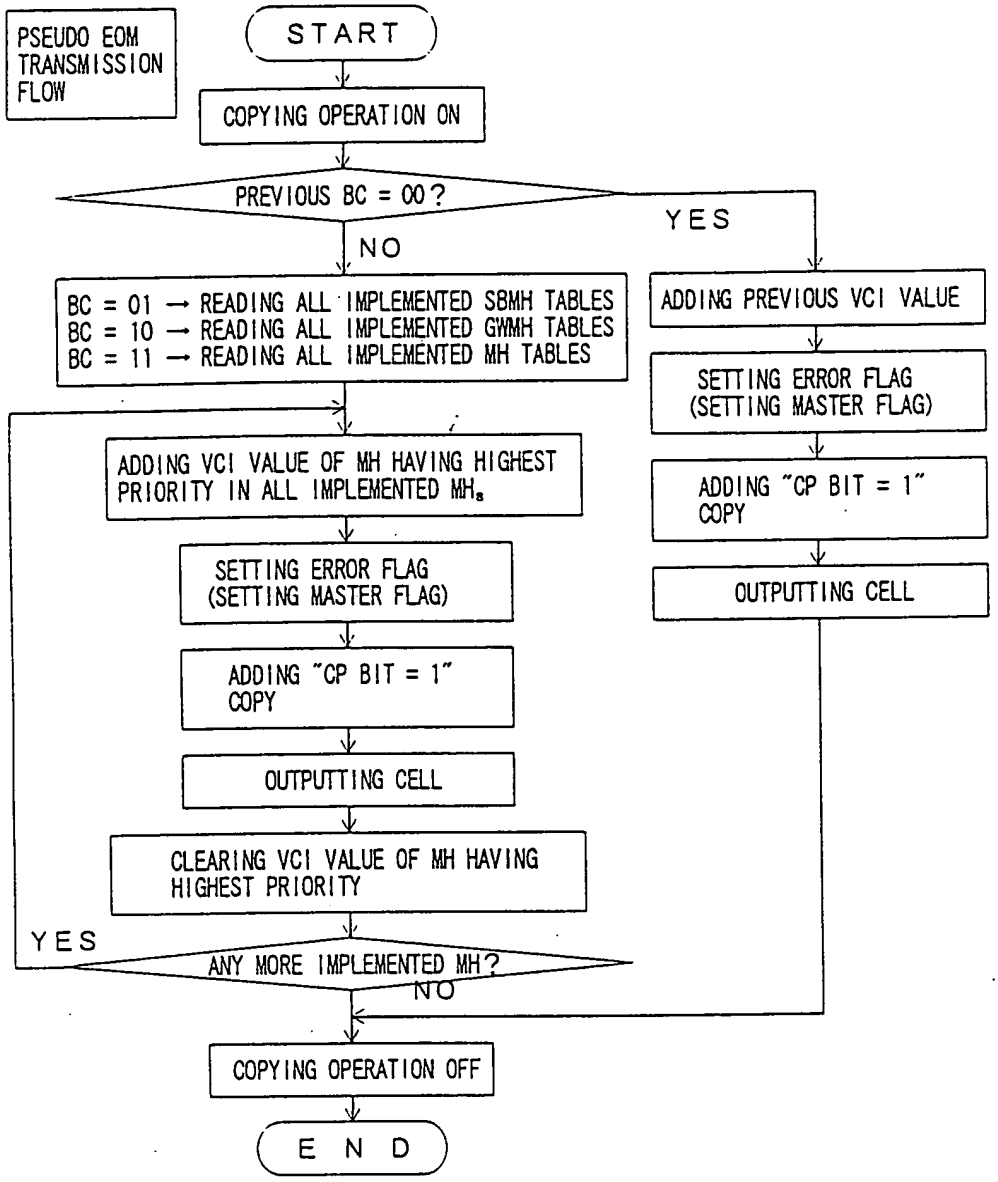

COPYING OPERATION ON
ADDING VCI VALUE OF MH HAVING HIGHEST PRIORITY IN ALL IMPLEMENTED MHs
ADDING "CP BIT = 1" COPY
OUTPUTTING CELL
CLEARING VCI VALUE OF MH HAVING HIGHEST PRIORITY
ANY MORE IMPLEMENTED MH ?
YES
NO
COPYING OPERATION OFF

FIG. 565



	BOM	COM	COM	COM	COM	EOM
EF MS FLAG	OK	OK	NG	—	—	—
RAM ACT TABLE NO ACT	ACT	ACT	ACT	NO ACT	NO ACT	NO ACT
PROCESS	ALL MHs DISTRIBUTED	ALL MHs DISTRIBUTED	ALL MHs DISTRIBUTED	1 MH TRANSMISSION (VCI VALUE 00_H)	1 MH TRANSMISSION (VCI VALUE 00_H)	1 MH TRANSMISSION (VCI VALUE 00_H)

(4) FIFO MONITOR UNIT OPERATION CONDITION (REALIZED BY RU CTL LSI)
- COUNTING UP WITH FIFO WRITE
- COUNTING DOWN WITH FIFO READ
- FIFO FULL OUTPUT WITH COUNT VALUE 511
- FIFO EMPTY OUTPUT WITH COUNT VALUE 0

FIG. 566

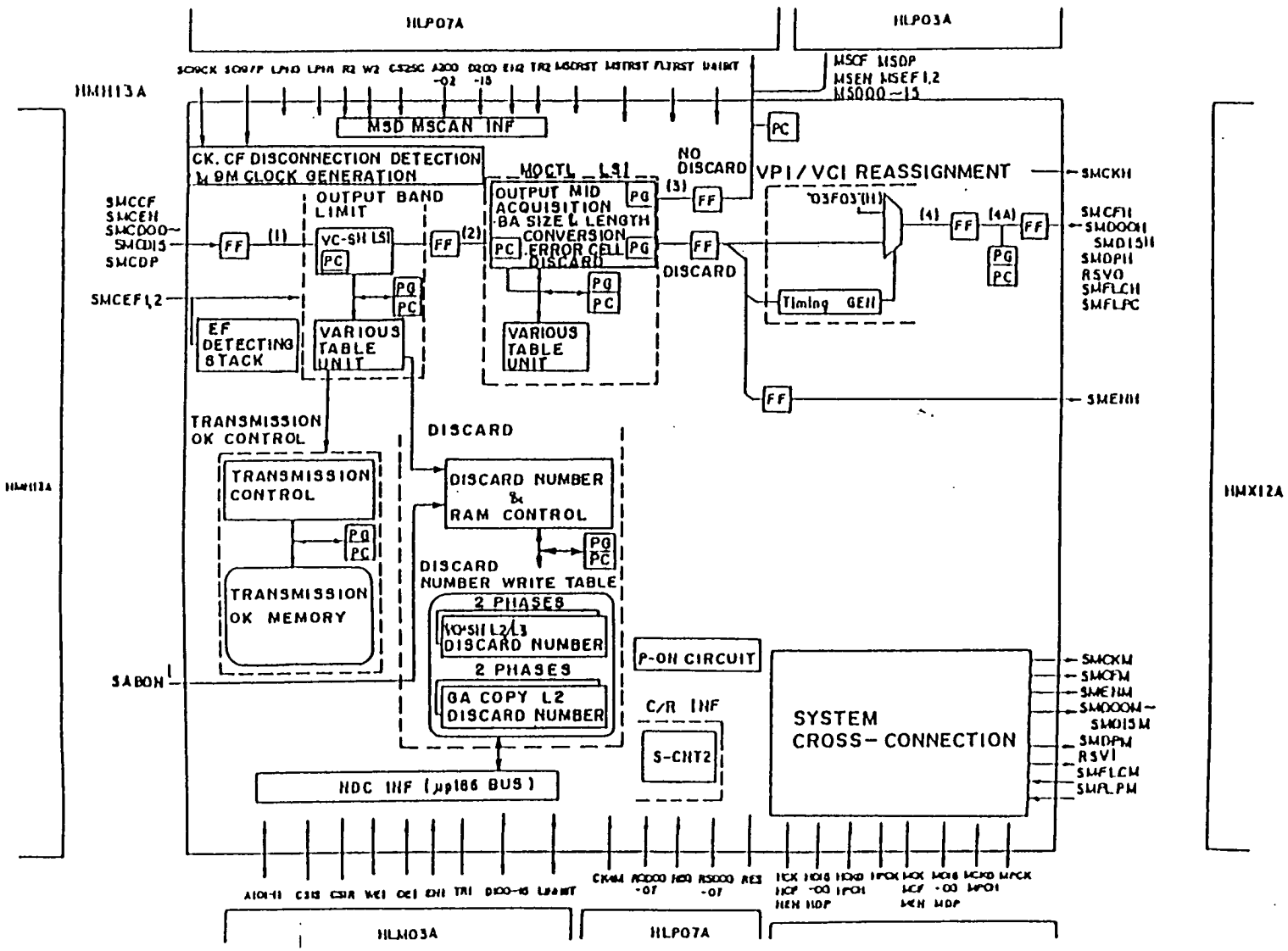

HLP07A
HLP03A
HMH13A
M5D MSCAN INF
CK. CF DISCONNECTION DETECTION & 9M CLOCK GENERATION
MOCTL_L9I
OUTPUT BAND LIMIT
OUTPUT MID ACQUISITION BA SIZE & LENGTH CONVERSION ERROR CELL DISCARD
NO DISCARD
VPI / VCI REASSIGNMENT
VC-SII LSI
EF DETECTING STACK
VARIOUS TABLE UNIT
TRANSMISSION OK CONTROL
TRANSMISSION CONTROL
TRANSMISSION OK MEMORY
DISCARD
DISCARD NUMBER & RAM CONTROL
DISCARD NUMBER WRITE TABLE
2 PHASES
2 PHASES
GA COPY L2 DISCARD NUMBER
P-ON CIRCUIT
C/R INF
S-CNT2
SYSTEM CROSS-CONNECTION
NDC INF (μp186 BUS)
Timing GEN
HMX12A
HLM03A
HLP07A

FIG. 567

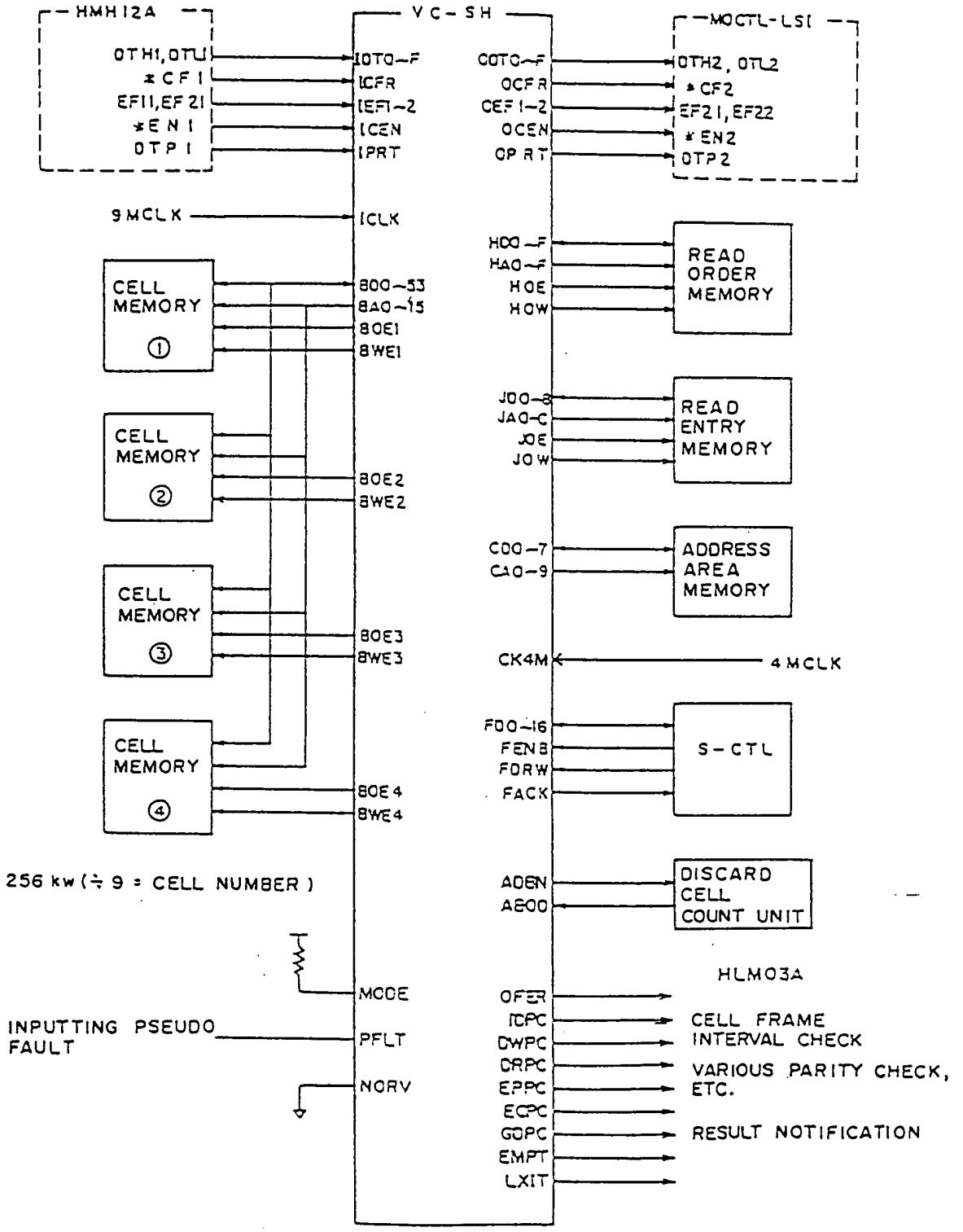

HMH12A
OTH1, OTL1
*CF1
EF11, EF21
*EN1
OTP1
VC-SH
IOTO-F
ICFR
IEF1-2
ICEN
IPRT
ICLK
COTO-F
OCFR
OEF1-2
OCEN
OPRT
MOCTL-LSI
OTH2, OTL2
*CF2
EF21, EF22
*EN2
OTP2
9MCLK
CELL MEMORY ①
CELL MEMORY ②
CELL MEMORY ③
CELL MEMORY ④
B00-33
BA0-15
B0E1
BWE1
B0E2
BWE2
B0E3
BWE3
B0E4
BWE4
256 kw (÷ 9 = CELL NUMBER)
MODE
INPUTTING PSEUDO FAULT
PFLT
NORV
H00-F
HA0-F
HOE
HOW
READ ORDER MEMORY
J00-3
JA0-C
JOE
JOW
READ ENTRY MEMORY
C00-7
CA0-9
ADDRESS AREA MEMORY
CK4M
4MCLK
F00-16
FENB
FORW
FACK
S-CTL
A0EN
A600
DISCARD CELL COUNT UNIT
HLM03A
OFER
IDPC
DWPC
DRPC
EPPC
ECPC
GDPC
EMPT
LXIT
CELL FRAME INTERVAL CHECK
VARIOUS PARITY CHECK, ETC.
RESULT NOTIFICATION

FIG. 568

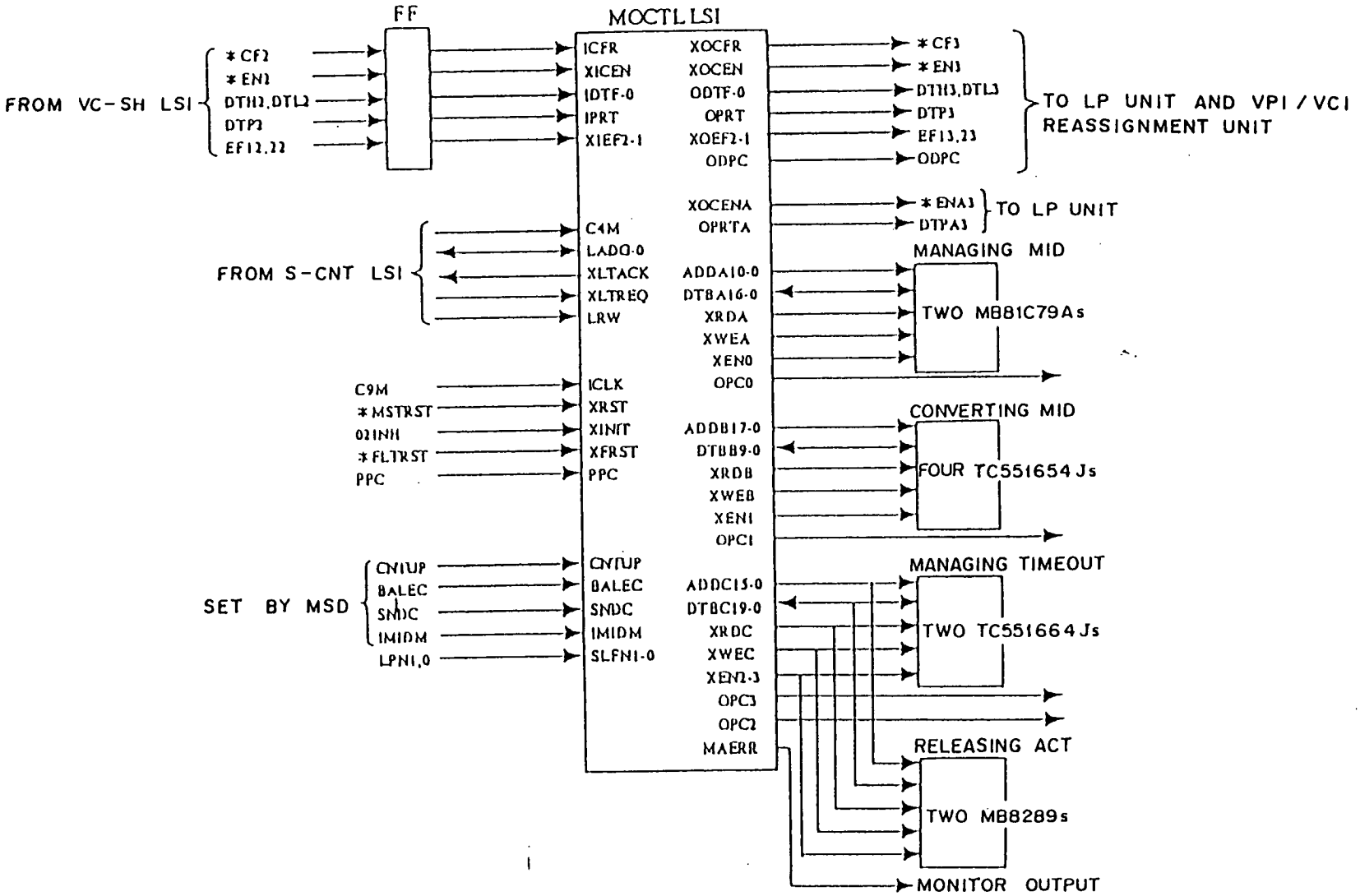
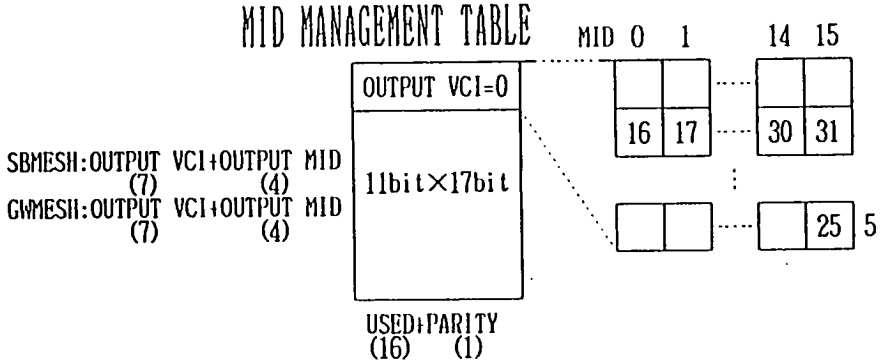

FF
MOCTL LSI
FROM VC-SH LSI
*CF2
*EN2
DTH2,DTL2
DTP2
EF12,22
ICFR
XICEN
IDTF-0
IPRT
XIEF2-1
XOCFR
XOCEN
ODTF-0
OPRT
XOEF2-1
ODPC
*CF3
*EN3
DTH3,DTL3
DTP3
EF13,23
ODPC
TO LP UNIT AND VPI / VCI REASSIGNMENT UNIT
XOCENA
OPRTA
*ENA3
DTPA3
TO LP UNIT
FROM S-CNT LSI
C4M
LADO-0
XLTACK
XLTREQ
LRW
ADDA10-0
DTBA16-0
XRDA
XWEA
XEN0
OPC0
MANAGING MID
TWO MB81C79As
C9M
*MSTRST
02INH
*FLTRST
PPC
ICLK
XRST
XINIT
XFRST
PPC
ADDB17-0
DTBB9-0
XRDB
XWEB
XEN1
OPC1
CONVERTING MID
FOUR TC551654Js
SET BY MSD
CNTUP
BALEC
SNDC
IMIDM
LPN1,0
CNTUP
BALEC
SNDC
IMIDM
SLFN1-0
ADDC15-0
DTBC19-0
XRDC
XWEC
XEN2-3
OPC3
OPC2
MAERR
MANAGING TIMEOUT
TWO TC551664Js
RELEASING ACT
TWO MB8289s
MONITOR OUTPUT

FIG. 569

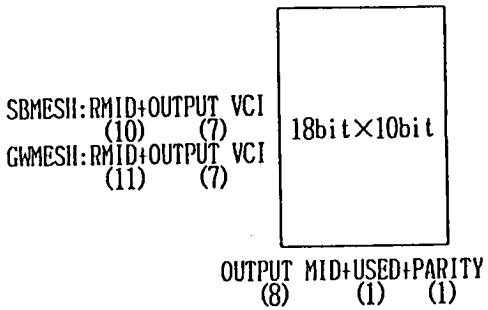
MOCTL LSI USE TABLE

MID MANAGEMENT TABLE



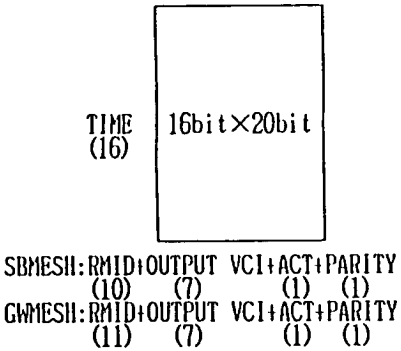
MIDs ARE MANAGED FOR EACH OUTPUT ACCORDING TO THIS TABLE.

MIE CONVERSION TABLE



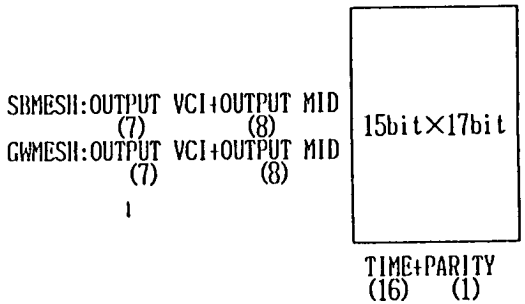
MID IS ACQUIRED FOR EACH PACKET AT BOM AND ENTERED IN THIS TABLE TO USE MID IN CONVERTING MID OF COM AND EOM.

TURNOUT MANAGEMENT TABLE



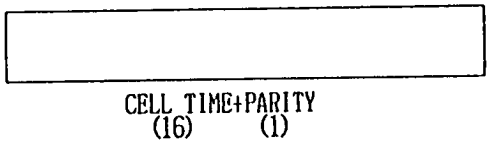
CELL TIMEOUT IS MANAGED FOR EACH PACKET ACCORDING TO THIS TABLE (64 CELLS FROM BOM TO EOM).

ACT RELEASE TABLE



WHEN EOM ARRIVES, THIS TABLE IS USED TO RELEASE ACT SIGNAL OF TIMEOUT MANAGEMENT TABLE.

TIMEOUT CYCLE TABLE



TIMEOUT CYCLE IS SET. (CURRENT TIME IS ADDED TO VALUE OF THIS TABLE TO OBTAIN TIMEOUT VALUE).

FIG. 570

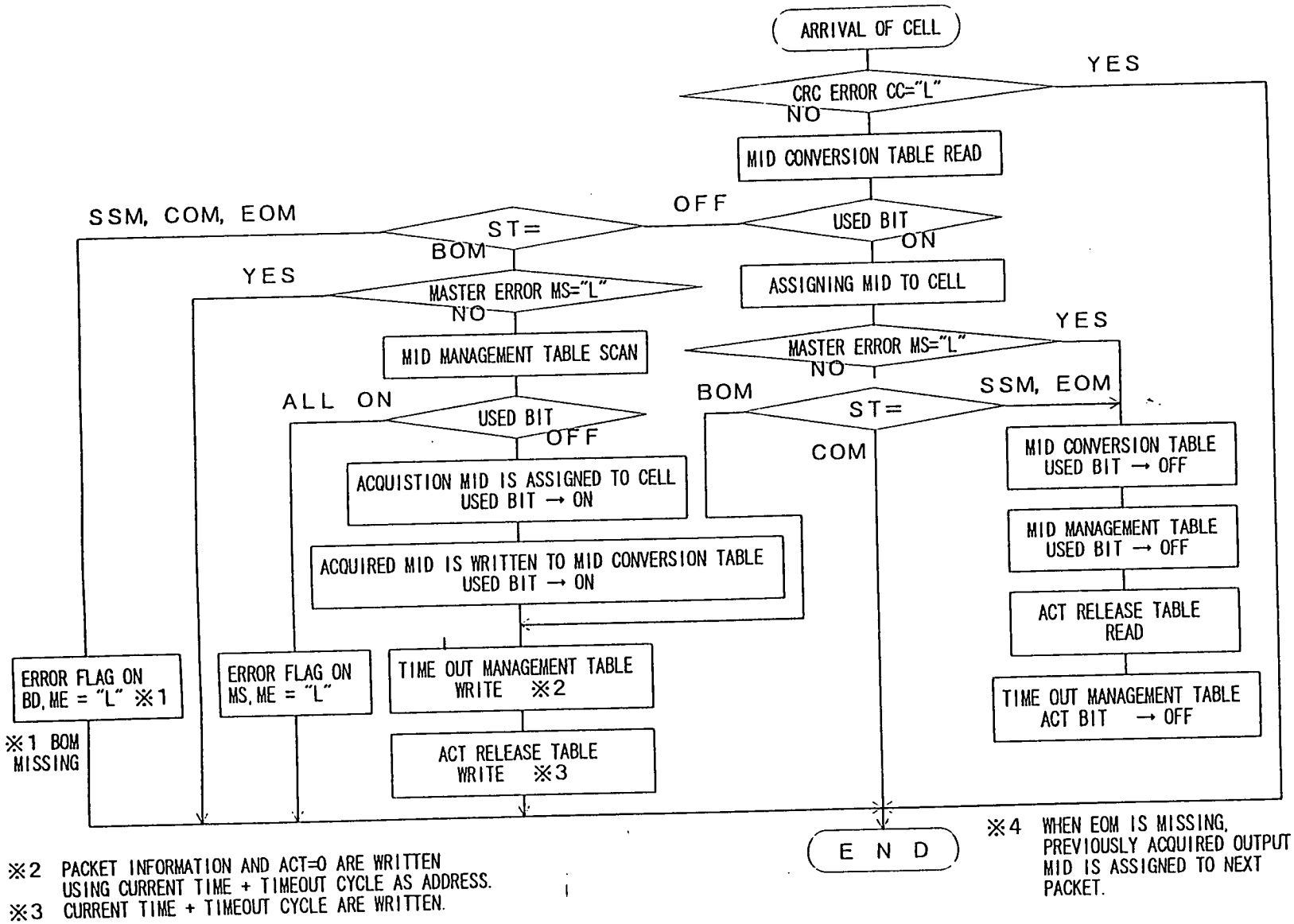
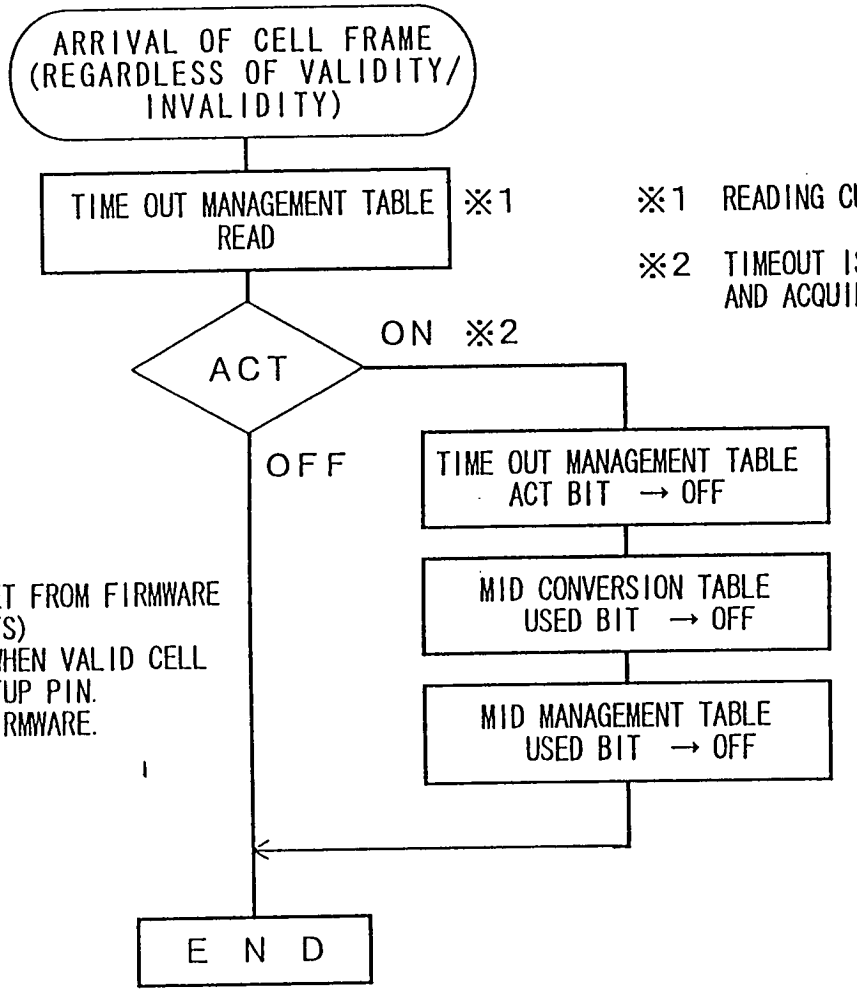

ARRIVAL OF CELL
CRC ERROR CC="L"
YES
NO
MID CONVERSION TABLE READ
USED BIT
OFF
ON
ASSIGNING MID TO CELL
MASTER ERROR MS="L"
YES
NO
ST=
BOM
SSM, EOM
COM
SSM, COM, EOM
YES
MASTER ERROR MS="L"
NO
MID MANAGEMENT TABLE SCAN
ALL ON
USED BIT
OFF
ACQUISTION MID IS ASSIGNED TO CELL
USED BIT → ON
ACQUIRED MID IS WRITTEN TO MID CONVERSION TABLE
USED BIT → ON
MID CONVERSION TABLE
USED BIT → OFF
MID MANAGEMENT TABLE
USED BIT → OFF
ACT RELEASE TABLE
READ
TIME OUT MANAGEMENT TABLE
ACT BIT → OFF
ERROR FLAG ON
BD, ME = "L" ※1
ERROR FLAG ON
MS, ME = "L"
TIME OUT MANAGEMENT TABLE
WRITE ※2
ACT RELEASE TABLE
WRITE ※3
※1 BOM
MISSING
E N D
※2 PACKET INFORMATION AND ACT=0 ARE WRITTEN
USING CURRENT TIME + TIMEOUT CYCLE AS ADDRESS.
※3 CURRENT TIME + TIMEOUT CYCLE ARE WRITTEN.
※4 WHEN EOM IS MISSING,
PREVIOUSLY ACQUIRED OUTPUT
MID IS ASSIGNED TO NEXT
PACKET.

FIG. 571



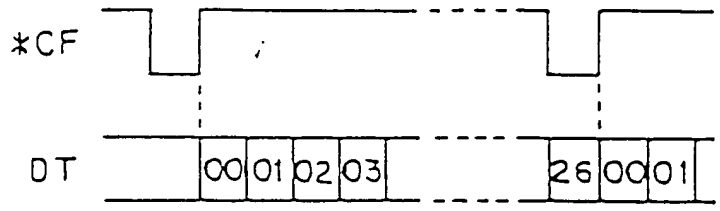
※1 READING CURRENT TIME AS ADDRESS

※2 TIMEOUT IS DETERMINED IF ACT BIT IS ON, AND ACQUIRED MID IS RELEASED.

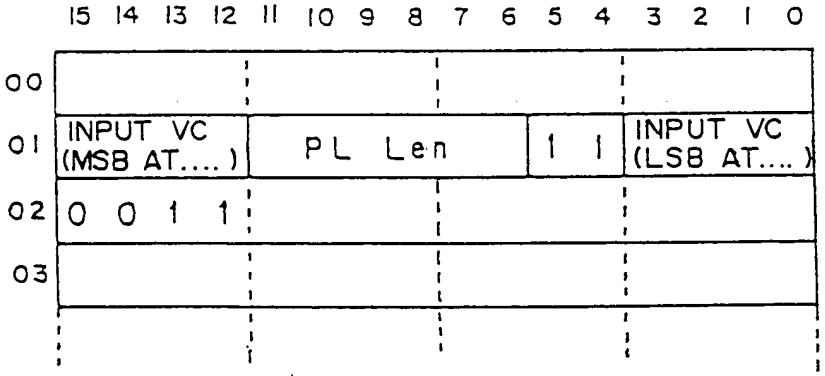
- TIMEOUT CYCLE TABLE IS SET FROM FIRMWARE AT INITIALIZATION (16 BITS)
- CLOCK CAN BE COUNTED UP WHEN VALID CELL IS ENTERED BY SETTING CNTUP PIN.
- CLOCK CAN BE READ FROM FIRMWARE.

FIG. 572

VPI / VCI REASSIGNMENT



HMH12A→HMH13A INPUT CELL FORMAT



HMH13A OUTPUT CELL FORMAT

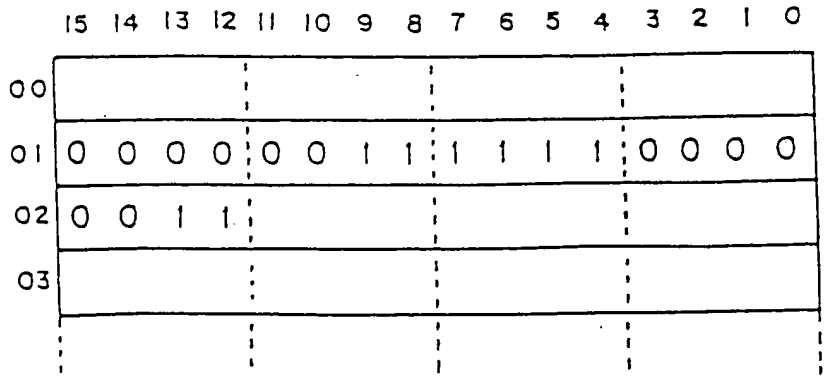


FIG. 573

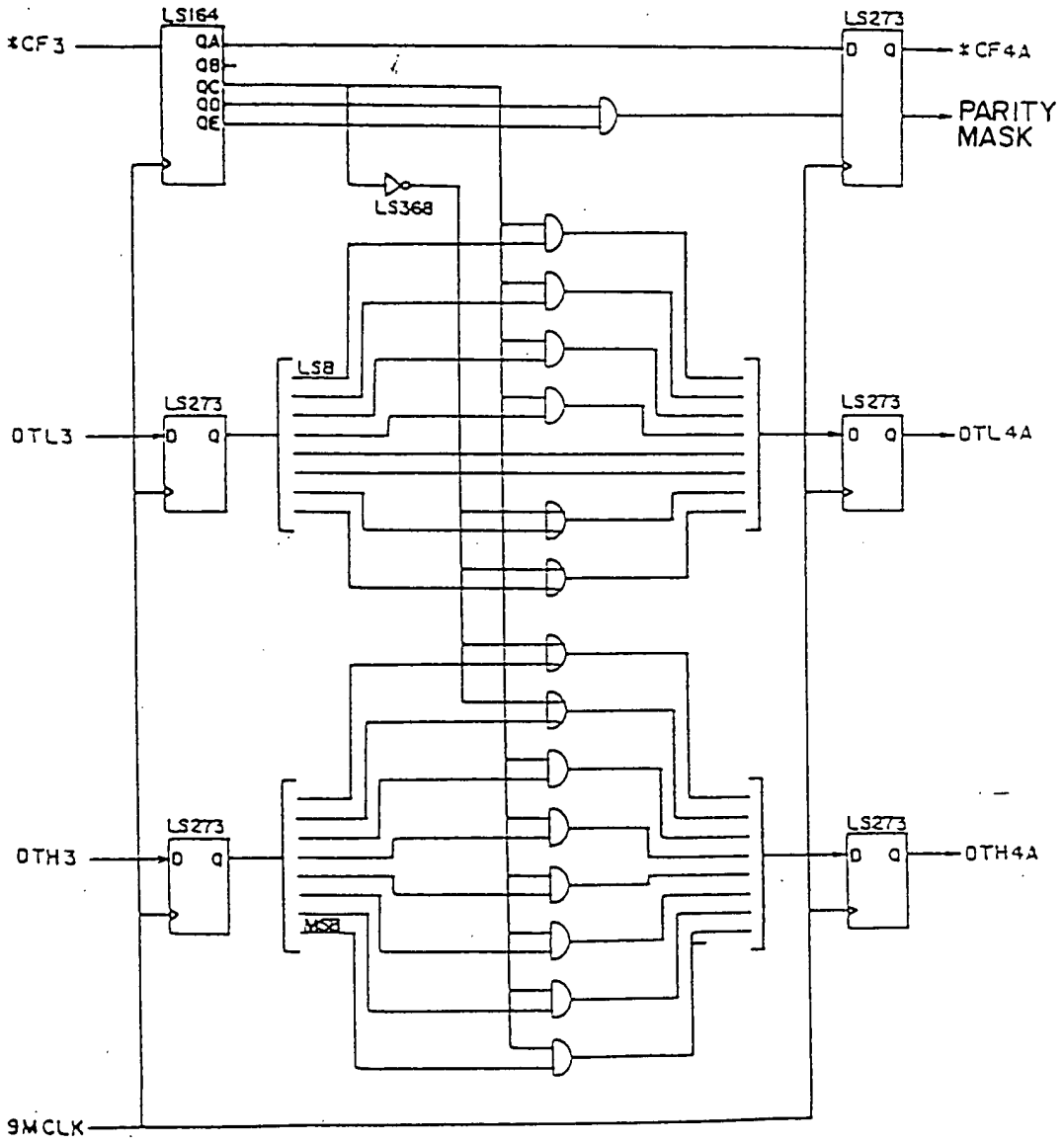

LS164
*CF3
QA
QB
QC
QD
QE
LS273
D Q
*CF4A
PARITY
MASK
LS368
LS8
LS273
OTL3
D Q
LS273
D Q
OTL4A
LS273
OTH3
D Q
LS273
D Q
OTH4A
MSB
9MCLK

FIG. 574

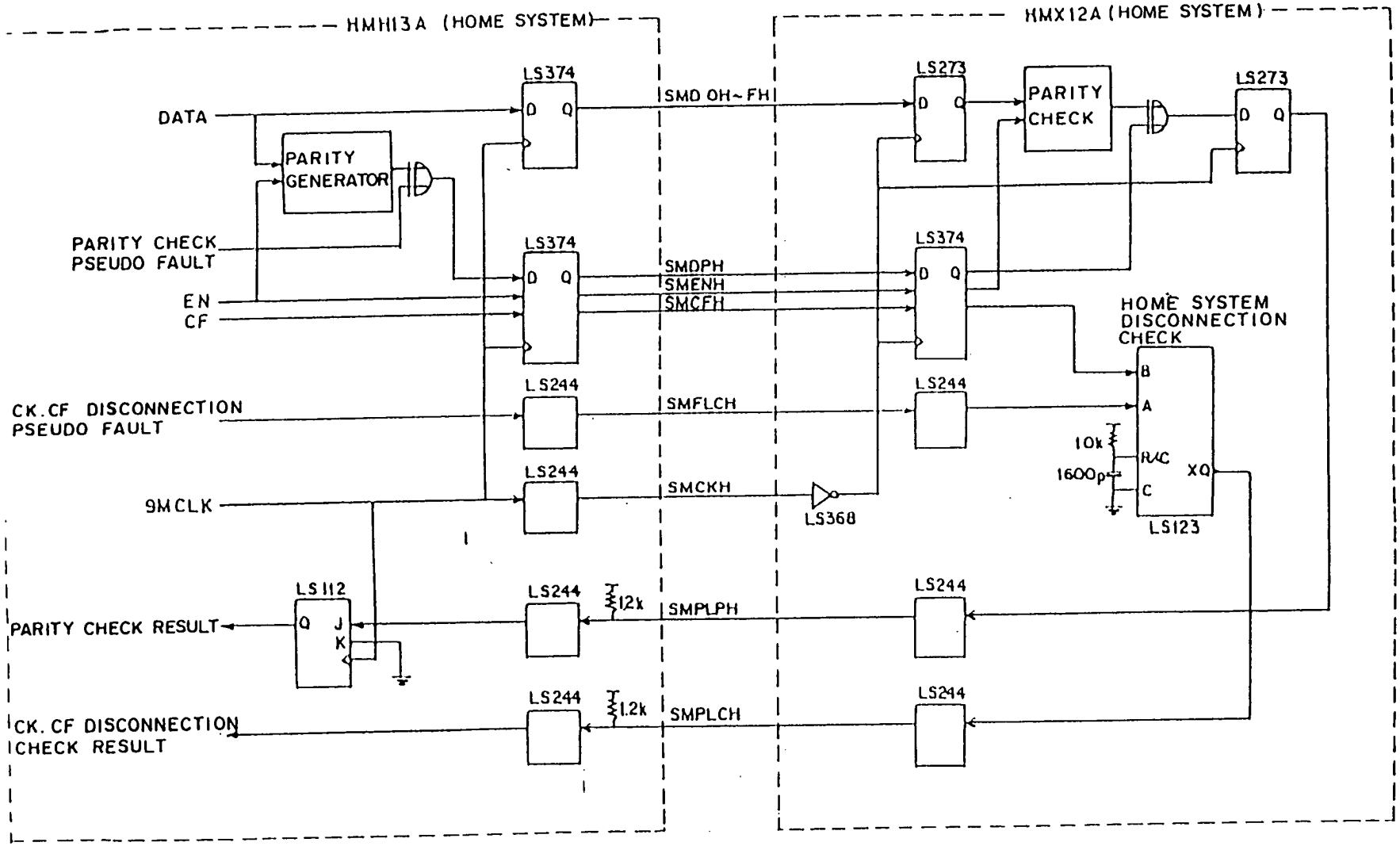

HMH13A (HOME SYSTEM)
HMX12A (HOME SYSTEM)
DATA
PARITY GENERATOR
PARITY CHECK PSEUDO FAULT
EN
CF
CK.CF DISCONNECTION PSEUDO FAULT
9MCLK
PARITY CHECK RESULT
CK.CF DISCONNECTION CHECK RESULT
LS374
LS273
LS244
LS112
LS368
LS123
SMD 0H~FH
SMDPH
SMENH
SMCFH
SMFLCH
SMCKH
SMPLPH
SMPLCH
PARITY CHECK
HOME SYSTEM DISCONNECTION CHECK
12k
1.2k
10k
1600p

FIG. 575

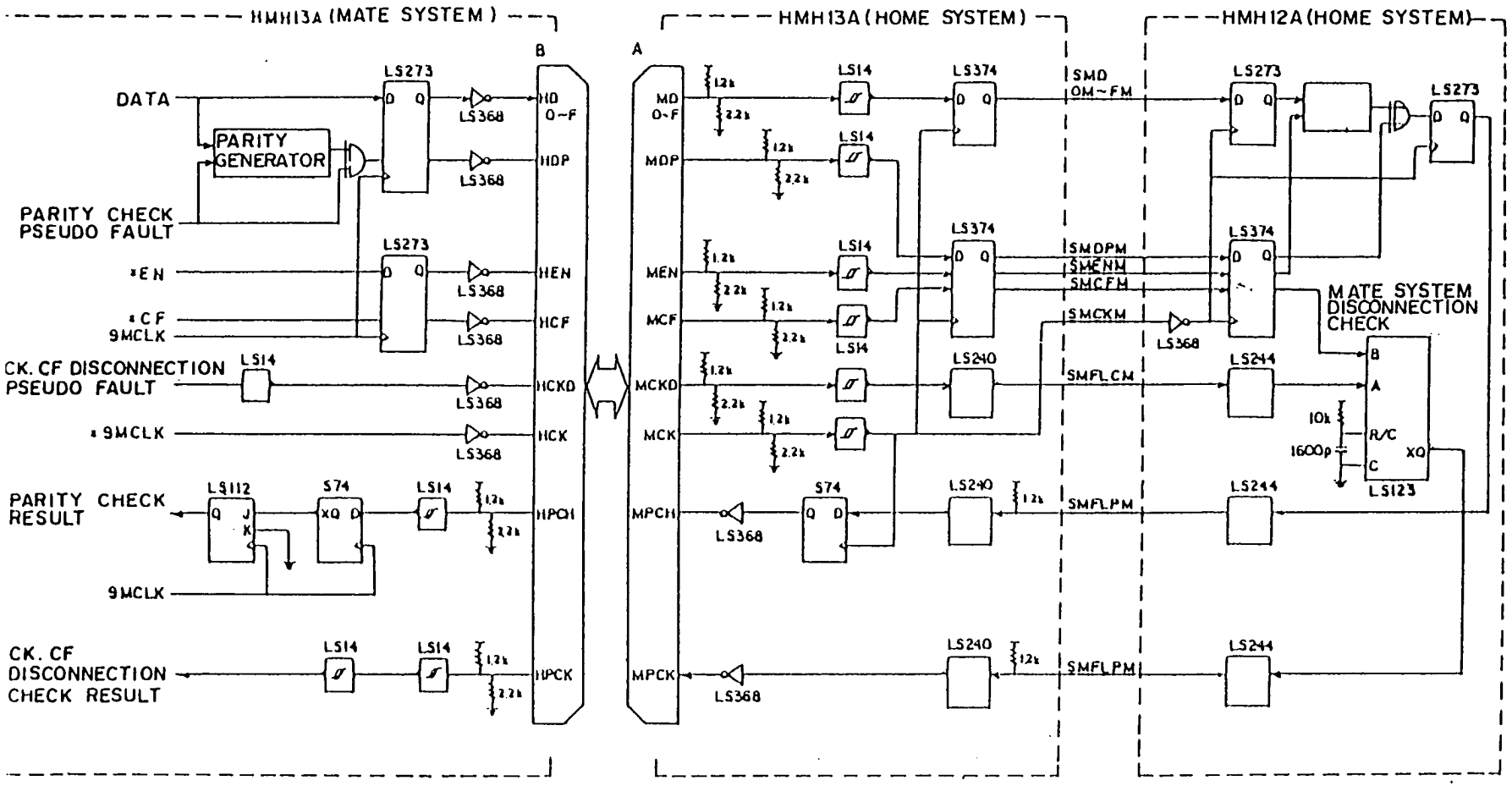

HMH13A (MATE SYSTEM)
HMH13A (HOME SYSTEM)
HMH12A (HOME SYSTEM)
DATA
PARITY GENERATOR
PARITY CHECK PSEUDO FAULT
*EN
*CF
9MCLK
CK. CF DISCONNECTION PSEUDO FAULT
* 9MCLK
PARITY CHECK RESULT
9MCLK
CK. CF DISCONNECTION CHECK RESULT
LS273
LS368
LS14
LS112
S74
LS374
LS240
LS244
LS123
MD 0~F
MDP
MEN
MCF
MCKD
MCK
MPCH
MPCK
SMD 0M~FM
SMDPM
SMENM
SMCFM
SMCKM
SMFLCM
SMFLPM
MATE SYSTEM DISCONNECTION CHECK
10k
1600p
R/C
HD 0~F
HDP
HEN
HCF
HCKD
HCK
HPCH
HPCK

FIG. 576

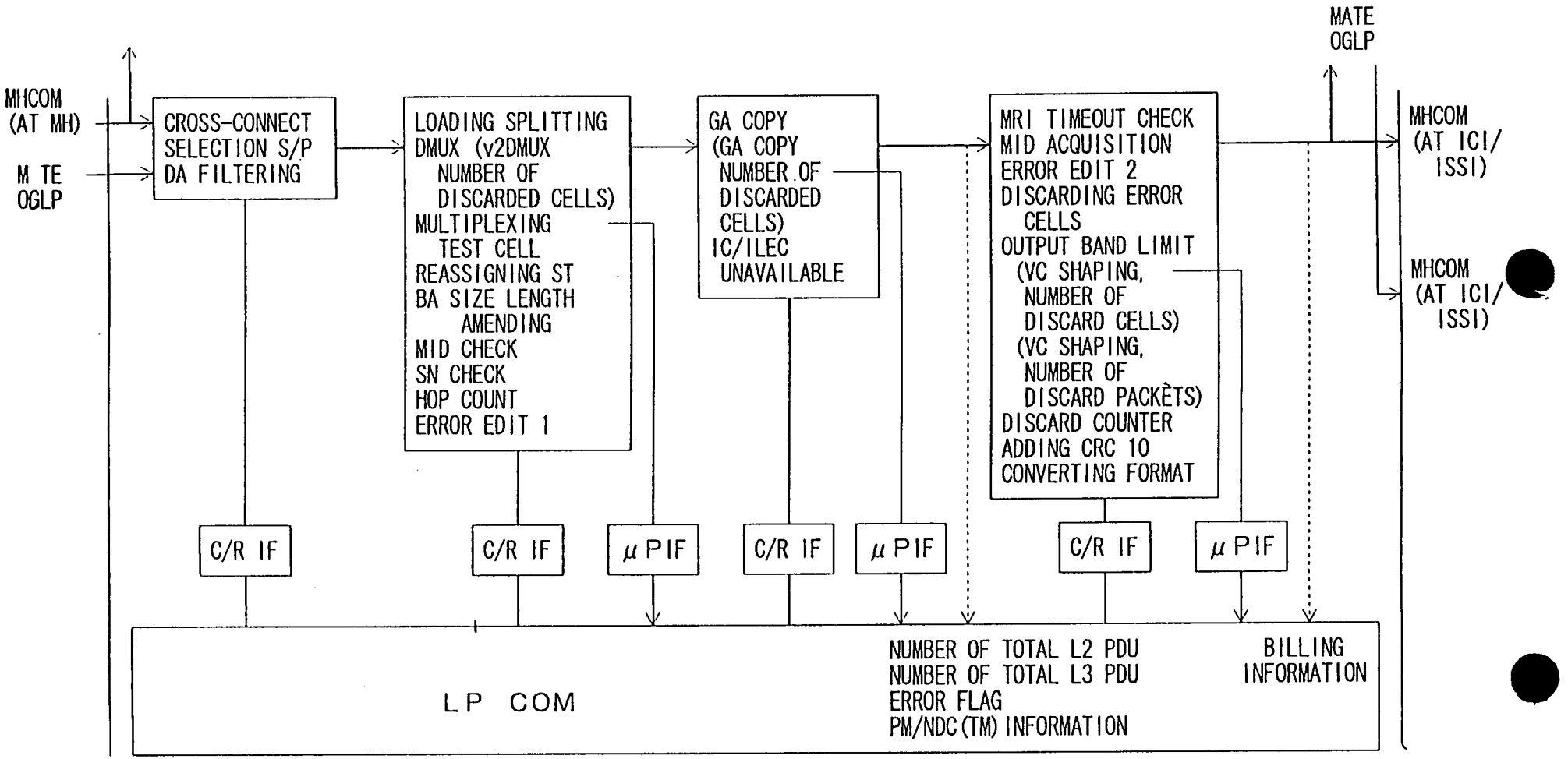

MHCOM
(AT MH)
M TE
OGLP
CROSS-CONNECT
SELECTION S/P
DA FILTERING
LOADING SPLITTING
DMUX (v2DMUX
NUMBER OF
DISCARDED CELLS)
MULTIPLEXING
TEST CELL
REASSIGNING ST
BA SIZE LENGTH
AMENDING
MID CHECK
SN CHECK
HOP COUNT
ERROR EDIT 1
GA COPY
(GA COPY
NUMBER OF
DISCARDED
CELLS)
IC/ILEC
UNAVAILABLE
MRI TIMEOUT CHECK
MID ACQUISITION
ERROR EDIT 2
DISCARDING ERROR
CELLS
OUTPUT BAND LIMIT
(VC SHAPING,
NUMBER OF
DISCARD CELLS)
(VC SHAPING,
NUMBER OF
DISCARD PACKETS)
DISCARD COUNTER
ADDING CRC 10
CONVERTING FORMAT
MATE
OGLP
MHCOM
(AT ICI/
ISSI)
MHCOM
(AT ICI/
ISSI)
C/R IF
C/R IF
μPIF
C/R IF
μPIF
C/R IF
μPIF
LP COM
NUMBER OF TOTAL L2 PDU
NUMBER OF TOTAL L3 PDU
ERROR FLAG
PM/NDC(TM) INFORMATION
BILLING
INFORMATION

FIG. 577

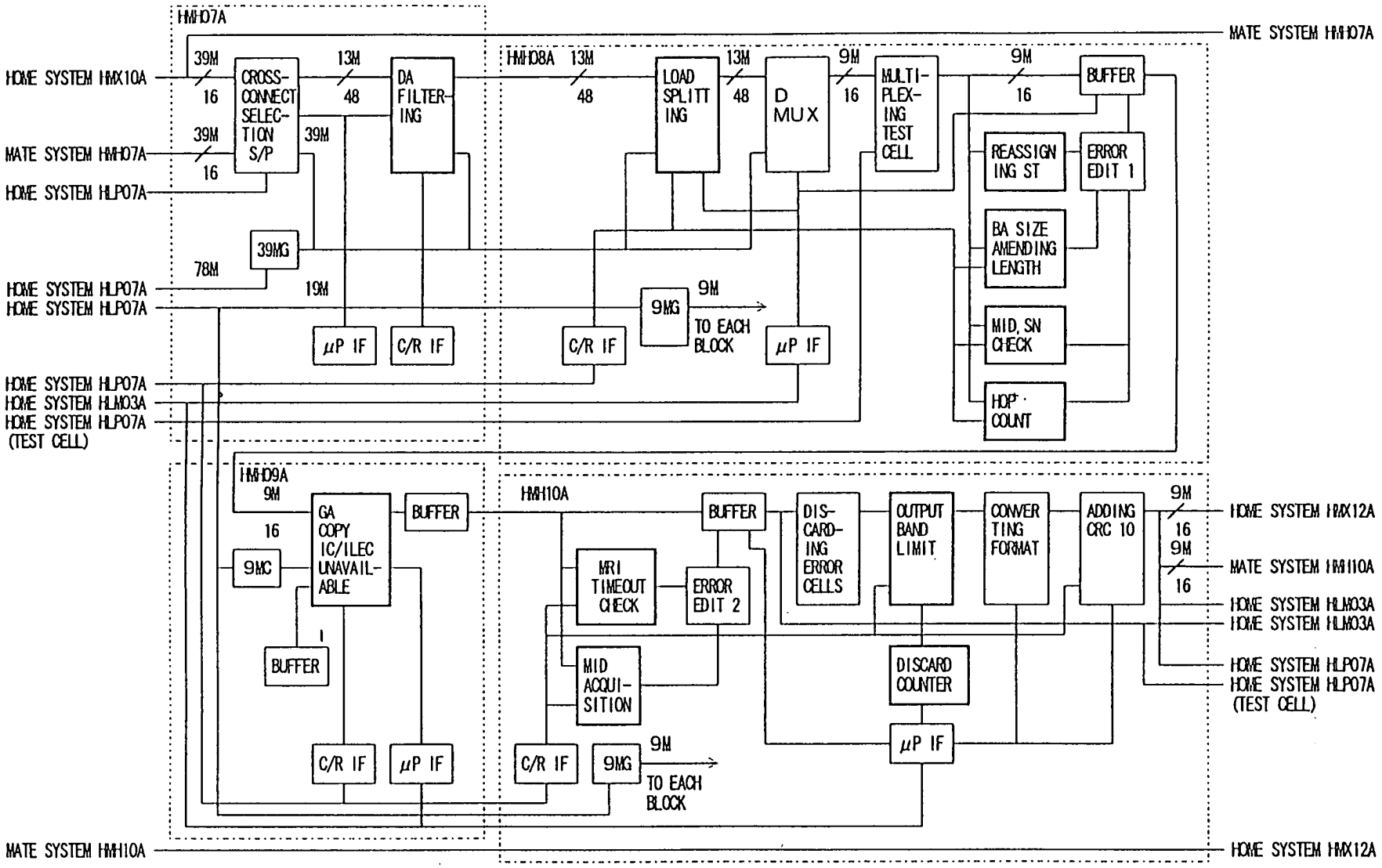

HMH07A
MATE SYSTEM HMH07A
HOME SYSTEM HMX10A
39M
16
CROSS-CONNECT SELEC-TION S/P
13M
48
DA FILTER-ING
HMH08A 13M
48
LOAD SPLITT ING
13M
48
D MUX
9M
16
MULTI-PLEX-ING TEST CELL
9M
16
BUFFER
REASSIGN ING ST
ERROR EDIT 1
BA SIZE AMENDING LENGTH
MID, SN CHECK
HOP COUNT
MATE SYSTEM HMH07A
HOME SYSTEM HLP07A
39MG
78M
19M
9MG
9M
TO EACH BLOCK
μP IF
C/R IF
C/R IF
μP IF
HOME SYSTEM HLP07A
HOME SYSTEM HLM03A
HOME SYSTEM HLP07A
(TEST CELL)
HMH09A
9M
16
9MC
GA COPY IC/ILEC UNAVAIL-ABLE
BUFFER
BUFFER
C/R IF
μP IF
HMH10A
BUFFER
MRI TIMEOUT CHECK
ERROR EDIT 2
MID ACQUI-SITION
C/R IF
9MG
9M
TO EACH BLOCK
DIS-CARD-ING ERROR CELLS
OUTPUT BAND LIMIT
CONVER TING FORMAT
ADDING CRC 10
DISCARD COUNTER
μP IF
9M
16
9M
16
HOME SYSTEM HMX12A
MATE SYSTEM HMH10A
HOME SYSTEM HLM03A
HOME SYSTEM HLM03A
HOME SYSTEM HLP07A
HOME SYSTEM HLP07A
(TEST CELL)
MATE SYSTEM HMH10A
HOME SYSTEM HMX12A

FIG. 578

6698260 "EP2260

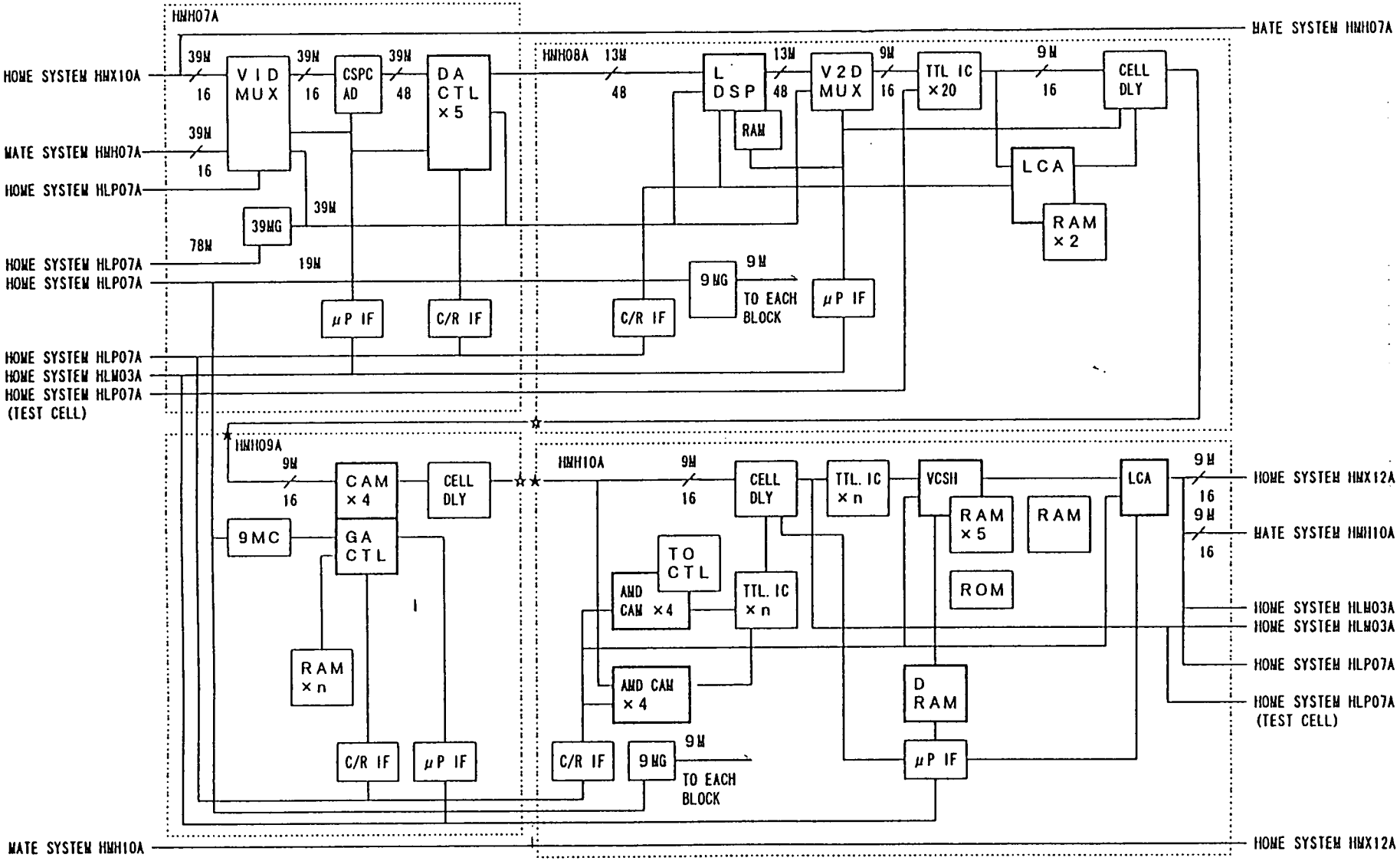


FIG. 579

ITEM	BROCK NAME	CONTENTS	PWCB
1	CROSS-CONNECT SELECTION	TCG CELL FOR USE IN SELECTING MDX ACT SYSTEM DATA ACCORDING TO SYSTEM INFORMATION OF SWITCH.	HMH07A
2	S/P	38.88 MB/S (16 PARALLEL) IS CONVERTED INTO 12.96 MB/S (48 PARALLEL).	
3	DA FILTERING (V2DMUX NUMBER OF DISCARDED CELLS)	ISSI AND ICI ADDRESSED TO DESTINATION ARE SPECIFIED BY DA AND CARRIER.	
4	LOAD SPLITTING	KEY IS GENERATED BY COMBINATION OF DA AND SA.	HMH08A
5	DMUX.	622.08 MB/S (12.96 MHZ 48 PARALLEL) IS CONVERTED INTO 155.52 MB/S (9.72 MHZ 16 PARALLEL).	
6	MULTIPLEXING TEST CELL	TEST CELL IS MULTIPLEXED AT IDLE CELLS IN LINE. TEST CELL IS PRIORITIZED DURING DIAGNOSTICS.	
7	REASSIGNING ST	ST VALUE OF SIP IS ASSIGNED TO ENCAPSULATED CELL.	
8	AMENDING BA SIZE LENGTH	BA SIZE LENGTH VALUE IS AMENDED.	
9	MID CHECK	IT IS CHECKED THAT VCI/MID IS NOT ACTIVE AT BOM AND THAT VCI/MID IS ACTIVE AT COM AND EOM.	
10	SN CHECK	IT IS CHECKED THAT SN IS INITIALIZED AT BOM AND SN IS IN GOOD ORDER AT COM AND EOM.	
11	HOP COUNT	1 IS SET EACH TIME INITIAL VALUE IS SET AND SS IS PASSED TO DETECT INDEFINITE SS LOOP OF PACKET. RESULTANT 0 INDICATES DISCARD.	
12	ERROR EDIT I	ERROR GENERATED AT EACH CHECK UINT IS ASSIGNED TO EACH POSITION.	
13	GA COPY (NUMBER OF DISCARDED CELLS)	CELL INPUT AT GA IS COPIED AND OUTPUT TO ISSI AND ICI ADDRESSED TO DESTINATION.	HMH09A
14	IC/ILEC UNAVAILABLE	CELL DETERMINED TO BE IC/ILEC UNAVAILABLE BY ROUTING TABLE IS DISCARDED.	
15	MRI TIMEOUT CHECK	TIME TO BOM AND EOM IS CHECKED IN L3 PDU UNITS.	HMH10A
16	MID ACQUISITION	OUTPUT MID IS CONVERTED.	
17	ERROR EDIT II	ERROR FLAG GENERATED IN EACH CHECKER IS ASSIGNED TO EACH POSITION.	
18	DISCARDING ERROR CELLS	NG CELLS ARE DISCARDED BY MS (MASTER ERROR) OF ERROR FLAG.	
19	OUTPUT BAND LIMIT (VC SHAPING, NUMBER OF DISCARDED CELLS) (VC SHAPING, NUMBER OF DISCARDED PACKETS)	OUTPUT BAND (PEAK PATE) IS LIMITED FOR EACH OUTPUT MH.	
20	DISCARD COUNTER	DISCARDED CELLS GENERATED BY DMUX, GA COPY, AND OUTPUT BAND LIMIT ARE COUNTED AND REPORTED TO LP-COM.	
21	GENERATING CRC-10	CRC-10 OF CELL PAYLOAD IS GENERATED AND ADDED.	
22	CONVERTING FORMAT	FORMAT IS CONVERTED.	
23	39MC	78 MHZ CLOCK IS RECEIVED FROM HLP02A TO GENERATE 39 MHZ CLOCK TO BE USED IN OGLP UNIT AND CELL FRAME.	HMH07A
24	μ P INTERFACE	INTERFACES WITH μ P OF HLM01A.	PWCB EXCLUDING HMH07A
25	9MC	19 MHZ CLOCK IS RECEIVED FROM HLP02A TO GENERATE 9 MHZ CLOCK TO BE USED IN OGLP UNIT.	PWCB EXCLUDING HMH07A
26	COMMAND RESPONSE INTERFACE	INTERFACES WITH C/R OF HLP02A.	COMMON TO EACH PWCB

FIG. 580

	Error Flag / Message	E1 MS	E2 MT	E1 MC	E2 MA	E2 SN	E2 LC	E2 GA	E2 EM	PVC
A	BOM with Unexpected MID	ON			ON					
	COM with Unexpected MID	ON		ON						
	EOM with Unexpected MID	ON			ON					
B	Unexpected SN Error	ON		OK	OK	ON				
C	ILEC/IC Unavailable	ON					ON			
D	CARRIER SELECTION	OK								
E	RMID ACQUISITION	OK								
F	MRI Time Out		ON							
G	GA COPY	ON		OK	OK	ON				
H	LIMIT OF SIMULTANEOUS TRANSMISSION NUMBER	ON		OK	OK				ON	

'ON': EF INDICATING "ON" WHEN CHECK RESULT OUTPUTS NG
'OK': CHECK IS MADE ONLY WHEN OK-MARKED EF INDICATES "OK".
'NO MARK': CHECK IS MADE REGARDLESS OF OK OR NG OF 'NO MARK' EF
'M': NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 581

HMH07 INPUT CELL (FROM SB)
INTER-MH BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00		0														
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	1	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	SIP PBEtag							
05	SIP BAsize															
06	ISSIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad I		QOS				CI	HE Len		
15	Bridging															
16	Header Extension (SIP)															
17																
18																
19																
20																
21																
22	Ingress Interface Type								ES	DC						
23	Carrier															
24	Incominng Network ID															
25	Incoming ICI Transmission Path Set															
26	PL Len.								CRC							

FIG. 582

INTER-MH SSM CELL

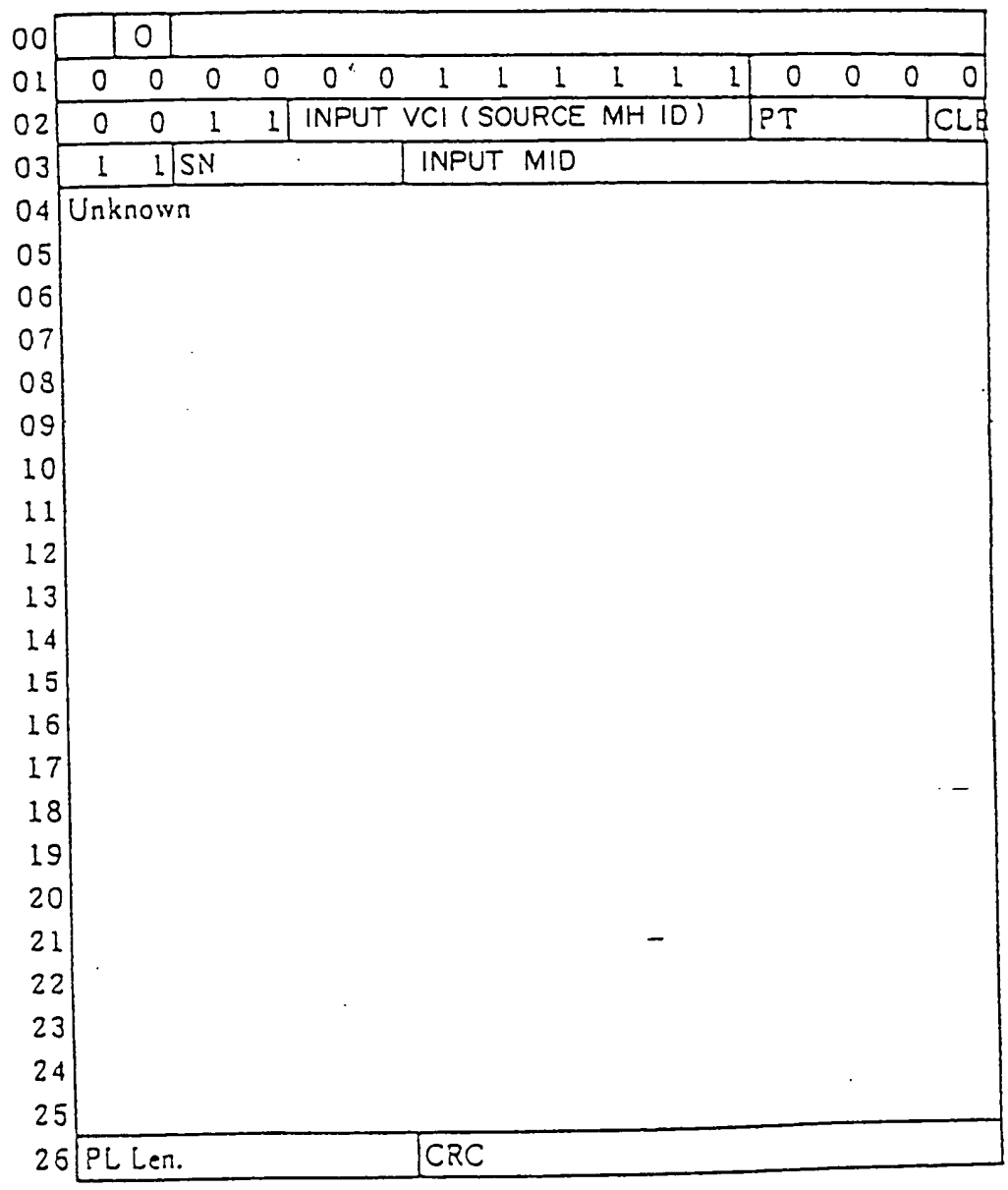


FIG. 583

SIP BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	0															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	0	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				CI	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	PL Len.						CRC									

FIG. 584

SIP SSM CELL

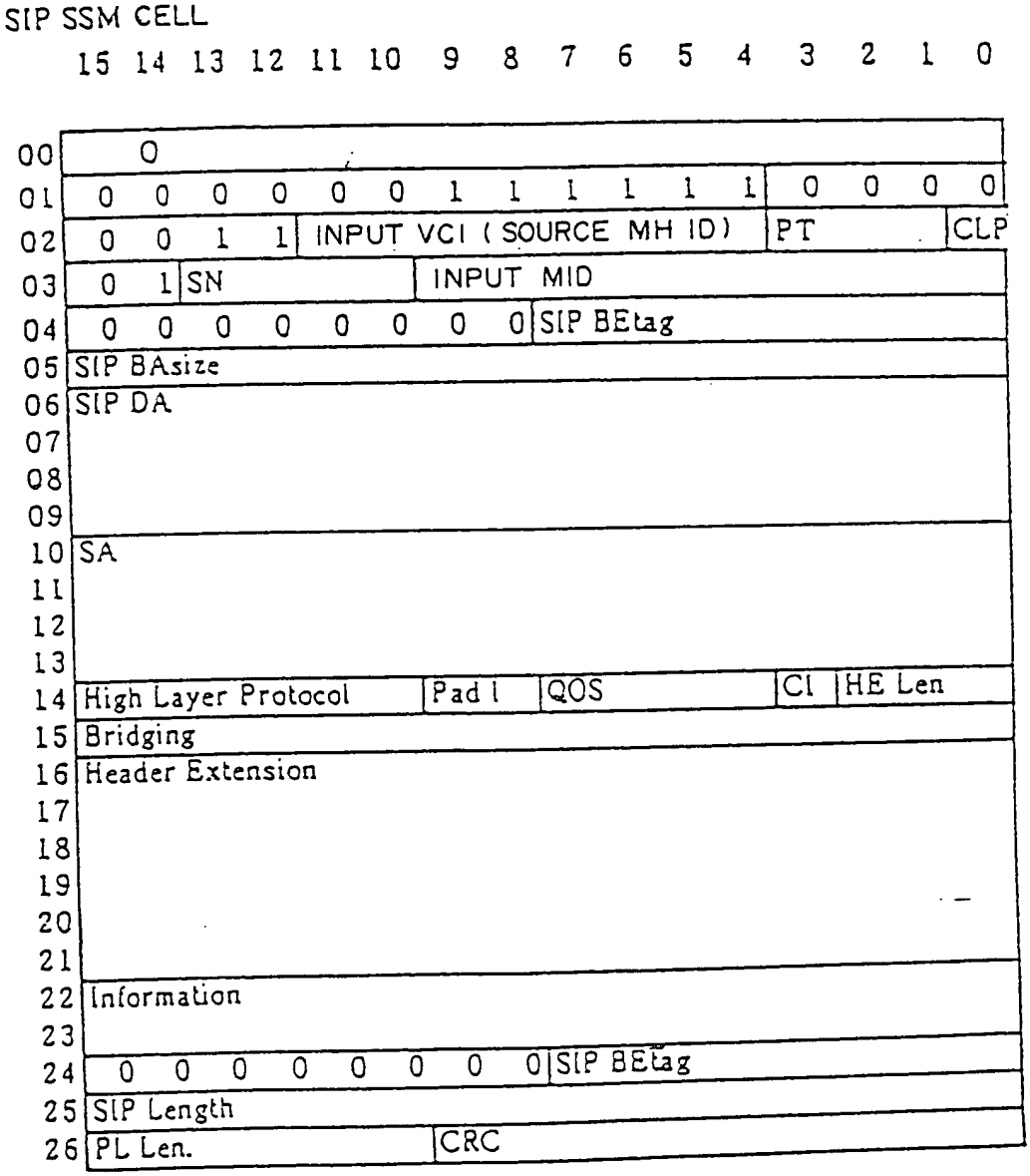


FIG. 585

SIP COM CELL

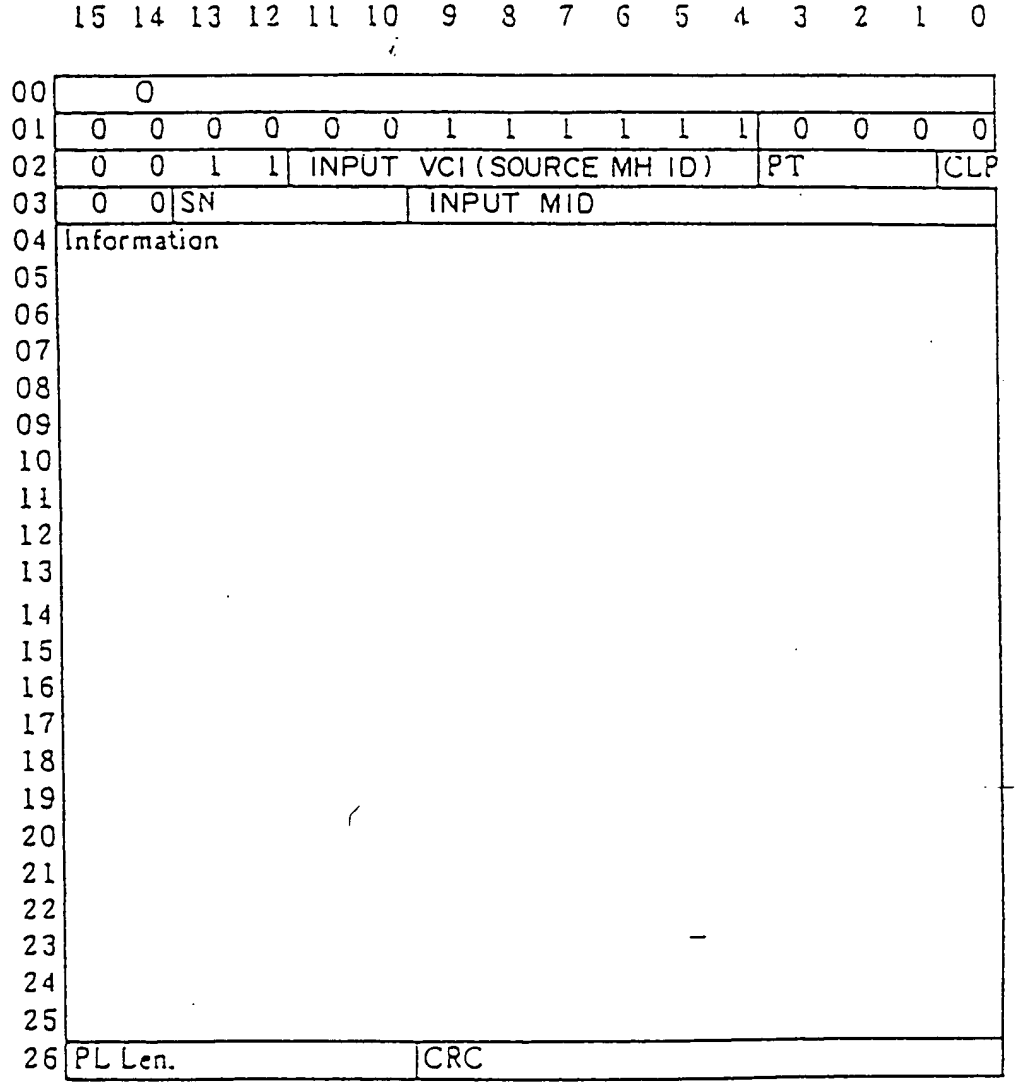


FIG. 586

SIP EOM(Inter-MH EOM) CELL

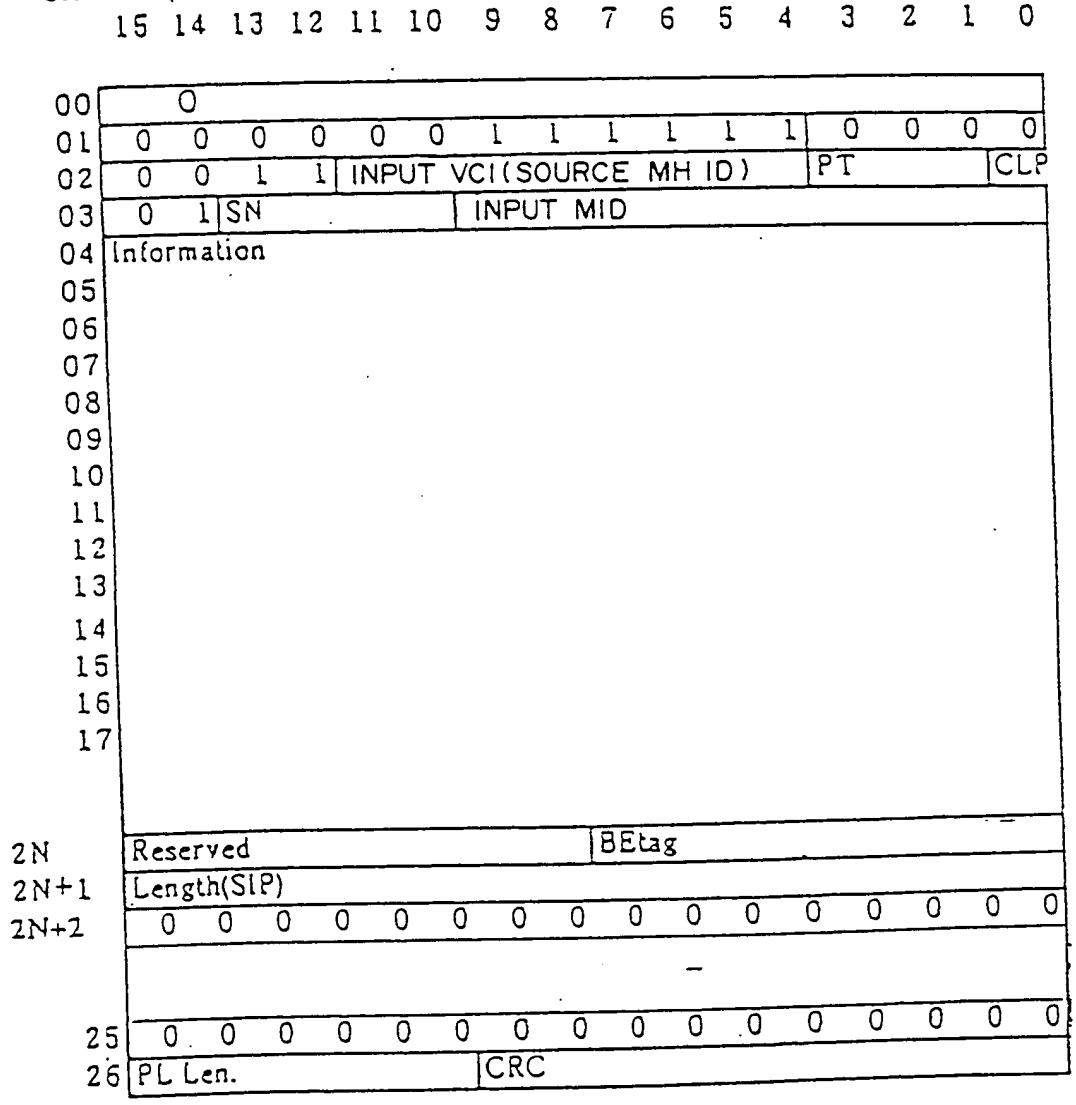


FIG. 587

HMH07 INPUT CELL (FROM GW)
INTER-MH BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00		0														
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	1	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	ISSIP BEtag							
05	SIP BAsize															
06	ISSIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	Service type															
15																
16	Header Extension															
17																
18																
19																
20																
21																
22	Ingress Interface Type								ES	Hop Count Ind						
23	Carrier															
24	Incominng Network ID															
25	Incoming ICI Transmission Path Set															
26	PL Len.								If	(CRC)						

VALID ONLY WHEN INPUT INTERFACE TO SS OF HOME SYSTEM IS ISSI AND IF BIT INDICATES 0

FIG. 588

INTER-MH SSM CELL

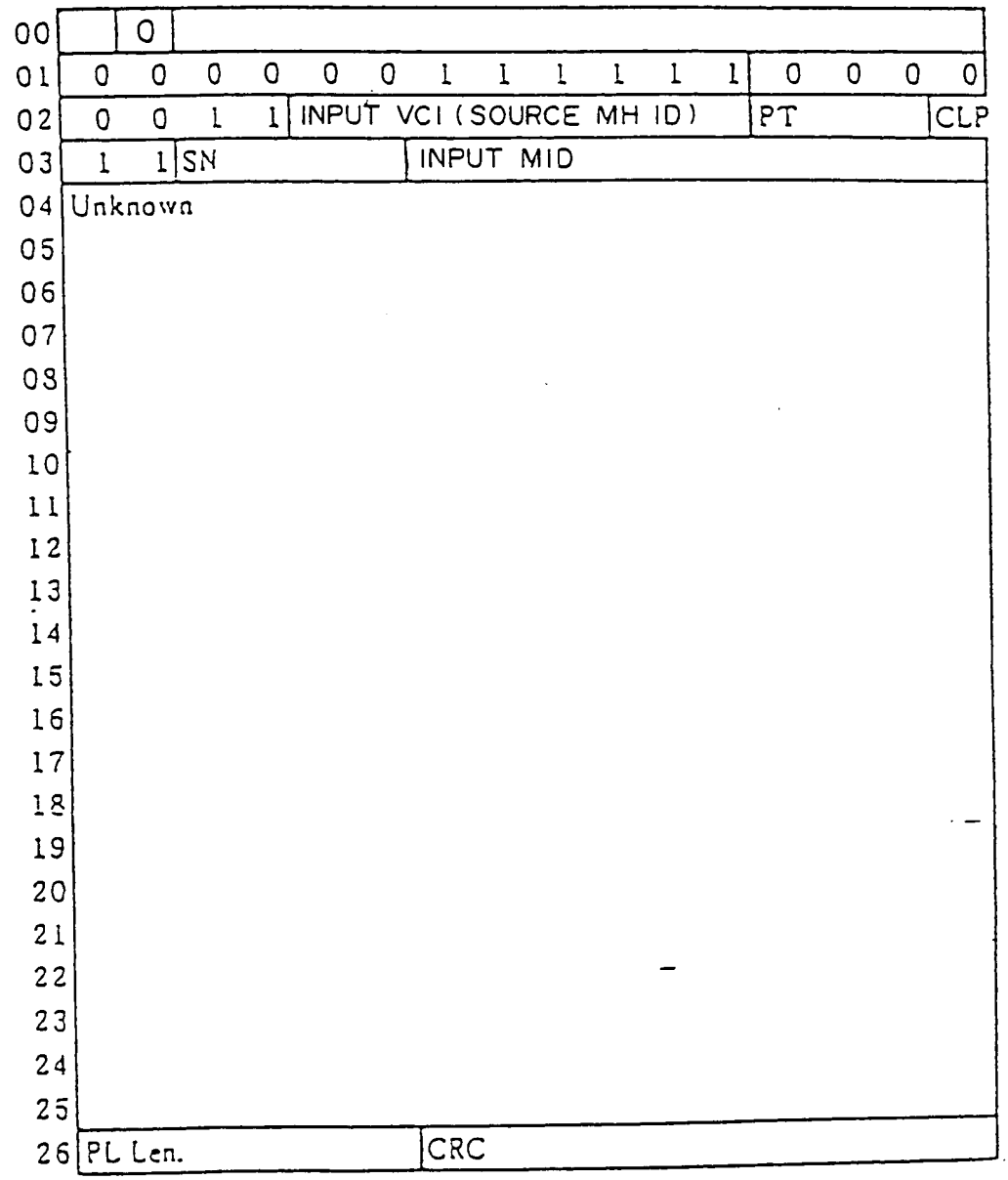


FIG. 589

SIP BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	0															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	0	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				CI	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	PL Len.						lf								(CRC)	

FIG. 590

SIP SSM CELL

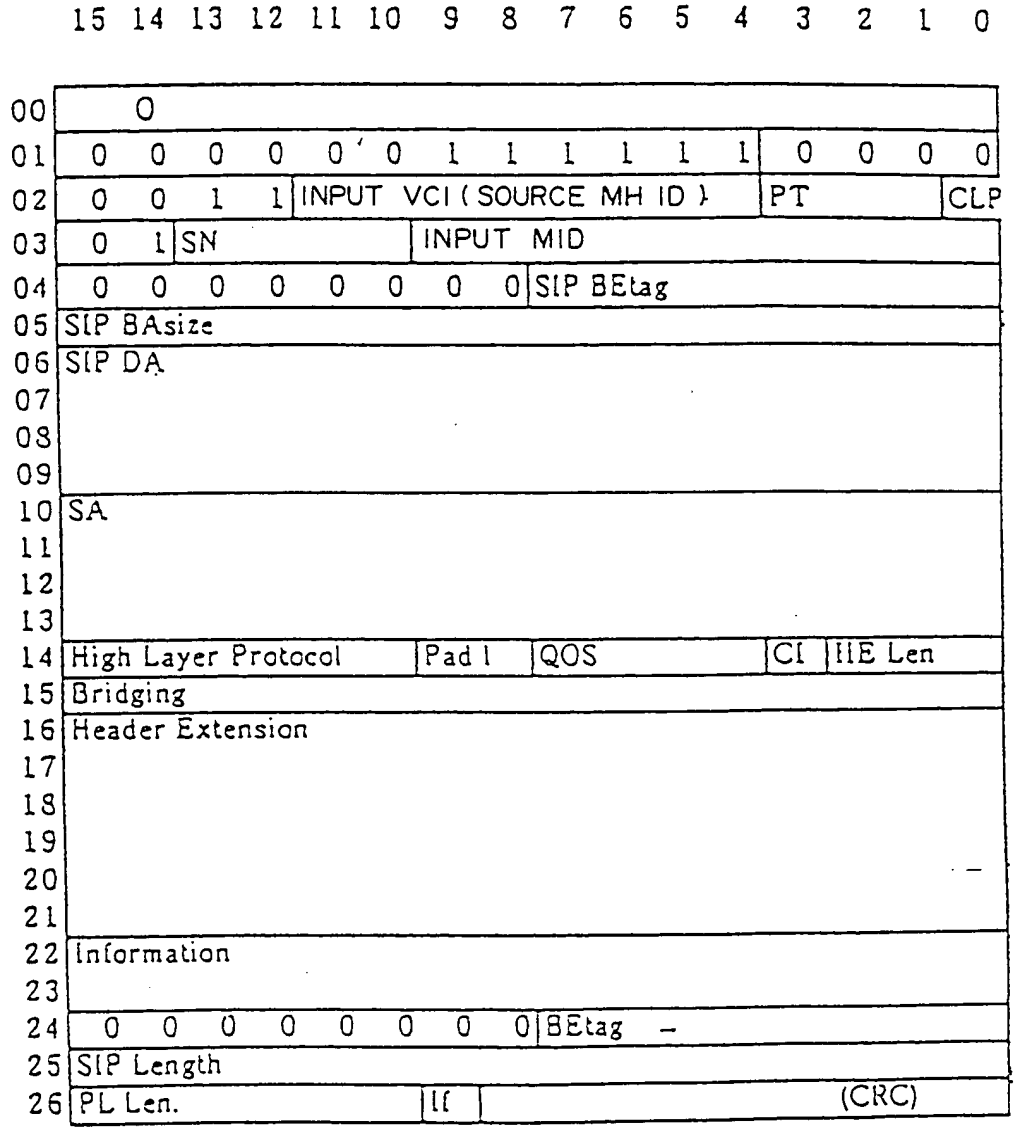


FIG. 591

SIP COM CELL

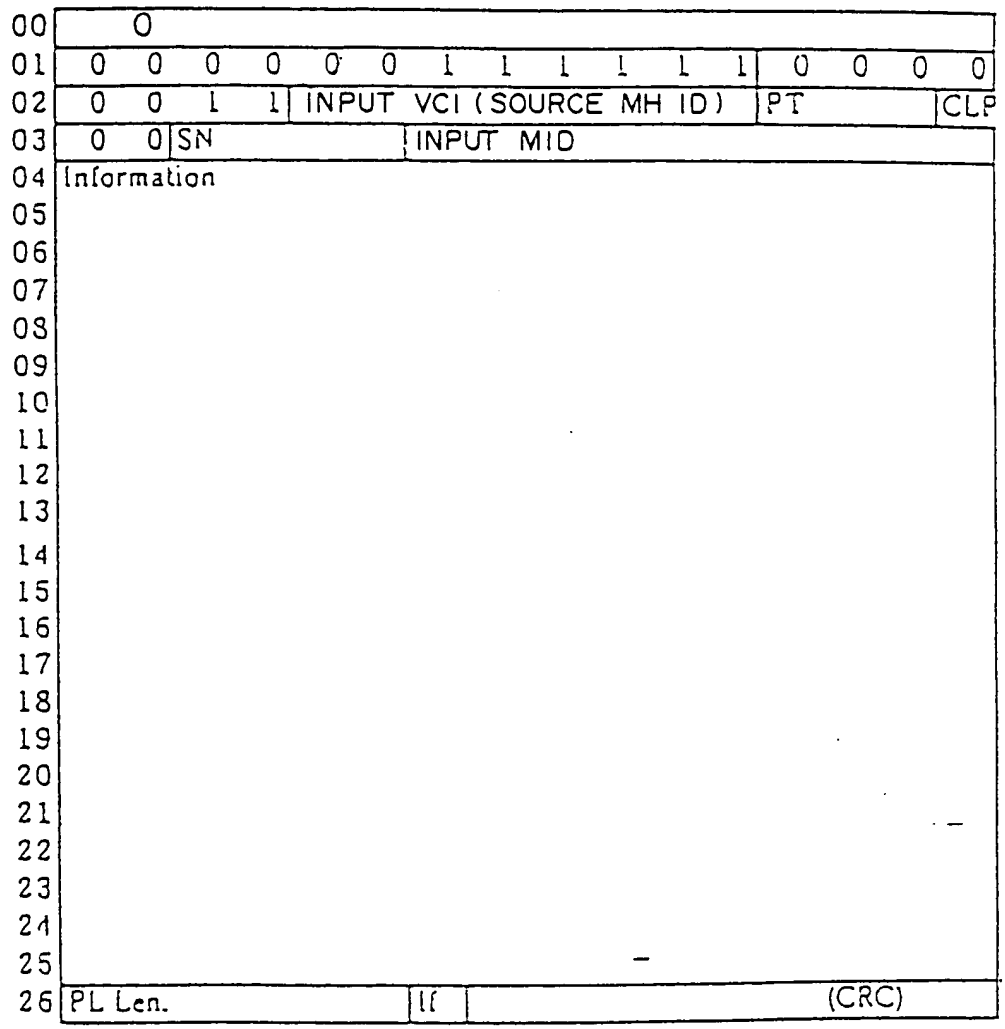


FIG. 592

SIP EOM(Inter-MH EOM) CELL

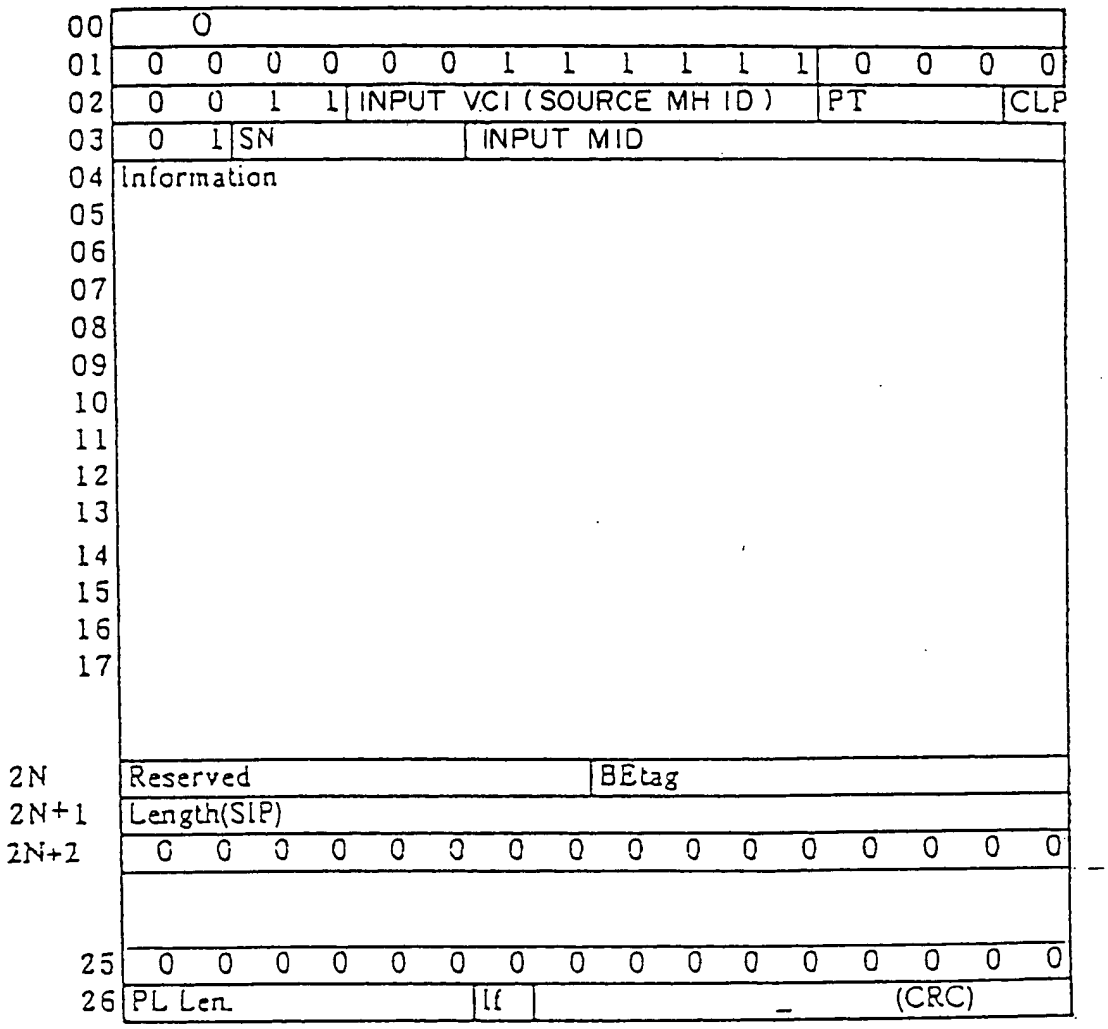


FIG. 593

HMH08 INPUT CELL (FROM GW)
INTER-MH BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	ST			DM	DC			MCHPO			MADRO					
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	1	0	SN					INPUT MID								
04	0	0	0	0	0	0	0	0	ISSIP BEtag							
05	SIP BAsize															
06	ISSIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	Service type															
15																
16	Header Extension															
17																
18																
19																
20																
21																
22	Ingress Interface Type								ES	Hop Count Ind						
23	Carrier															
24	Incominng Network ID															
25	Incoming ICI Transmission Path Set															
26	PL Len.							If	(CRC)							

VALID ONLY WHEN INPUT INTERFACE TO SS OF HOME SYSTEM IS ISSI AND IF BIT INDICATES 0

FIG. 594

INTER-MH SSM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	ST			DM	DC			MCHPO			MADRO					
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	1	1	SN					INPUT MID								
04	Unknown															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
20																
21																
22																
23																
24																
25																
26	PL Len.						CRC									

FIG. 595

SIP BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	ST		DC													
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	0	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				Cl	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	PL Len.						lf							(CRC)		

FIG. 596

SIP SSM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	ST		DC													
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	0	1	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				CI	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24	0	0	0	0	0	0	0	0	BEtag							
25	SIP Length															
26	PL Len.							If						(CRC)		

FIG. 597

SIP COM CELL

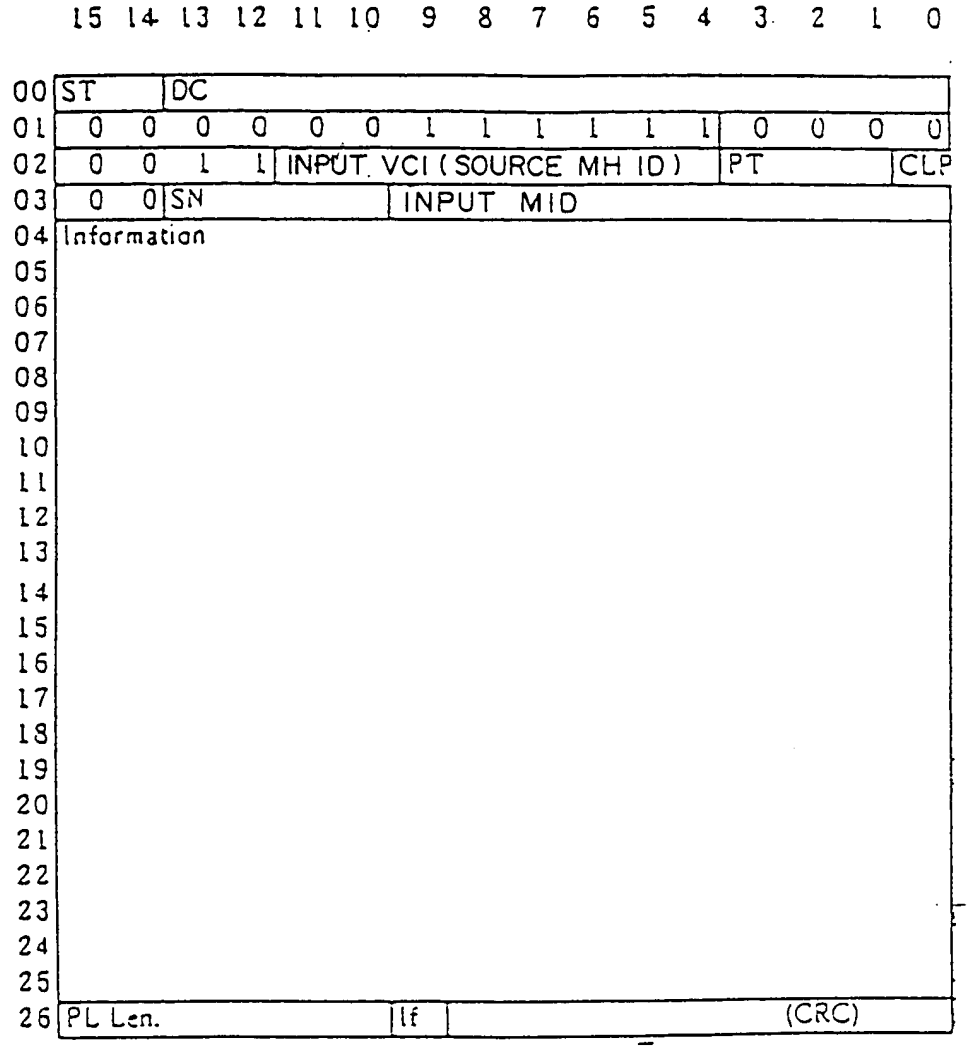


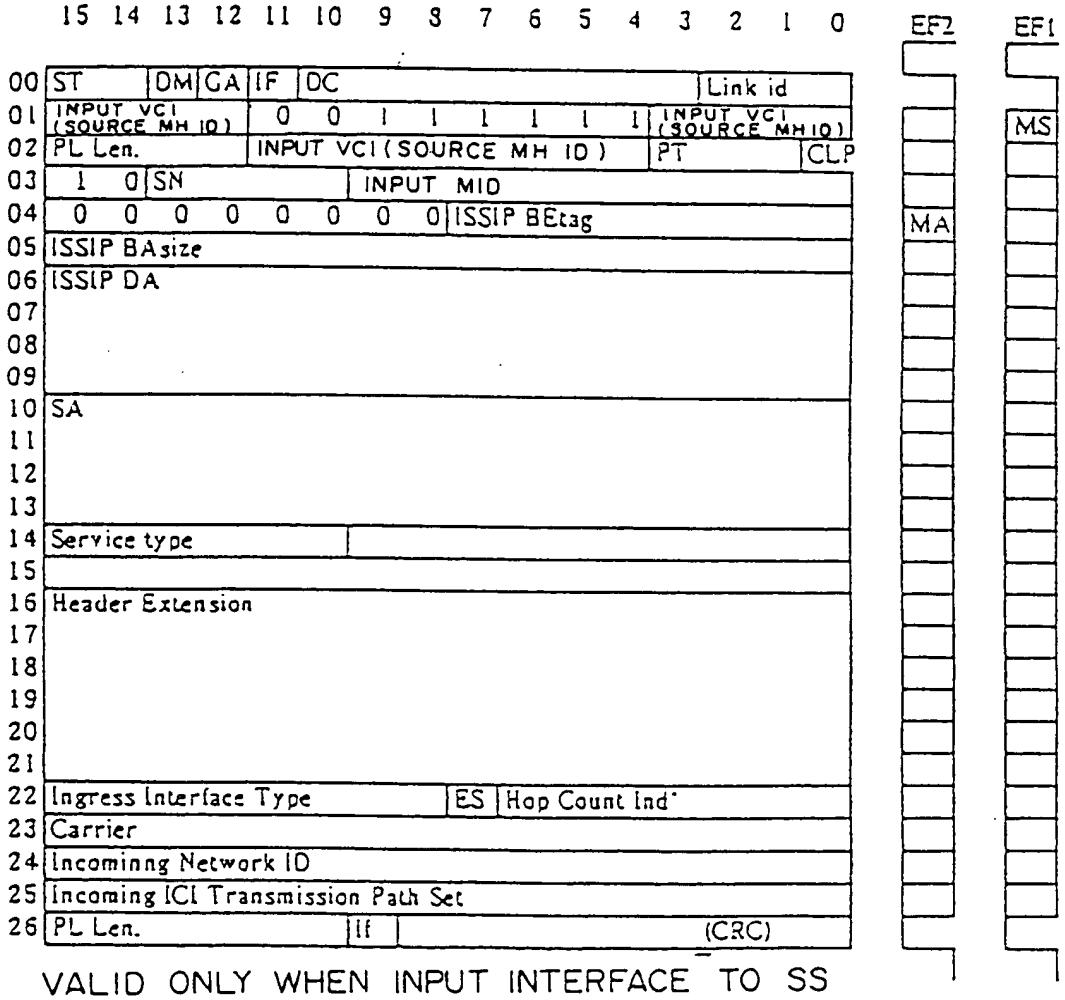
FIG. 598

SIP EOM(Inter-MH EOM) CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	ST		DC													
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT			CLP
03	0	1	SN				INPUT MID									
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
2N	Reserved												BEtag			
2N+1	Length(SIP)															
2N+2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	PL Len.						If						(CRC)			

FIG. 599

HMH09 INPUT CELL (FROM GW)
INTER-MH BOM CELL



VALID ONLY WHEN INPUT INTERFACE TO SS OF HOME SYSTEM IS ISSI AND IF BIT INDICATES 0.

FIG. 600

INTER MII SSM CELL

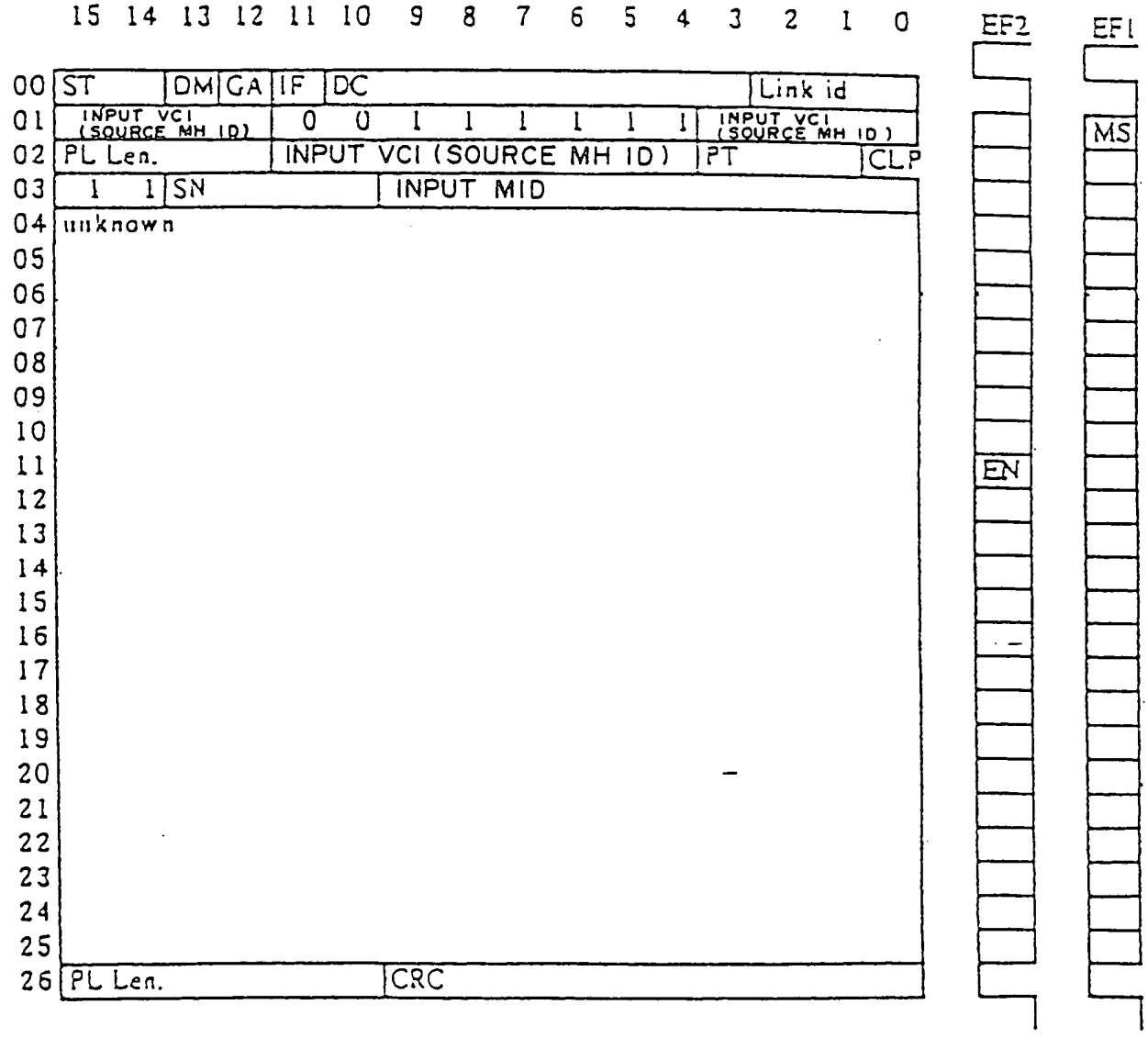


FIG. 601

SIP BOM CELL

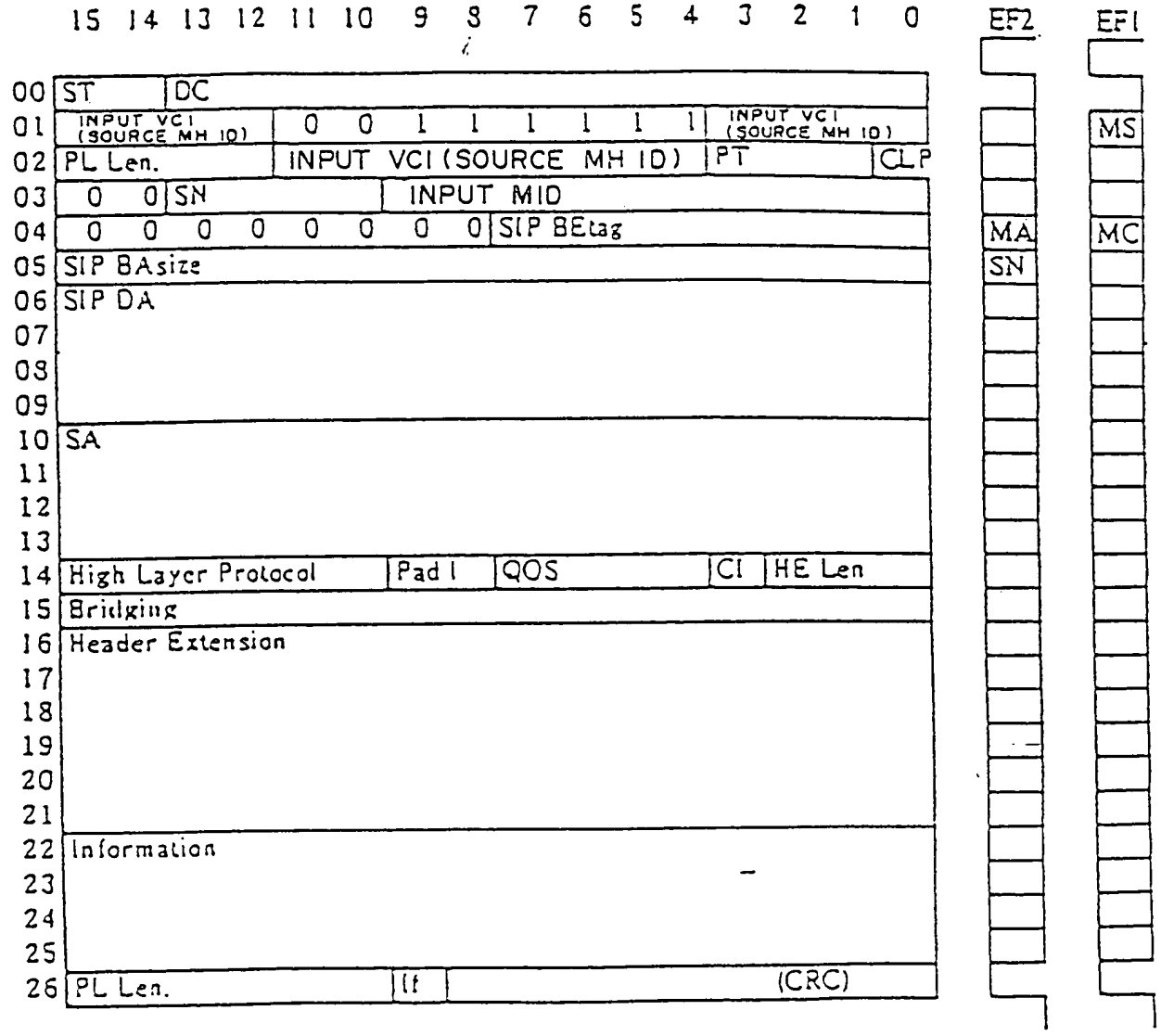


FIG. 602

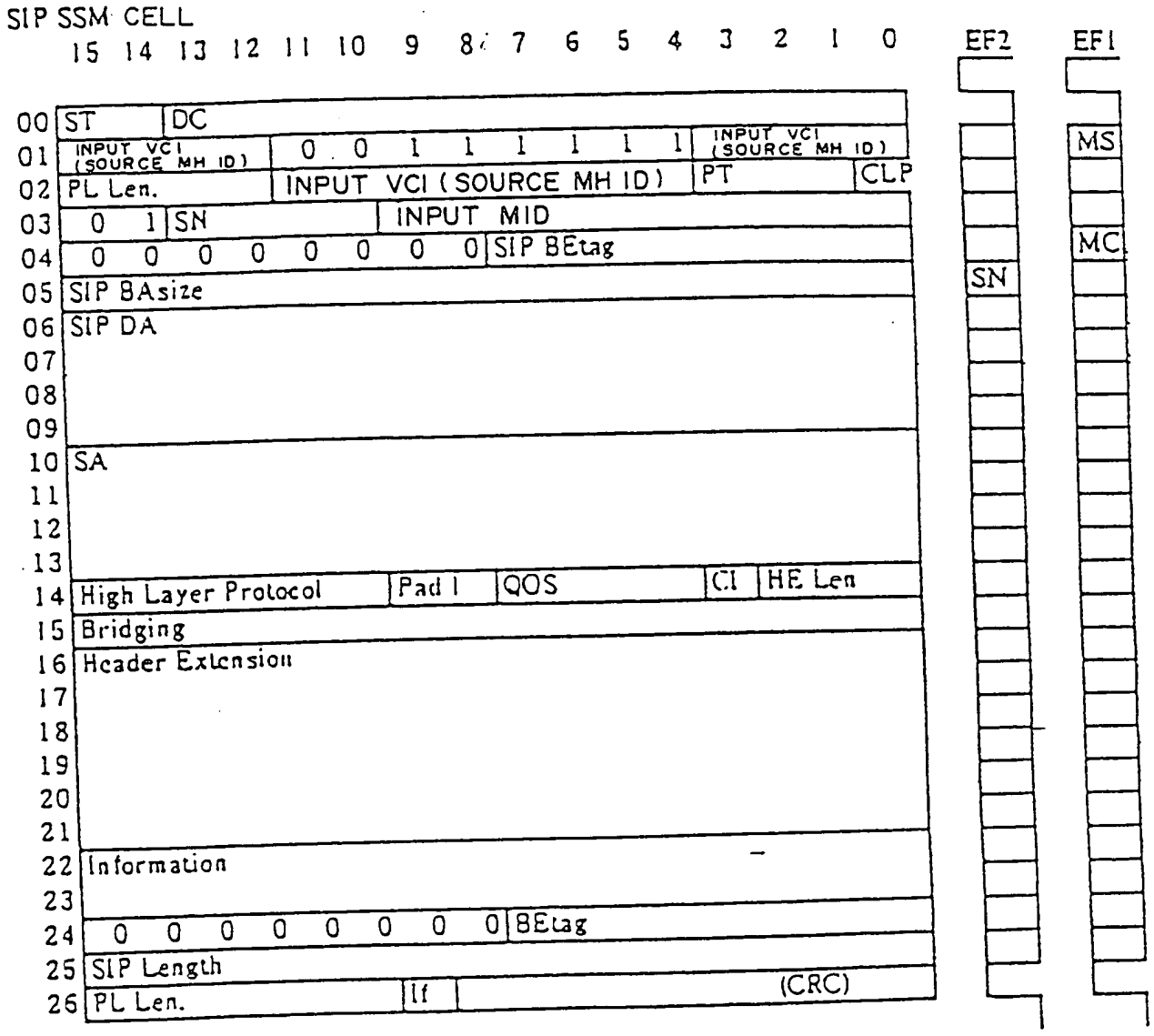

SIP SSM CELL
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
EF2
EF1
00 ST DC
01 INPUT VCI (SOURCE MH ID) 0 0 1 1 1 1 1 1 INPUT VCI (SOURCE MH ID)
02 PL Len. INPUT VCI (SOURCE MH ID) PT CLP
03 0 1 SN INPUT MID
04 0 0 0 0 0 0 0 0 SIP BEtag
05 SIP BAsize
06 SIP DA
07
08
09
10 SA
11
12
13
14 High Layer Protocol Pad l QOS CI HE Len
15 Bridging
16 Header Extension
17
18
19
20
21
22 Information
23
24 0 0 0 0 0 0 0 0 BEtag
25 SIP Length
26 PL Len. If (CRC)
MS
MC
SN

FIG. 603

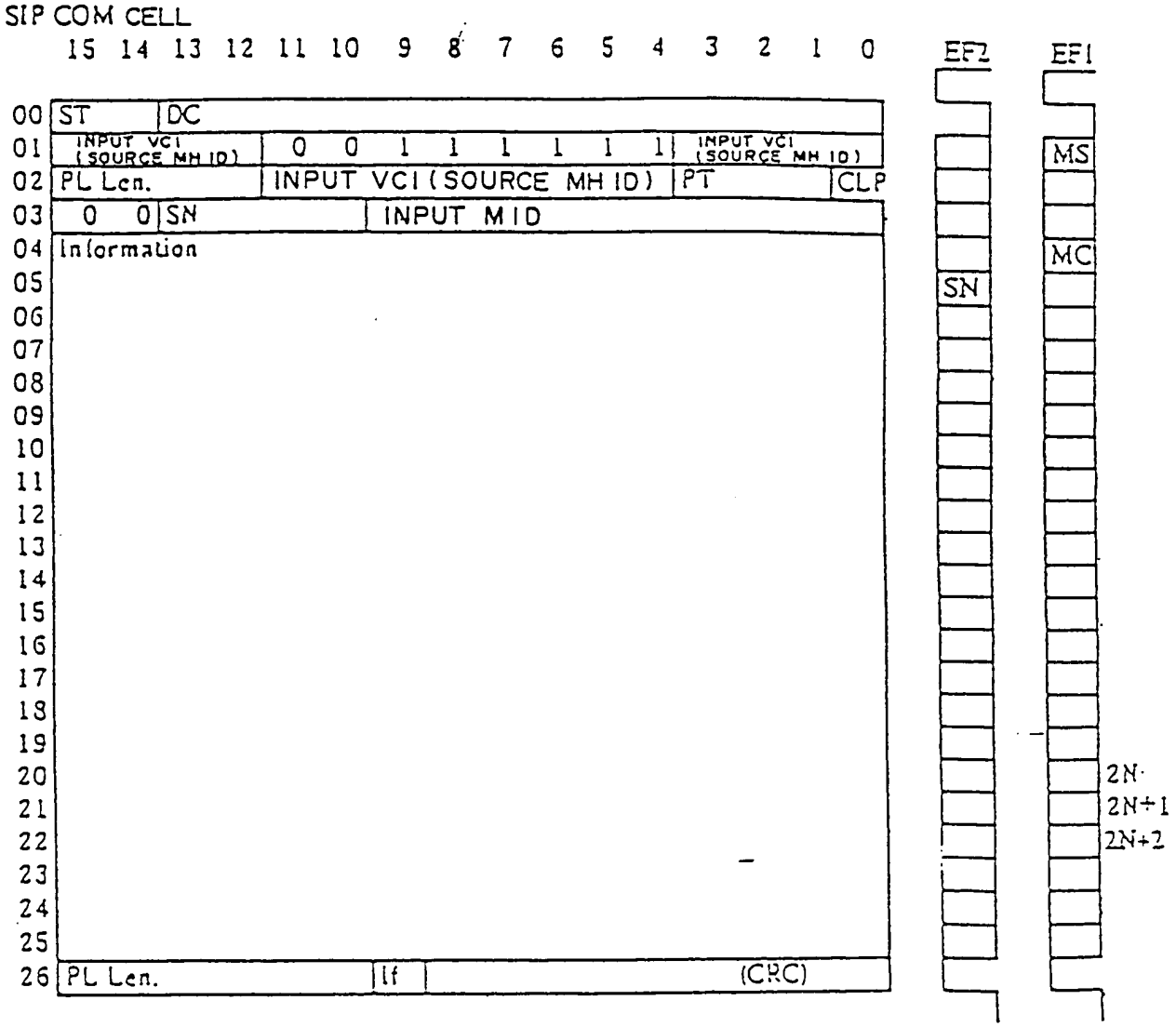

SIP COM CELL
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
00 ST DC
01 INPUT VCI (SOURCE MH ID) 0 0 1 1 1 1 1 1 INPUT VCI (SOURCE MH ID)
02 PL Len. INPUT VCI (SOURCE MH ID) PT CLP
03 0 0 SN INPUT MID
04 Information
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26 PL Len. If (CRC)
EF2
EF1
MS
MC
SN
2N
2N+1
2N+2

FIG. 604

SIP EOM(Inter-MH EOM) CELL

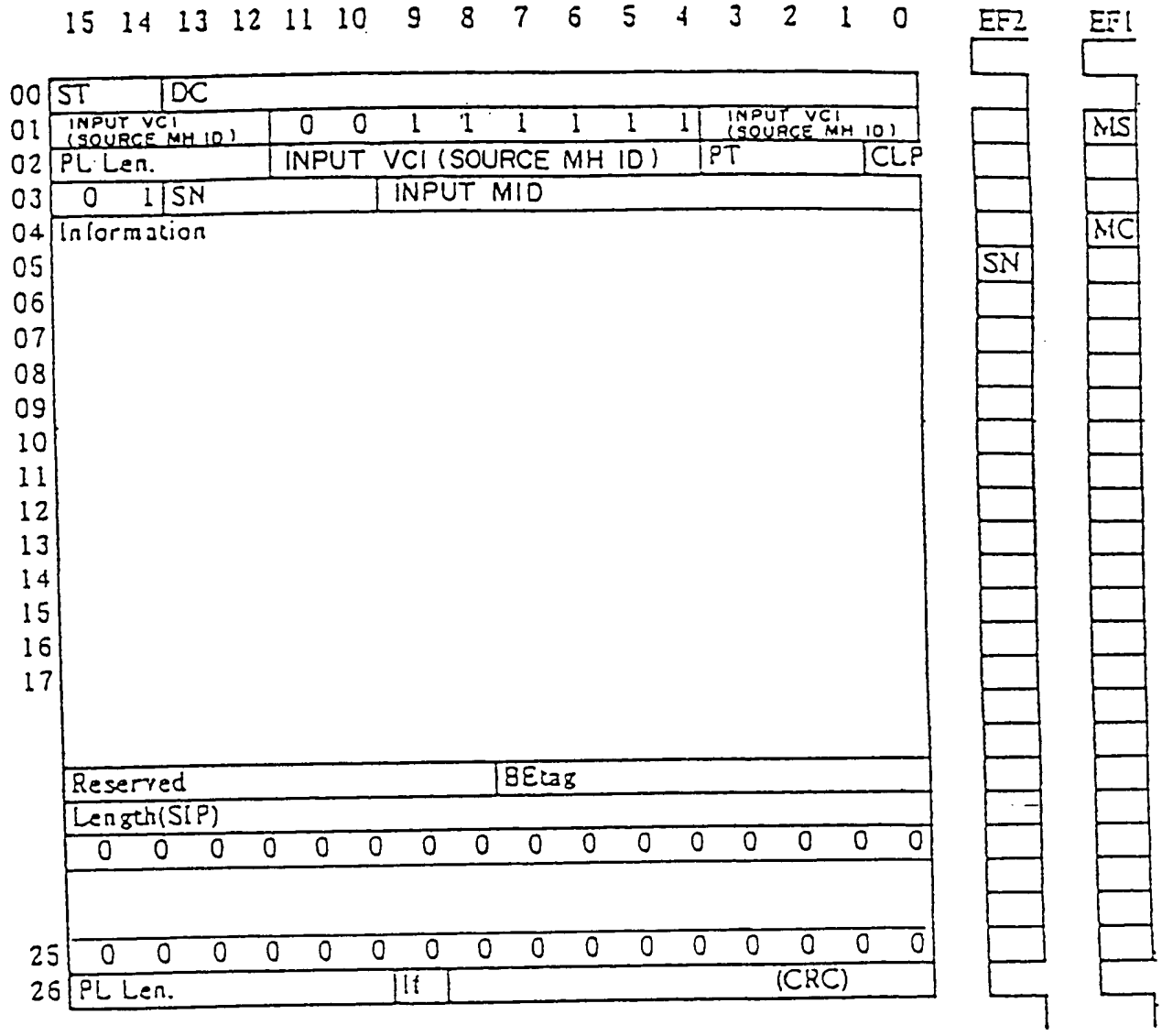
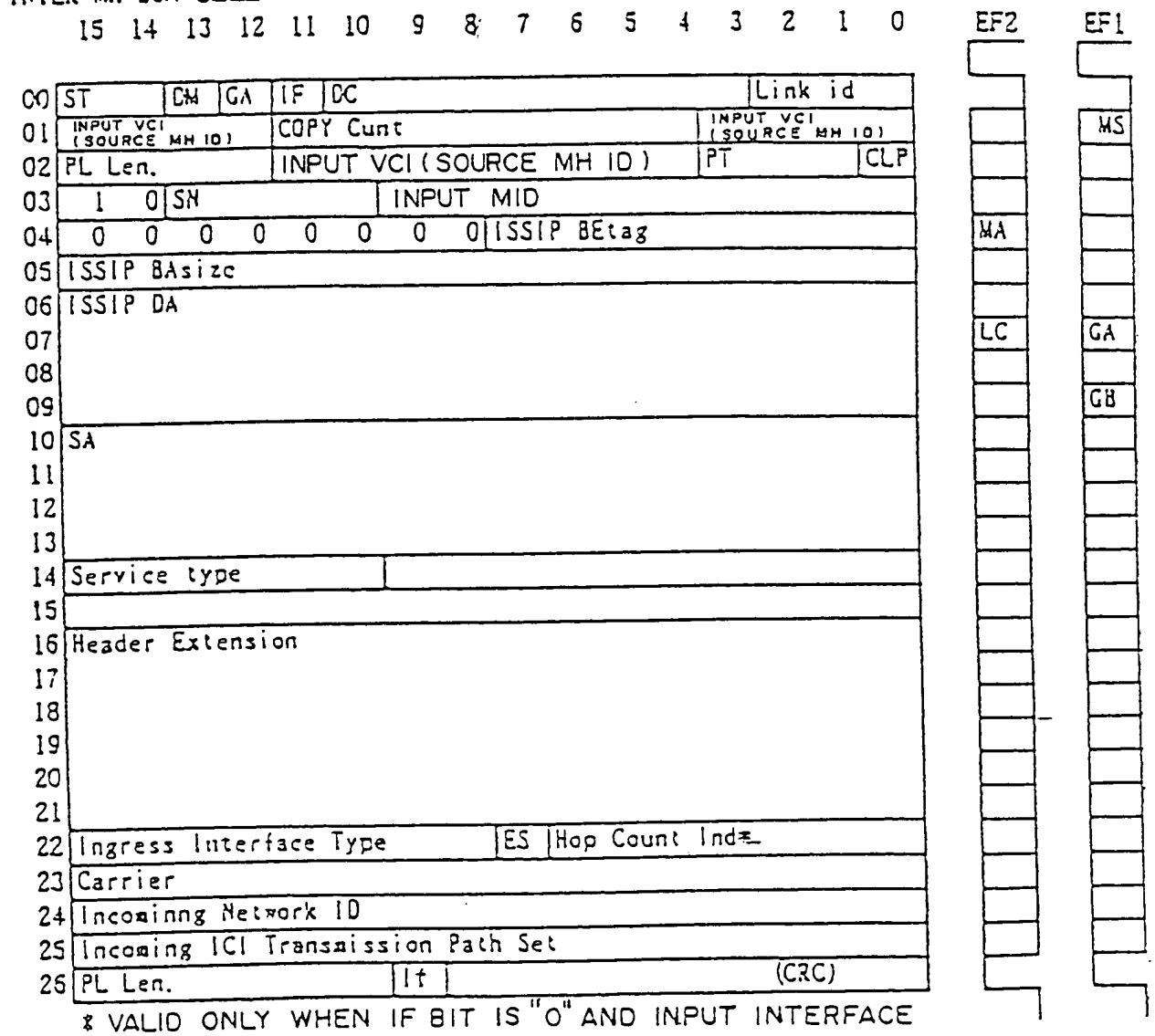


FIG. 605

HMH10 INPUT CELL (FROM GW)

INTER-MH BOM CELL



* VALID ONLY WHEN IF BIT IS "0" AND INPUT INTERFACE TO SS OF HOME SYSTEM IS ISSI

FIG. 606

INTER-MH SSM CELL

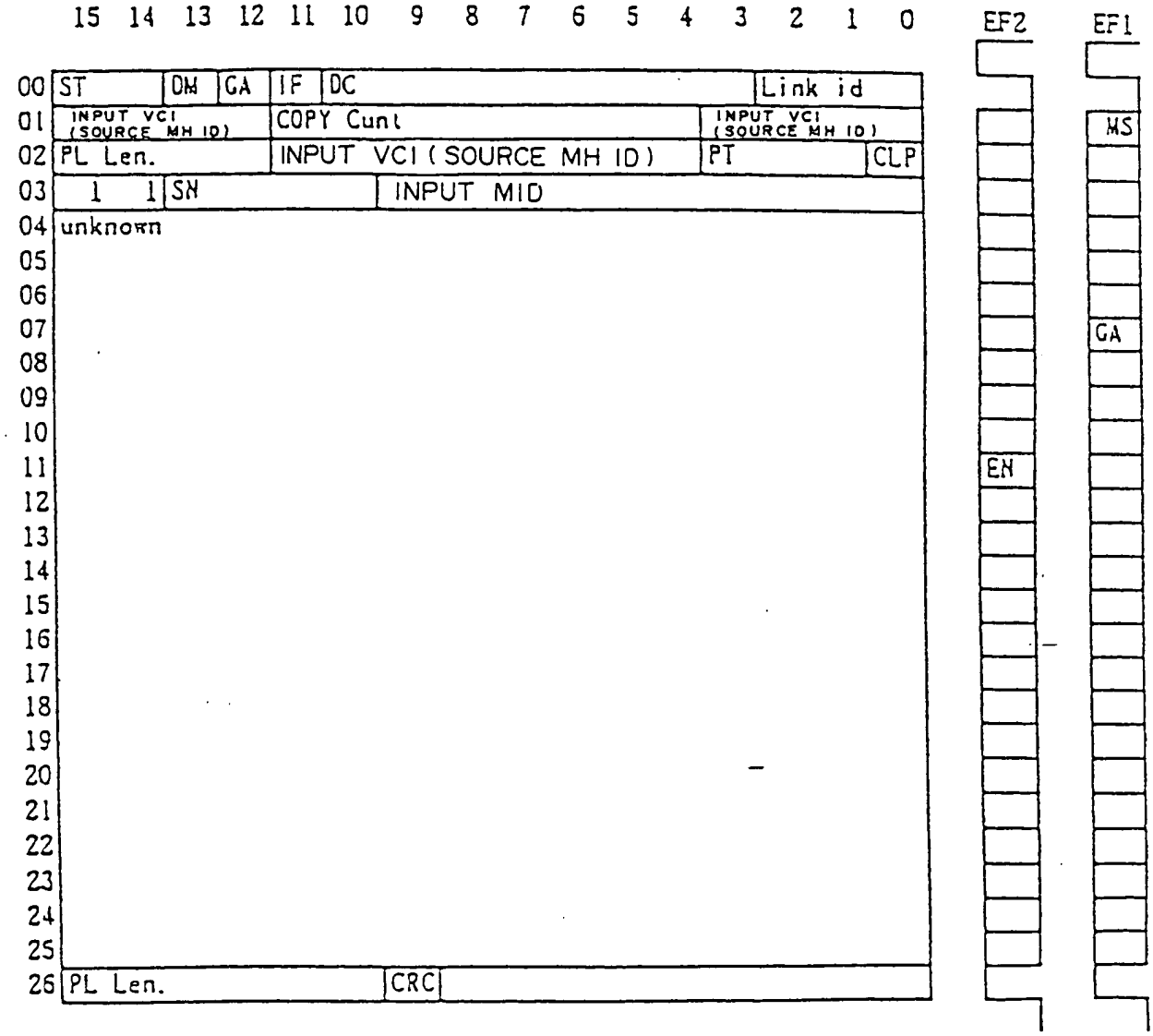


FIG. 607

SIP BOM CELL

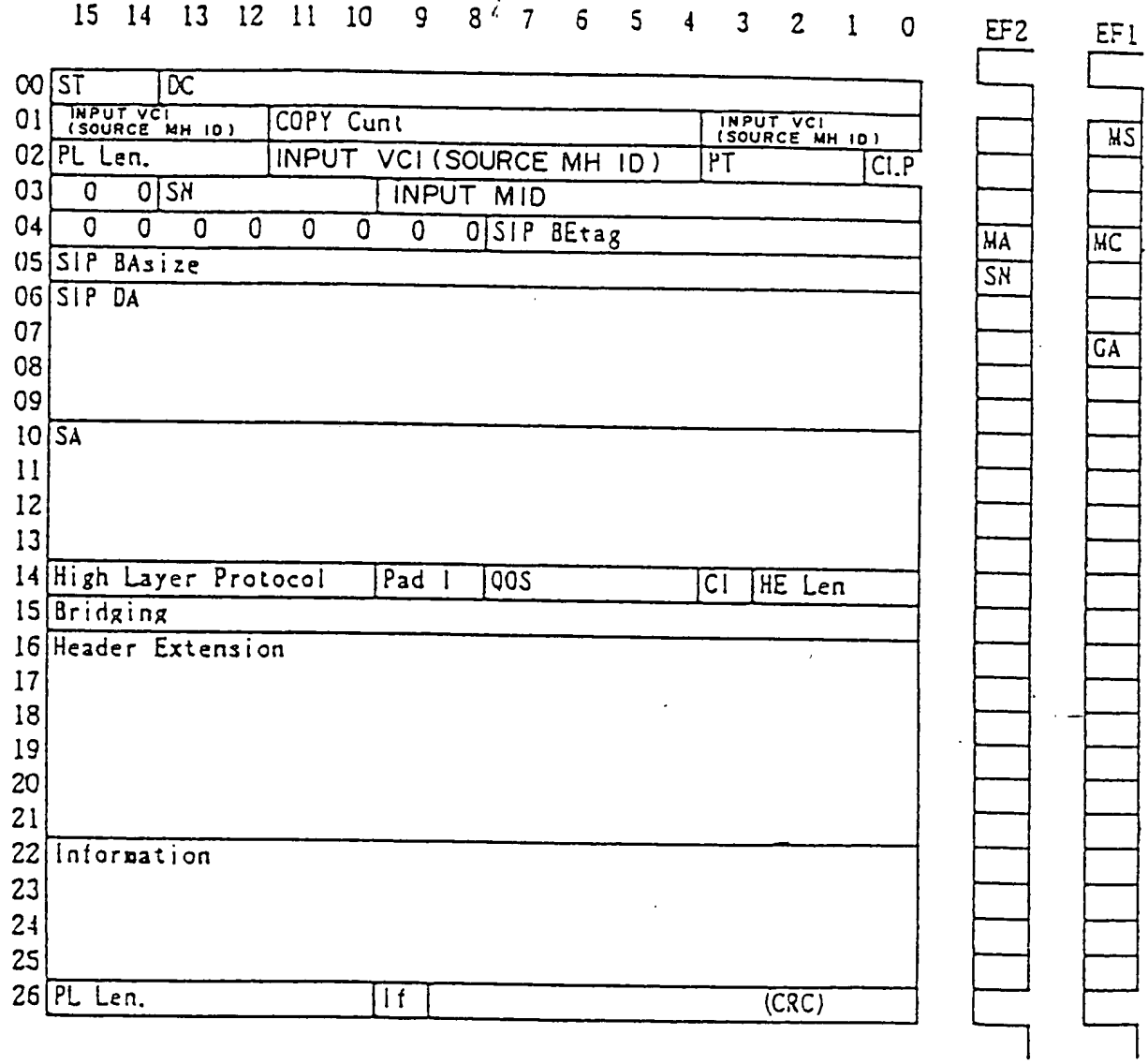


FIG. 608

SIP SSM CELL

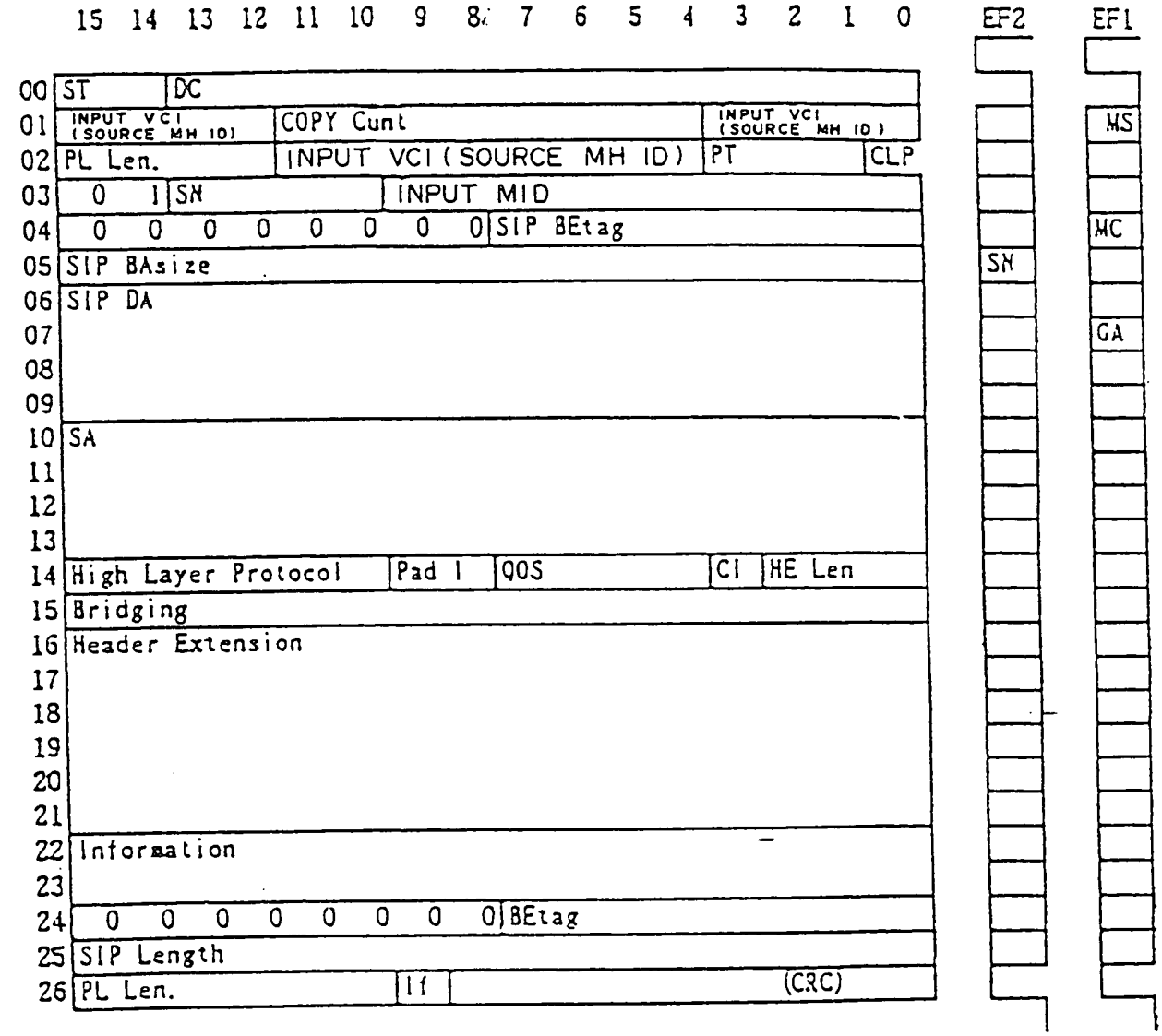


FIG. 609

SIP COM CELL

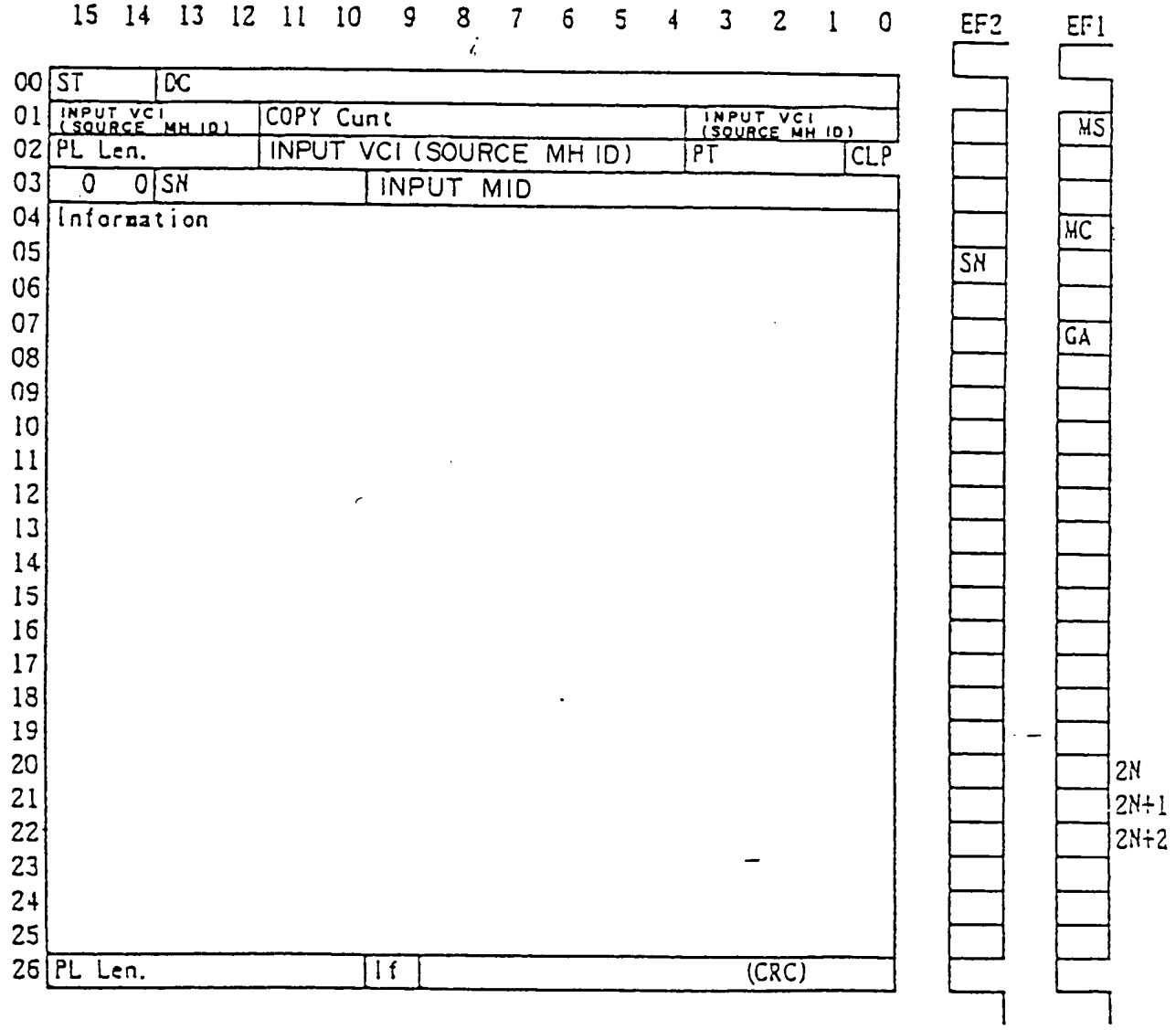


FIG. 610

SIP EOM (Inter-MH EOM) CELL

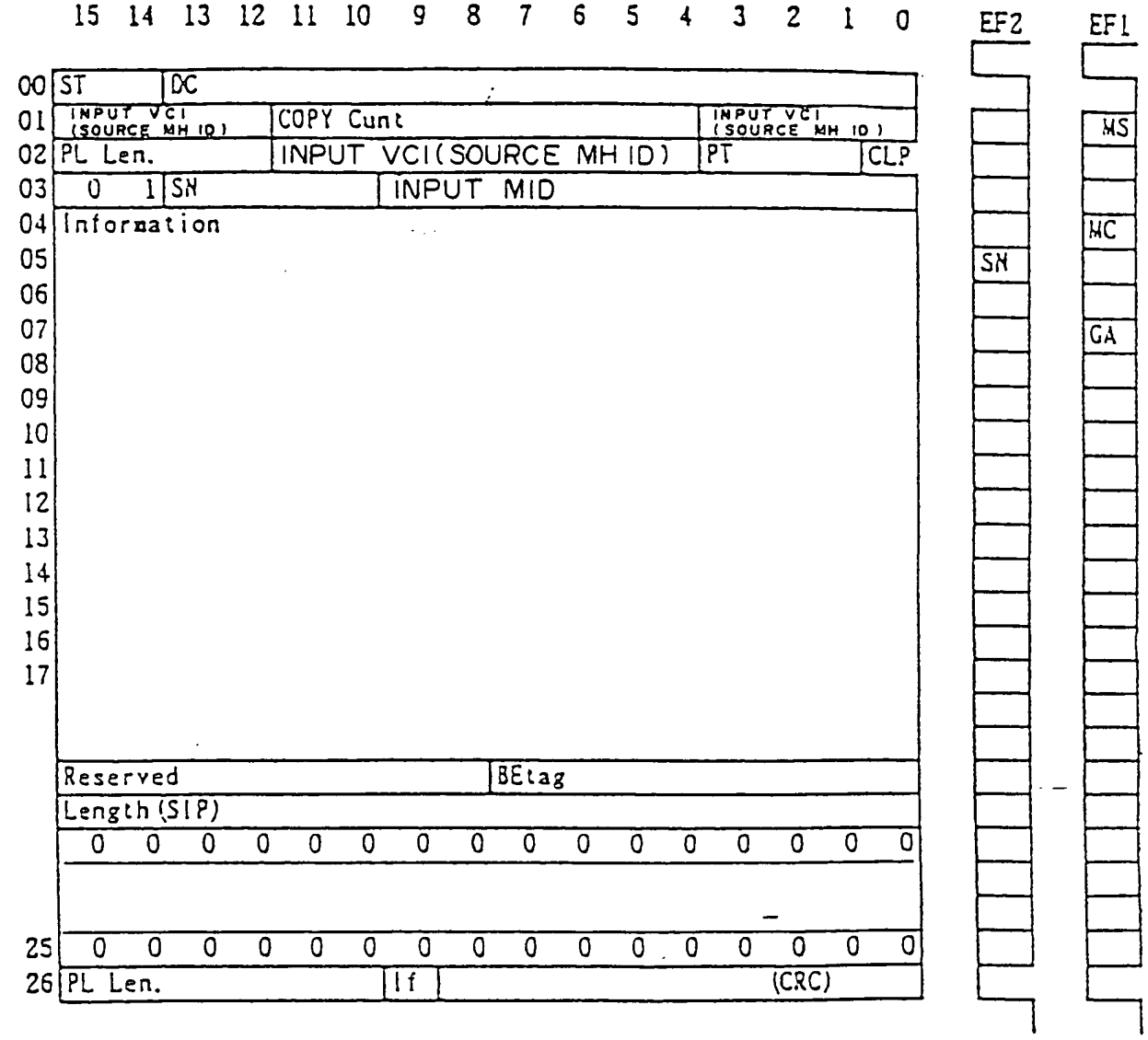


FIG. 611

DATA INTERFACE BETWEEN OGLP AND LPCOM

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	ST		DM	GA	IF	DC									Link id	
01	INPUT VCI (SOURCE MH ID)				COPY Count										INPUT VCI (SOURCE MH ID)	
02	PL Len.								Link id						PT	CLP
03	SST		SN				OUTPUT MID									
04	0	0	0	0	0	0	0	0	ISSIP BEtag							
05	ISSIP BAsize															
06	ISSIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	Service type															
15																
16	Header Extension															
17																
18																
19																
20																
21																
22	Ingress Interface Type								ES	Hop Count Ind*						
23	Carrier															
24	Incominng Network ID															
25	Incoming ICI Transmission Path Set															
26	PL Len.						If									(CRC)

*VALID ONLY WHEN INPUT INTERFACE TO SS OF HOME SYSTEM IS ISSI AND IF BIT IS 0.

EF2		EF1	
MT	MRI time out	MS	master
MA	MID active error	MC	COM MID active error
SN	Invalid sequene number		
LC	ILEC/IC Unavailable	GA	GA active error
EM	Exceed Max Numver of CDU	ED	CDU Active Error
		GB	GA bit error
EN	Encapsulation Error		

FIG. 612

INTER-MH BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	EF2	EF1
00	ST		DM	GA	IF	DC									Link id			
01	INPUT VCI (SOURCE MH ID)				COPY Count										INPUT VCI (SOURCE MH ID)		MT	MS
02	PL Len.										Link id			PT		CLP		
03	1	0	SN						OUTPUT MID									
04	0	0	0	0	0	0	0	0	ISSIP BEtag								MA	
05	ISSIP BAsize																	
06	ISSIP DA																LC	
07																		GA
08																	EM	
09																		GB
10	SA																	
11																		
12																		
13																		
14	Service type																	
15																		
16	Header Extension																	
17																		
18																		
19																		
20																		
21																		
22	Ingress Interface Type								ES	Hop Count Ind								
23	Carrier																	
24	Incominng Network ID																	
25	Incoming ICI Transmission Path Set																	
26	PL Len.							If	(CRC)									

· VALID ONLY WHEN INPUT INTERFACE TO SS OF HOME SYSTEM IS ISSI AND IF BIT IS 0.

FIG. 613

INTER-MH SSM CELL

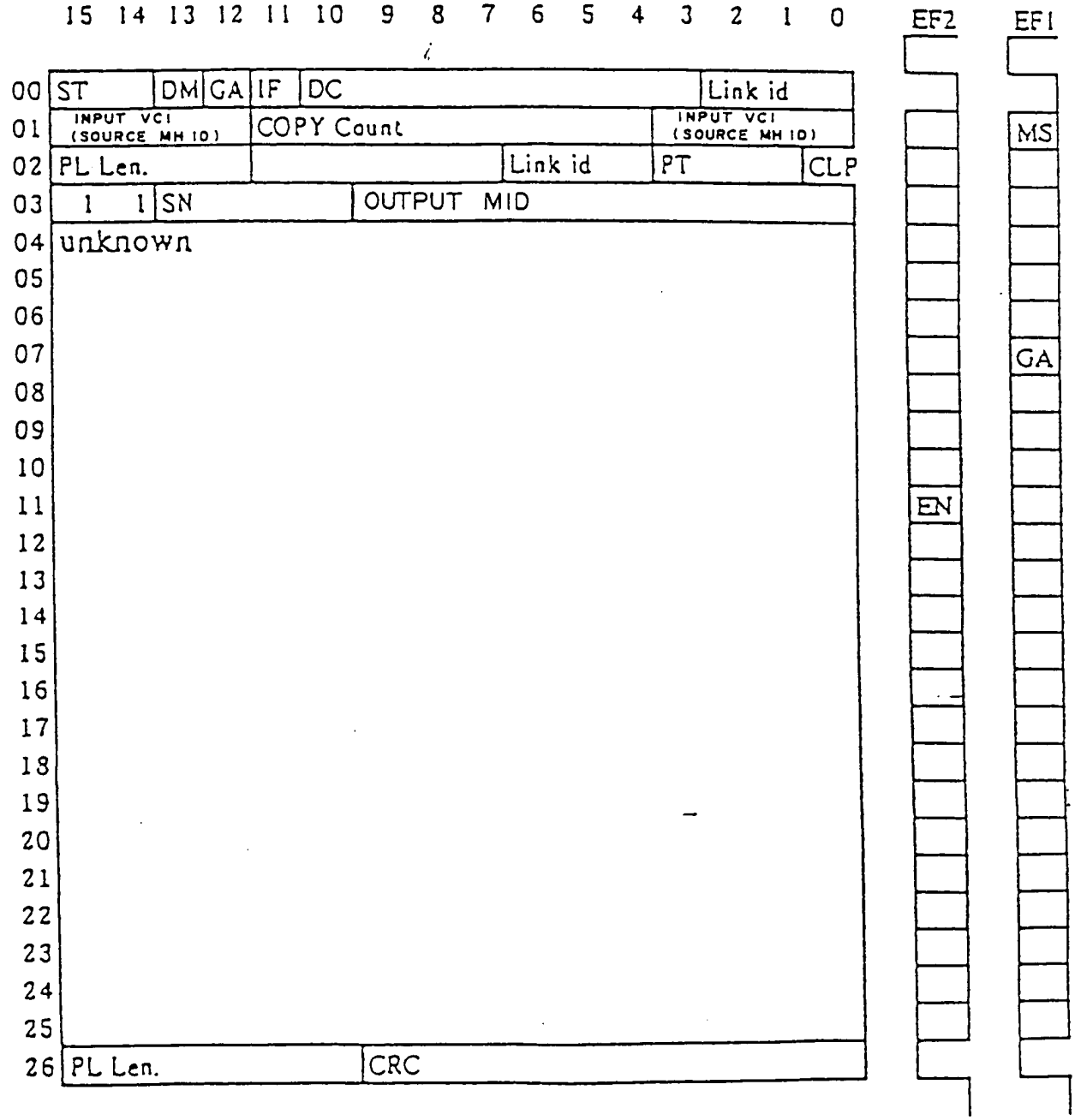


FIG. 614

SIP BOM CELL

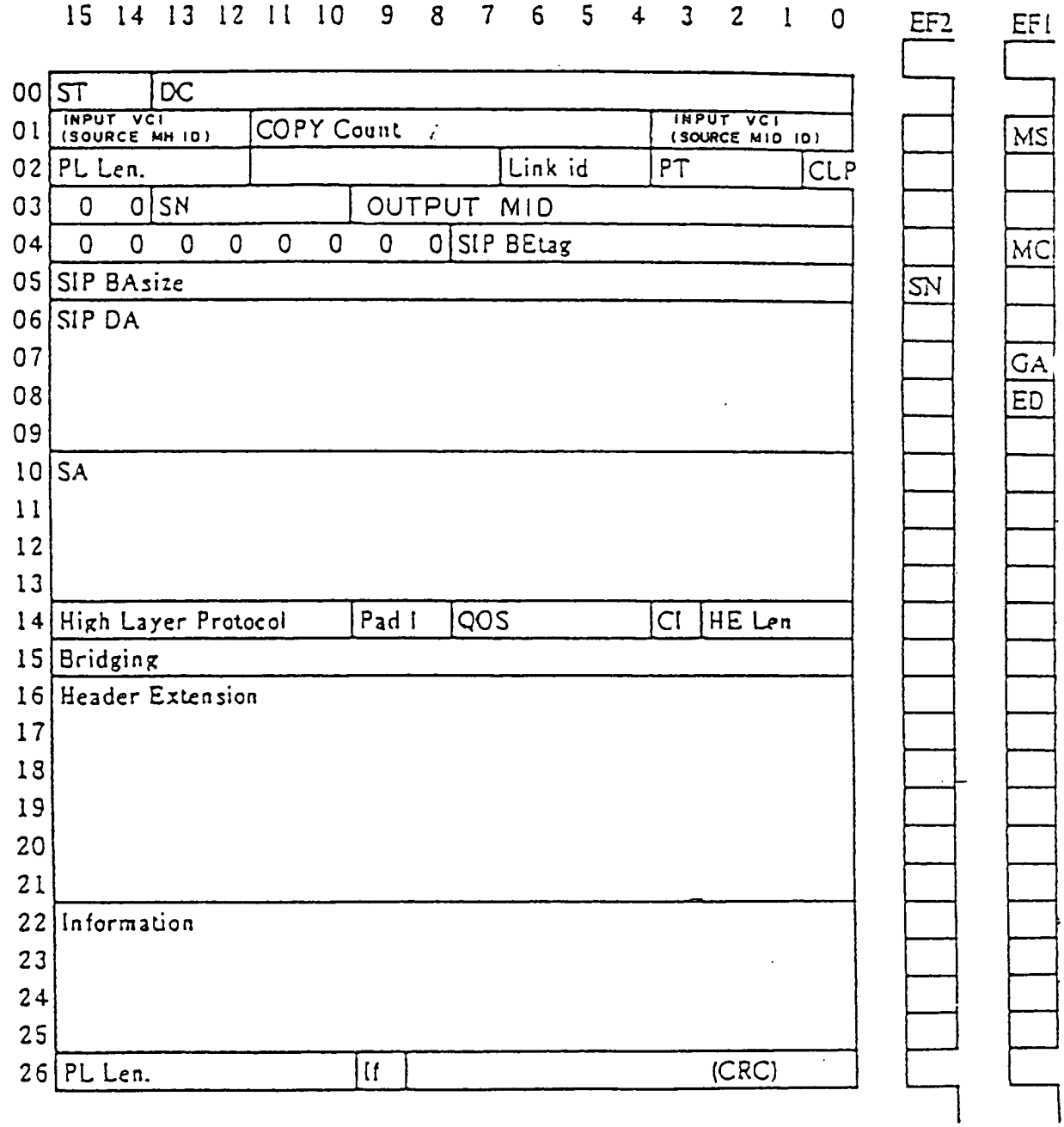


FIG. 615

SIP SSM CELL

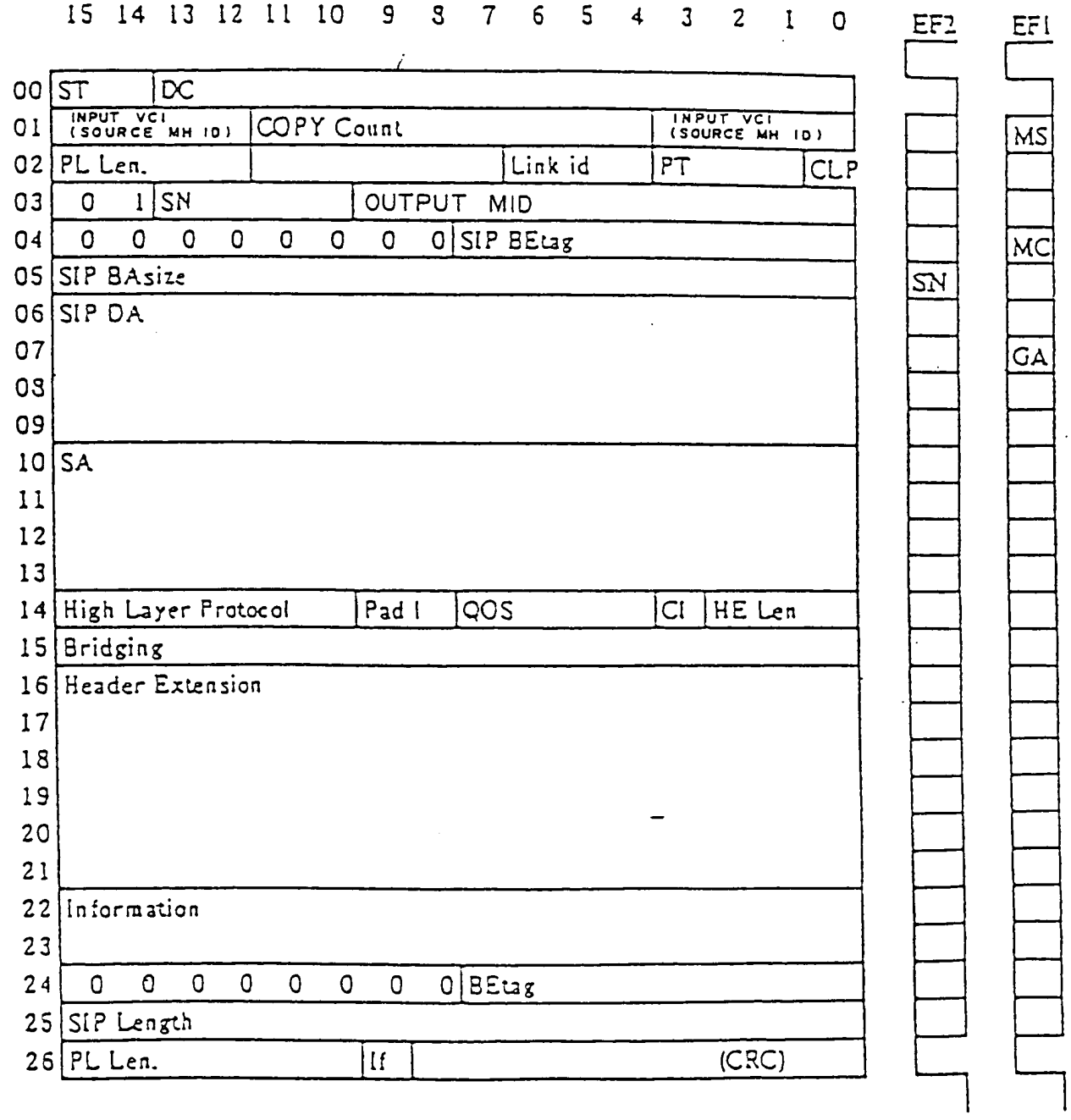


FIG. 616

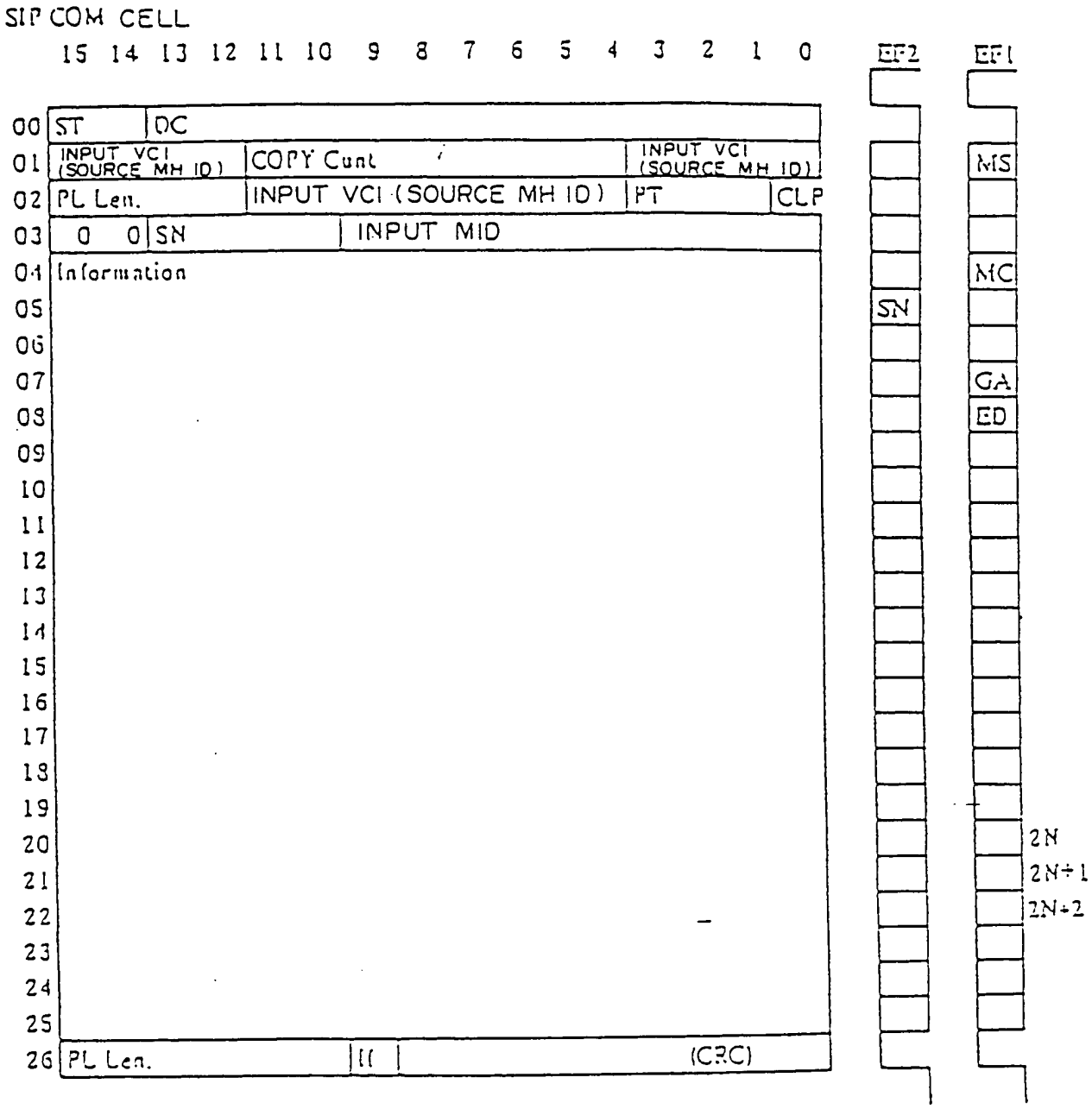

SIP COM CELL
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
EF2
EF1
00 ST DC
01 INPUT VCI (SOURCE MH ID) COPY Cunt INPUT VCI (SOURCE MH ID)
02 PL Len. INPUT VCI (SOURCE MH ID) PT CLP
03 0 0 SN INPUT MID
04 Information
26 PL Len. (CRC)
MS
MC
SN
GA
ED
2N
2N+1
2N+2

FIG. 617

SIP EOM(Inter-MII EOM) CELL

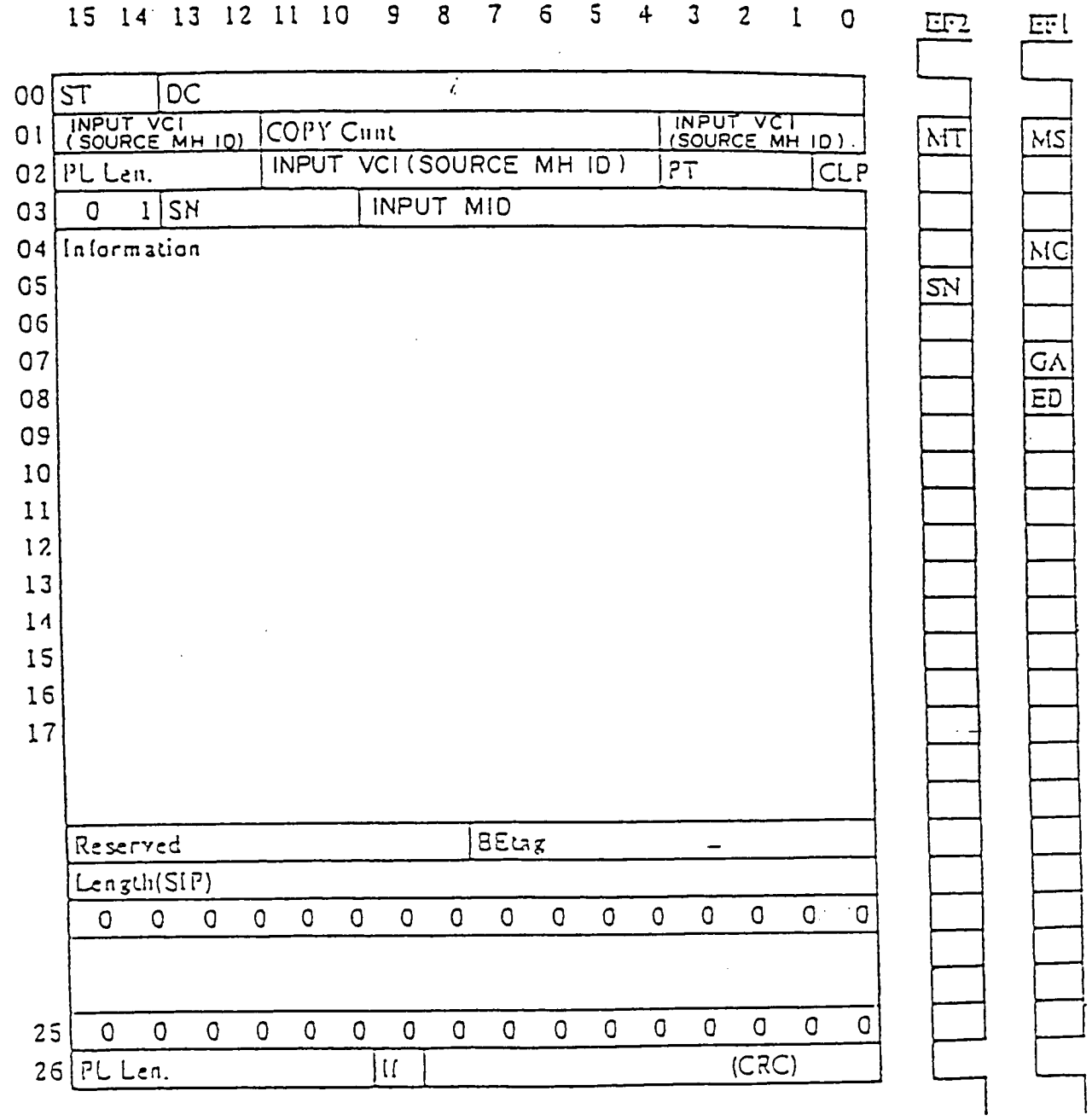


FIG. 618

HMH10 OUTPUT CELL (ICI)

INTER-MH BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	0	Link ID			PT			CLP
03	1	0	SN				0	0	0	MID						
04	0	0	0	0	0	0	0	0	ICIP BEtag							
05	ICI BA size															
06	ICIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	Protocol ID						Pad l		QOS				CI	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	ICIP Version								Carrier							
23									ES	Reserved						
24	Reserved															
25																
26	PL Len.						CRC									

FIG. 619

SIP BOM CELL

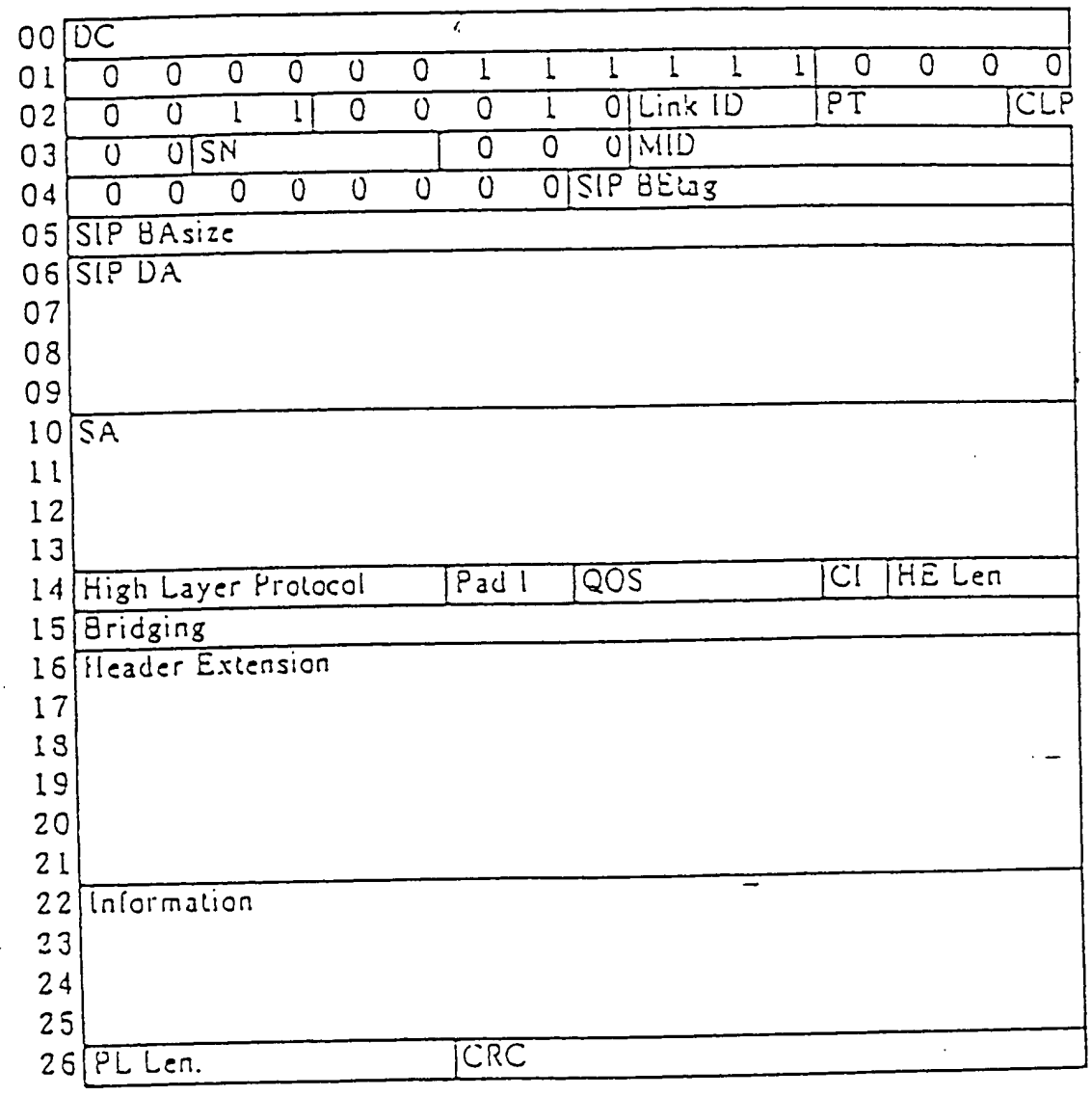


FIG. 620

SIP SSM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	0	Link ID			PT			CLP
03	0	1	SN				0	0	0	MID						
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				CI	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24	0	0	0	0	0	0	0	0	SIP BEtag							
25	SIP Length															
26	PL Len.						CRC									

FIG. 621

SIP COM CELL

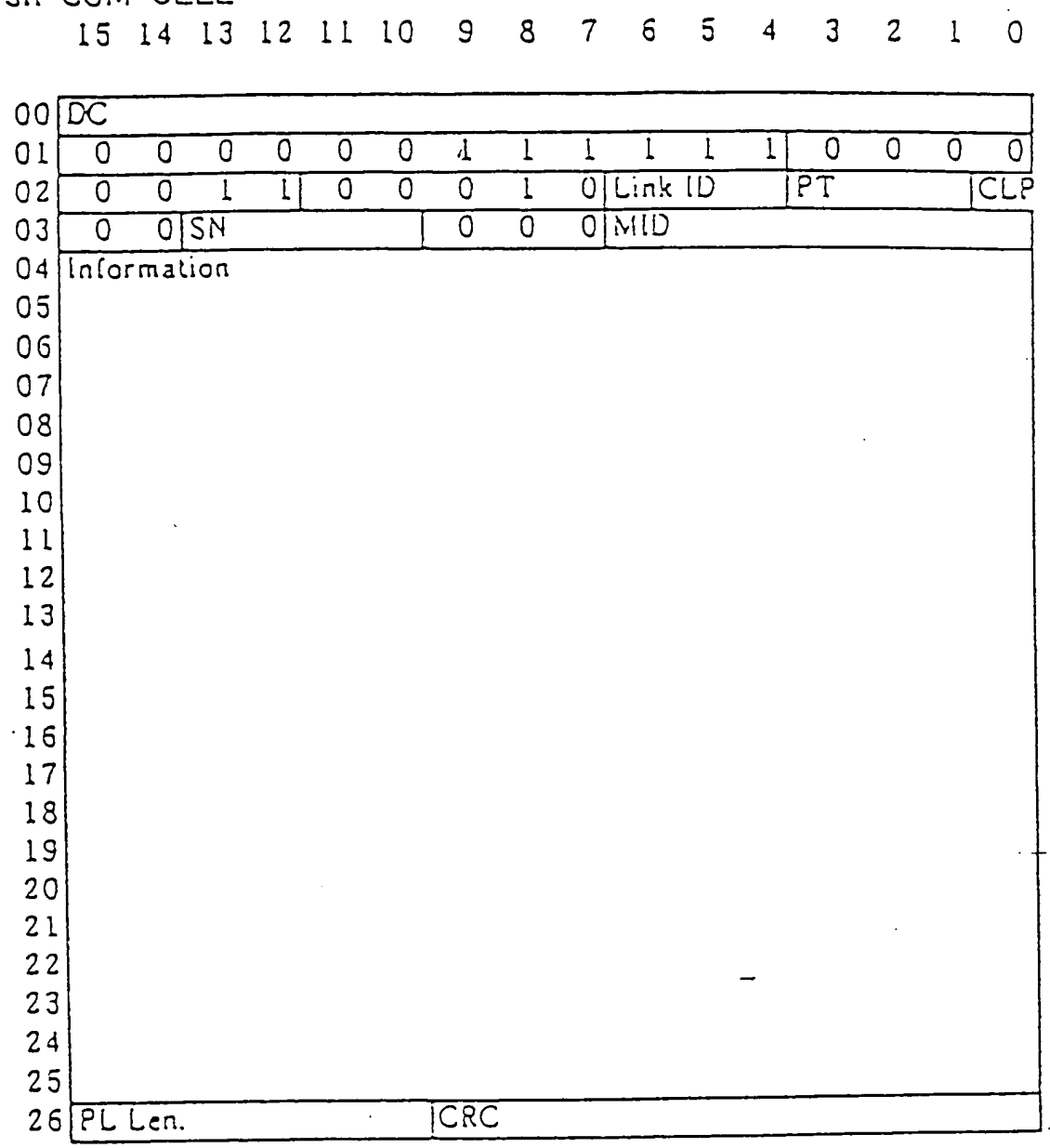


FIG. 622

SIP EOM(Inter-MH EOM) CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	0	Link ID			PT			CLP
03	0	1	SN				0	0	0	MID						
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
2N	Reserved								BEtag							
2N+1	Length(ICIP)															
2N+2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	PL Len.						CRC									

FIG. 623

HMH10 OUTPUT CELL (ISSI)

ISSI-MH BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	0	0	Link ID			PT			CLP
03	1	0	SN						0	0	0	MID				
04	0	0	0	0	0	0	0	0	ISSIP BEtag							
05	ISSI BA size															
06	ISSIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	Service type						Pad 1		Priority			CI	HE Len			
15	Protocol Version								Protool Discriminator							
16	Header Extension															
17																
18																
19																
20																
21																
22	Ingress IntLType								Carrier							
23									ES	Hop Count Ind						
24	Incoming Network ID															
25	Incoming ICI TPS ID															
26	PL Len.						CRC									

FIG. 624

SIP BOM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	0	0	Link ID			PT			CLP
03	0	0	SN				0	0	0	MID						
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				CI	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	PL Len.						CRC									

FIG. 625

SIP SSM CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	0	0	Link ID			PT			CLP
03	0	1	SN				0	0	0	MID						
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				CI	HE Len		
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24	0	0	0	0	0	0	0	0	ISSIP BEtag							
25	ISSIP Length															
26	PL Len.						CRC									

FIG. 626

SIP COM CELL

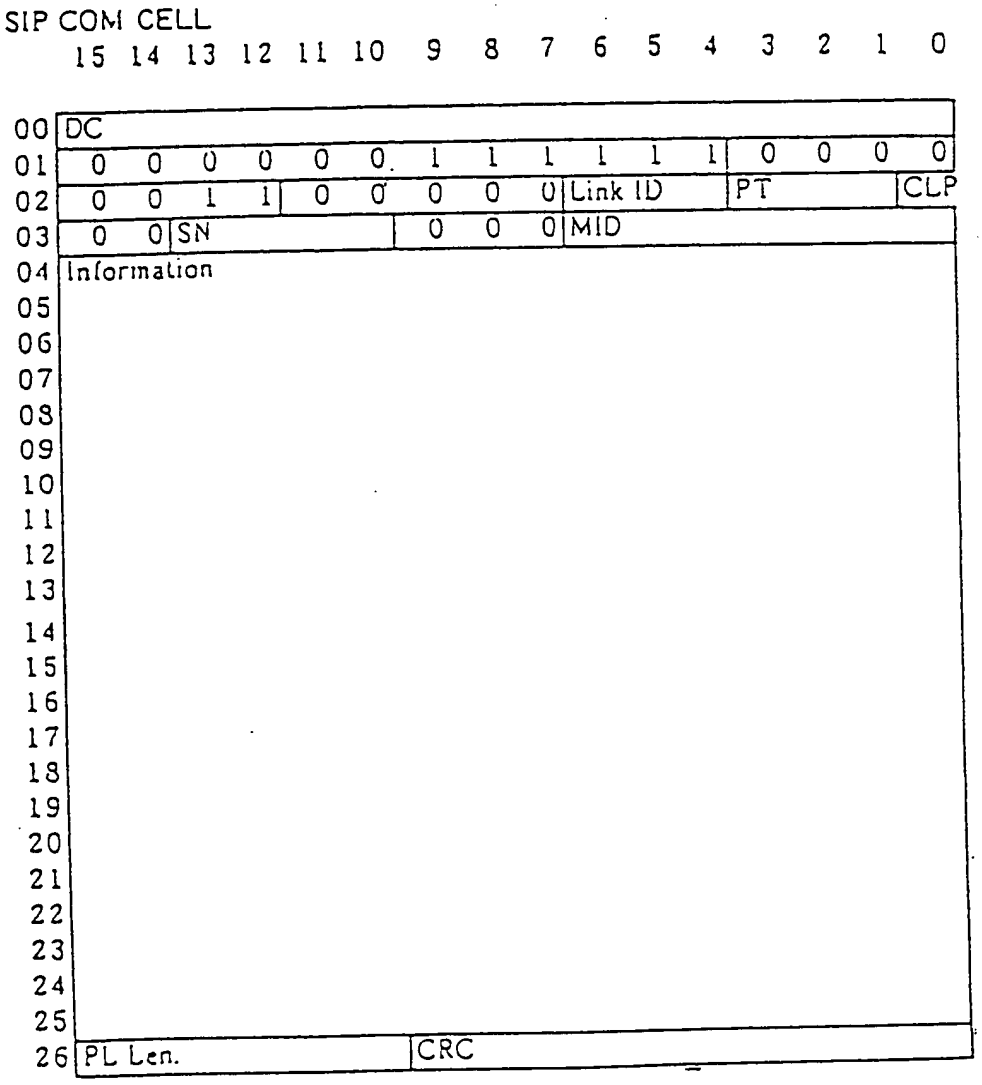


FIG. 627

SIP EOM(Inter-MH EOM) CELL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	0	0	Link ID			PT			CLP
03	0	1	SN				0	0	0	MID						
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
2N	Reserved								BEtag							
2N+1	Length(ISSIP)															
2N+2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	PL Len.						CRC									

FIG. 628

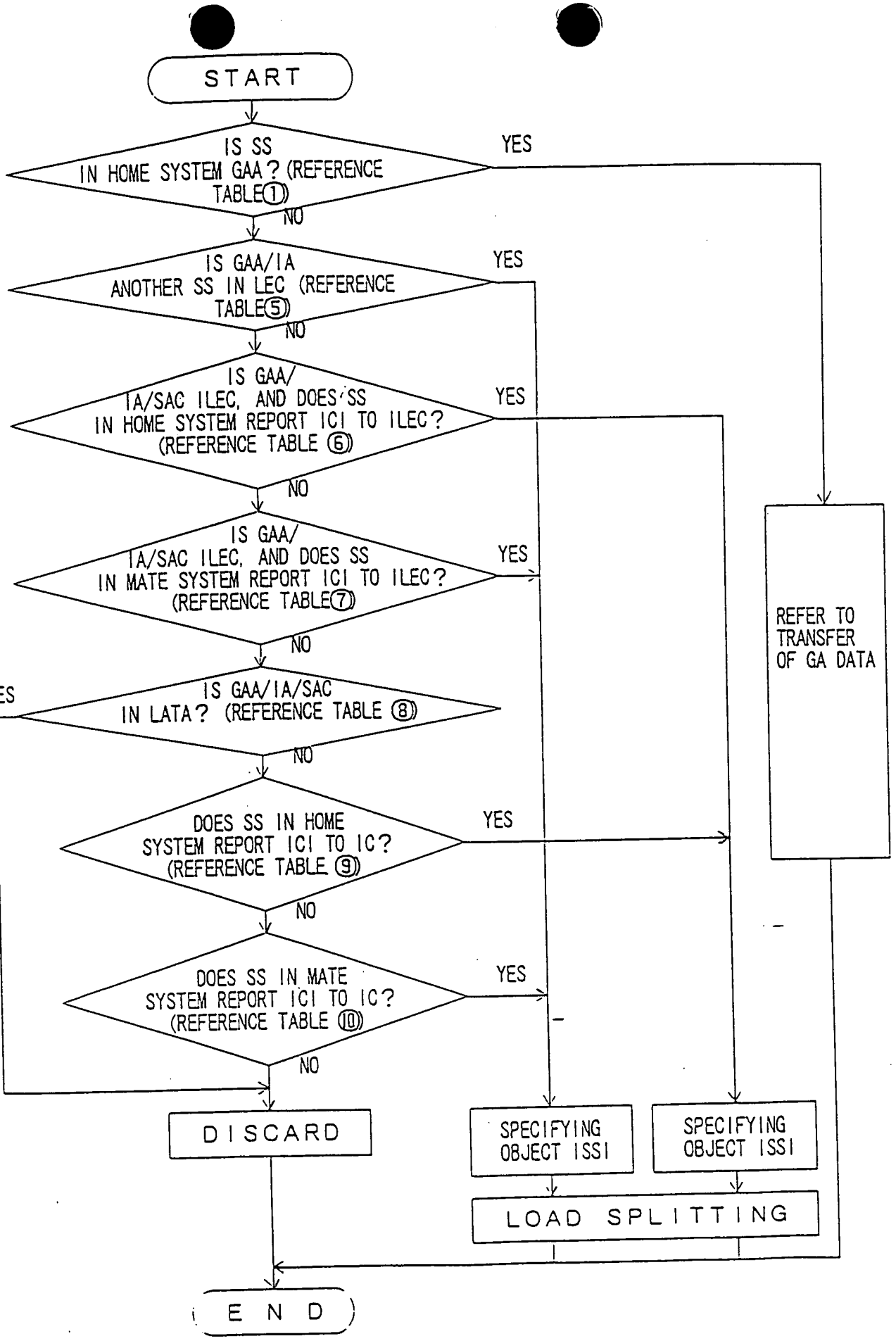

START
IS SS IN HOME SYSTEM GAA? (REFERENCE TABLE①)
YES
NO
IS GAA/IA ANOTHER SS IN LEC (REFERENCE TABLE⑤)
YES
NO
IS GAA/ IA/SAC ILEC, AND DOES SS IN HOME SYSTEM REPORT ICI TO ILEC? (REFERENCE TABLE ⑥)
YES
NO
IS GAA/ IA/SAC ILEC, AND DOES SS IN MATE SYSTEM REPORT ICI TO ILEC? (REFERENCE TABLE⑦)
YES
NO
IS GAA/IA/SAC IN LATA? (REFERENCE TABLE ⑧)
YES
NO
DOES SS IN HOME SYSTEM REPORT ICI TO IC? (REFERENCE TABLE ⑨)
YES
NO
DOES SS IN MATE SYSTEM REPORT ICI TO IC? (REFERENCE TABLE ⑩)
YES
NO
REFER TO TRANSFER OF GA DATA
DISCARD
SPECIFYING OBJECT ISSI
SPECIFYING OBJECT ISSI
LOAD SPLITTING
END

FIG. 629

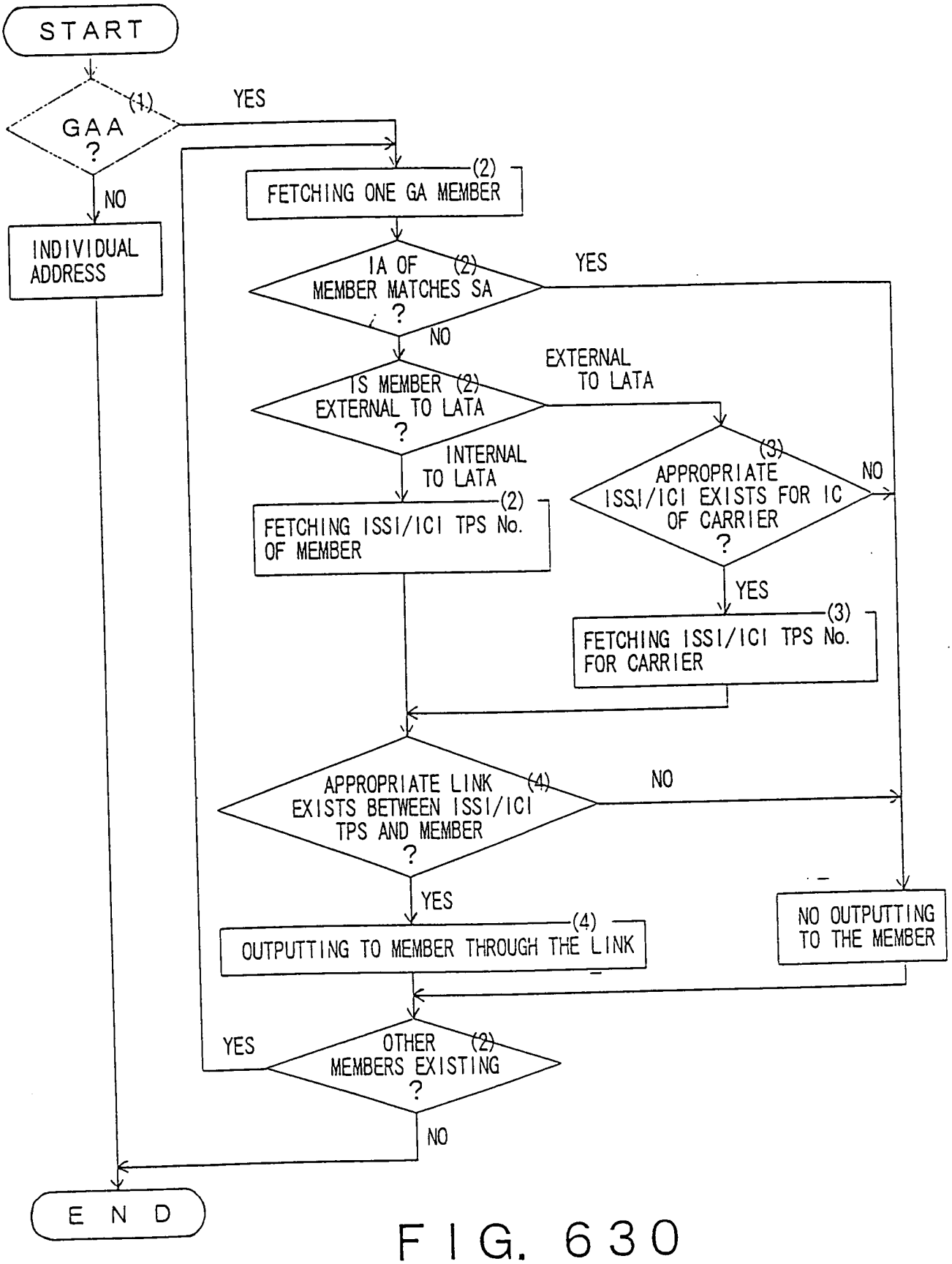

START
GAA ?
(1)
YES
NO
INDIVIDUAL ADDRESS
(2)
FETCHING ONE GA MEMBER
IA OF MEMBER MATCHES SA ?
(2)
YES
NO
IS MEMBER EXTERNAL TO LATA ?
(2)
EXTERNAL TO LATA
INTERNAL TO LATA
(2)
FETCHING ISSI/ICI TPS No. OF MEMBER
(3)
APPROPRIATE ISSI/ICI EXISTS FOR IC OF CARRIER ?
NO
YES
(3)
FETCHING ISSI/ICI TPS No. FOR CARRIER
APPROPRIATE LINK EXISTS BETWEEN ISSI/ICI TPS AND MEMBER ?
(4)
NO
YES
(4)
OUTPUTTING TO MEMBER THROUGH THE LINK
NO OUTPUTTING TO THE MEMBER
YES
OTHER MEMBERS EXISTING ?
(2)
NO
END

FIG. 630

① DETERMINING WHETHER OR NOT SS IN HOME SYSTEM "GAA" ACCORDING TO GAA LIST.

	GAA (64 bit)	GA ID (10 bit)
1024 (W)	.....	.....

② COPYING WHILE ASSIGNING GA-SUPPORTED IA, ISSI/ICI No., GA MEMBER ID, AND FLAG FOR OUTSIDE OF LATA.

	GA ID (10bit)	IA (64 bit)	ISSI/ICI No. (3 bit)	GA MEMBER ID (6 bit)	OUTSIDE LATA (1 bit)
1024 (W)	.....	.....	.....	.....	.....

③ ASSIGNING CARRIER BY REFERRING TO TABLE BELOW WHEN OUTSIDE-OF-LATA FLAG IS SET AFTER COPYING GA.

	SMDS CIC(16 bit)	ISSI/ICI No. (3bit)
256 (W)	.....	.....

④ DETERMINING WHETHER OR NOT SPECIFIED LINK IS SUPPORTED BY MESH OF HOME SYSTEM ACCORDING TO TABLE BELOW.

	ISSI/ICI No. (3 bit)	GA MEMBER ID (6 bit)	LINK (3 bit)
256 (W)	.....	.....	.....

FIG. 631

⑤ IT IS DETERMINED ACCORDING TO THE GAA/IA STATION NUMBER IN THE LEC WHETHER OR NOT GAA/IA IS ANOTHER SS IN THE LEC.

INSIDE LEC GAA STATION NUMBER (32bit)	ISSI No. (3bit)
.....	.....
INSIDE LEC IA STATION NUMBER (32bit)	ISSI No. (3bit)
.....	.....

⑥ IT IS DETERMINED ACCORDING TO THE GAA/IA/SAC STATION NUMBER IN THE LEC WHETEHR OR NOT GAA/IA/SAC REFERS TO THE ILEC AND THE ICI TO THE ILEC IS SUPPROTED BY THE SS IN THE HOME SYSTEM.

INSIDE ILEC GAA STATION NUMBER (32bit)	ICI No. (3bit)
.....	.....
INSIDE ILEC IA STATION NUMBER (32bit)	ICI No. (3bit)
.....	.....
INSIDE ILEC SAC STATION NUMBER (32bit)	ICI No. (3bit)
.....	.....

⑦ IT IS DETERMINED ACCORDING TO THE GAA/IA/SAC STATION NUMBER IN THE LEC WHETHER OR NOT GAA/IA/SAC REFERS TO THE ILEC AND THE ICI TO THE ILEC IS SUPPORTED BY THE SS IN THE MATE SYSTEM.

INSIDE ILEC GAA STATION NUMBER (32bit)	ISSI No. (3bit)
.....	.....
INSIDE ILEC IA STATION NUMBER (32bit)	ISSI No. (3bit)
.....	.....
INSIDE ILEC SAC STATION NUMBER (32bit)	ISSI No. (3bit)
.....	.....

⑧ IT IS DETERMINED ACCORDING TO THE GAA/IA/SAC STATION NUMBER IN THE LATA WHTHER OR NOT STATION NUMBER OF LATA IS REFERRED TO.

INSIDE LATA GAA STATION NUMBER (32bit)
.....
INSIDE LATA IA STATION NUMBER (32bit)
.....
INSIDE LATA SAG STATION NUMBER (32bit)
.....

TOTAL STATION NUMBER OF TABLES ⑤~⑧ IS 512

FIG. 632

⑨ IT IS DETERMINED WHETHER OR NOT ICI FROM SMDS CIC TO IC IS SUPPORTED BY SS OF HOME SYSTEM.

SMDS CIC (16BIT)	ICI No. (3 BIT)
.....	.....

⑩ IT IS DETERMINED WHETHER OR NOT ICI FROM SMDS CIC TO IC IS SUPPORTED BY SS OF MATE SYSTEM.

SMDS CIC (16BIT)	ISSI No. (3 BIT)
.....	.....

A TOTAL OF 256 CARRIERS ARE SPECIFIED FOR⑫ AND ⑬

FIG. 633

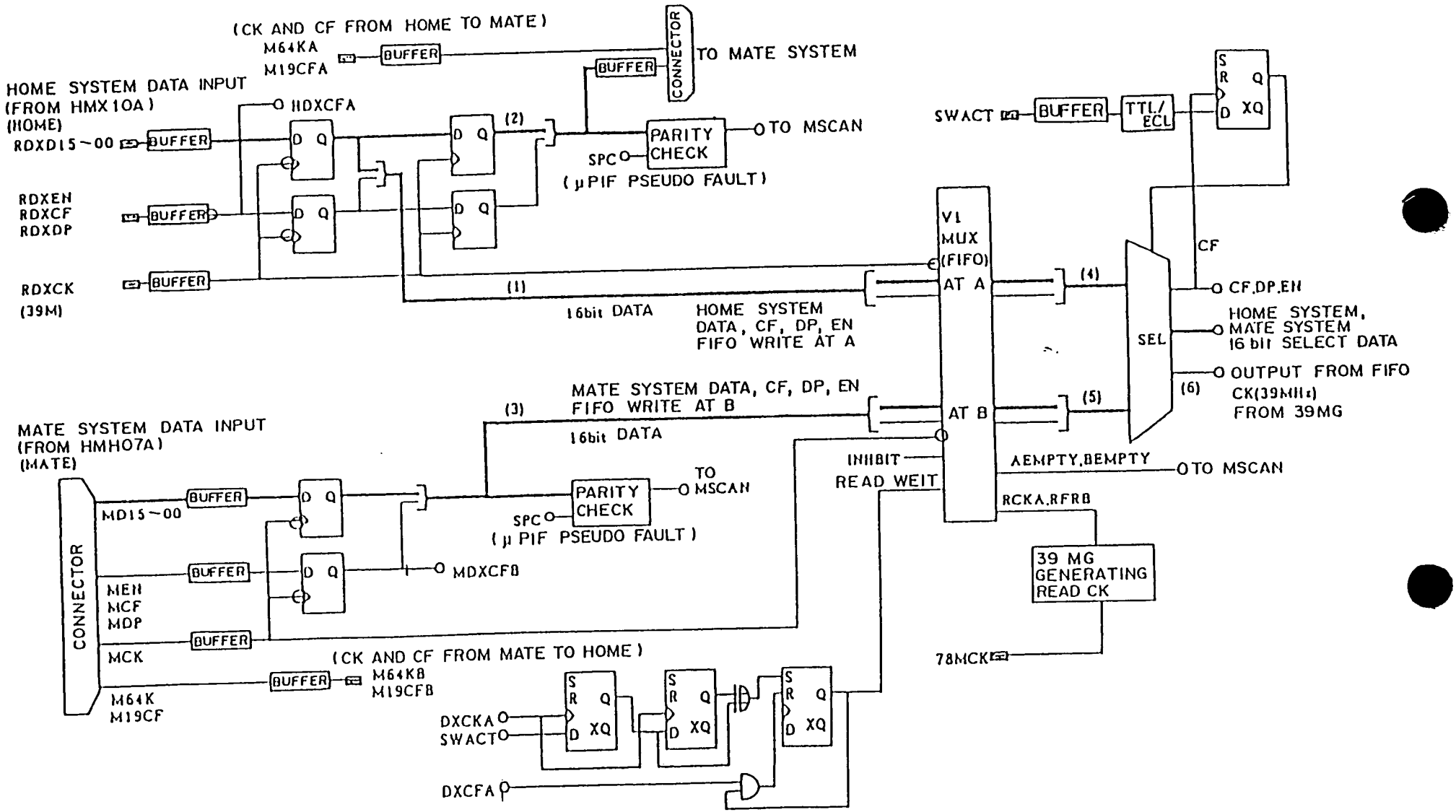

(CK AND CF FROM HOME TO MATE)
M64KA
M19CFA
BUFFER
CONNECTOR
TO MATE SYSTEM
HOME SYSTEM DATA INPUT
(FROM HMX10A)
(HOME)
RDXD15~00
RDXEN
RDXCF
RDXDP
RDXCK
(39M)
IIDXCFA
D Q
(2)
PARITY CHECK
SPC
(μPIF PSEUDO FAULT)
TO MSCAN
(1)
16bit DATA
HOME SYSTEM DATA, CF, DP, EN FIFO WRITE AT A
SWACT
TTL/ ECL
S R Q D XQ
VL MUX (FIFO)
AT A
AT B
(4)
(5)
(6)
SEL
CF
CF.DP.EN
HOME SYSTEM, MATE SYSTEM 16 bit SELECT DATA
OUTPUT FROM FIFO CK(39MHz) FROM 39MG
MATE SYSTEM DATA, CF, DP, EN FIFO WRITE AT B
(3)
16bit DATA
MATE SYSTEM DATA INPUT
(FROM HMH07A)
(MATE)
CONNECTOR
MD15~00
MEN
MCF
MDP
MCK
M64K
M19CF
MDXCFB
INHIBIT
READ WEIT
AEMPTY,BEMPTY
RCKA,RFRB
39 MG GENERATING READ CK
78MCK
(CK AND CF FROM MATE TO HOME)
M64KB
M19CFB
DXCKA
SWACT
DXCFA

FIG. 634

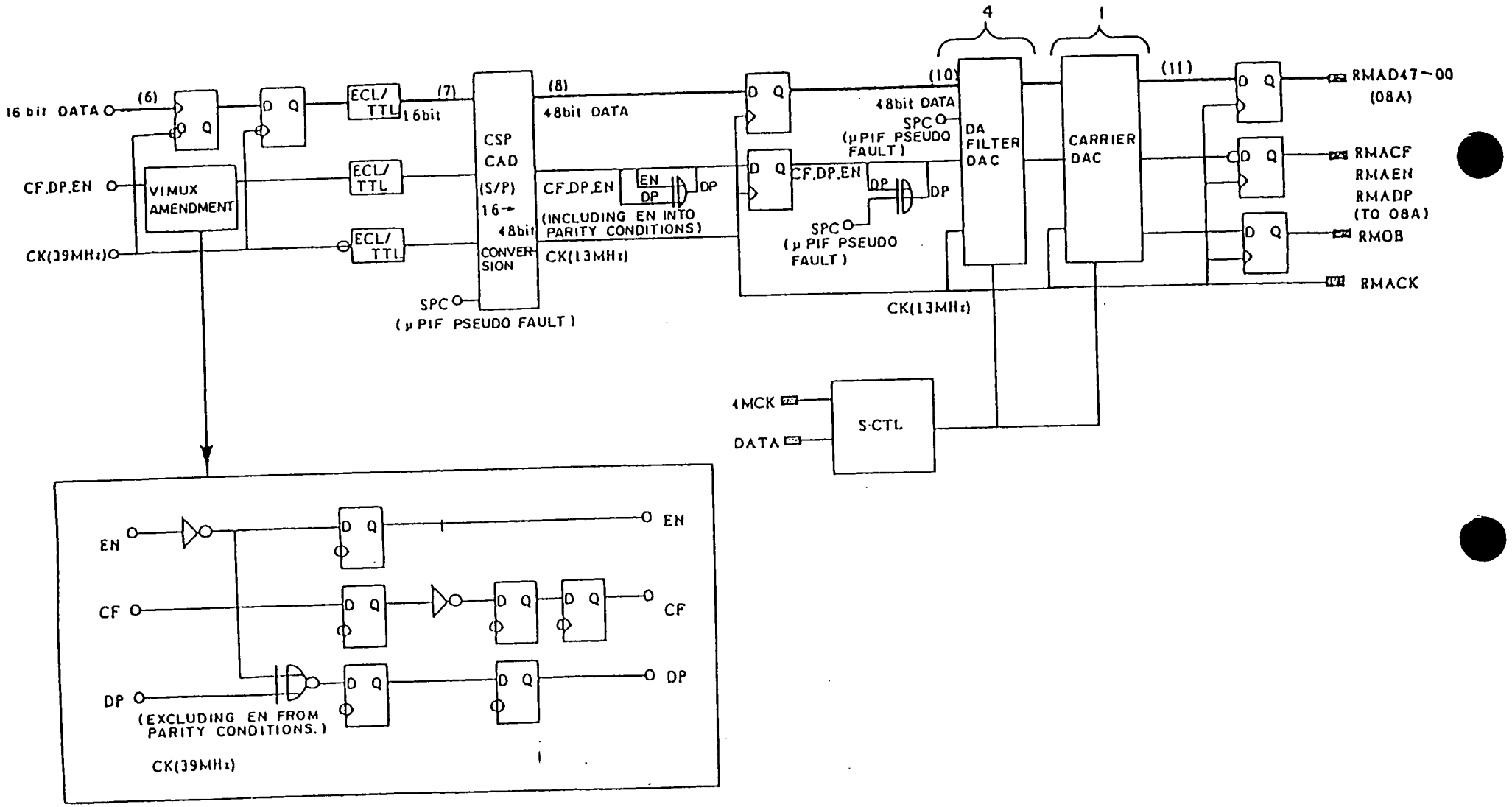
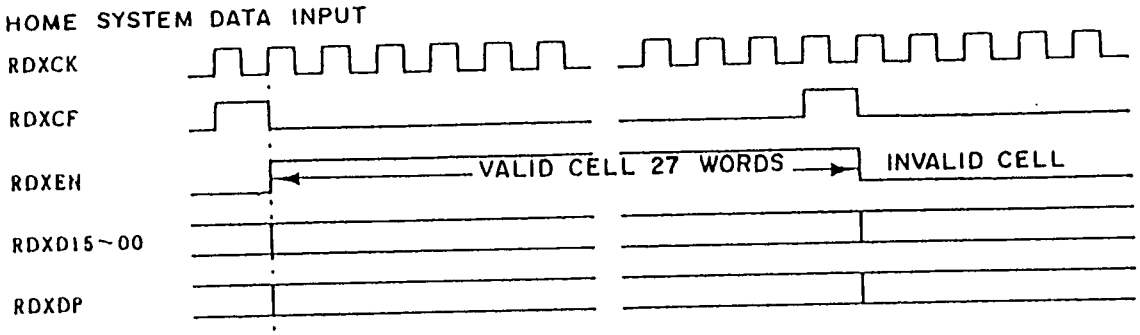
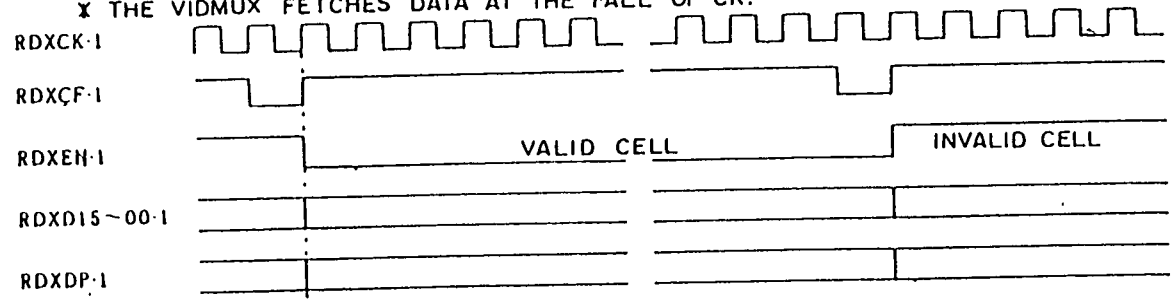

16 bit DATA
(6)
CF.DP.EN
VIMUX AMENDMENT
CK(39MHz)
ECL/TTL
16bit
(7)
CSP CAD
(S/P)
16→48bit
CONVERSION
SPC
(μPIF PSEUDO FAULT)
(8)
48bit DATA
CF.DP.EN
EN
DP
(INCLUDING EN INTO PARITY CONDITIONS)
CK(13MHz)
(10)
48bit DATA
SPC
(μPIF PSEUDO FAULT)
DA FILTER DAC
4
CARRIER DAC
1
(11)
RMAD47~00
(08A)
RMACF
RMAEN
RMADP
(TO 08A)
RMOB
RMACK
4MCK
DATA
S-CTL
EN
CF
DP
(EXCLUDING EN FROM PARITY CONDITIONS.)
CK(39MHz)

FIG. 635



(1) HOME SYSTEM DATA (CF, EN, AND DP ARE INVERTED IN THE INPUT BUFFER) IS PROCESSED BY INVERTING THE RDXCK AND FETCHED TO THE VIMUX (FIFO) USING THE CK.
※ THE VIDMUX FETCHES DATA AT THE FALL OF CK.



(2) (1) DATA IS PROCESSED BY THE RDXCK, PARITY-CHECKED, AND PASSED TO A MATE SYSTEM

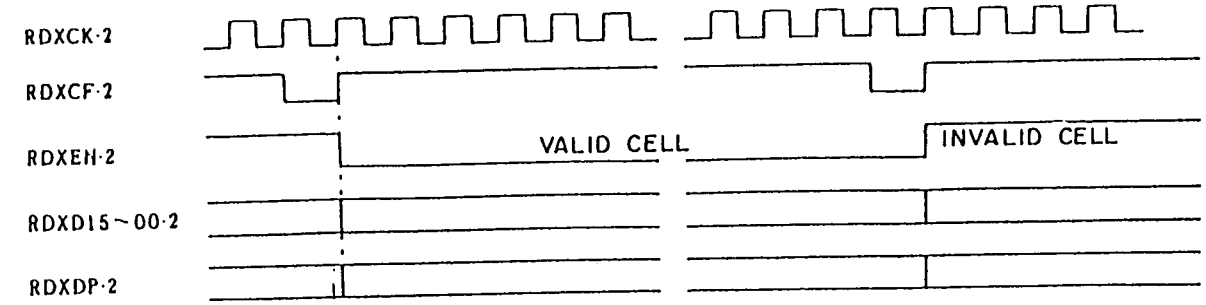


FIG. 636

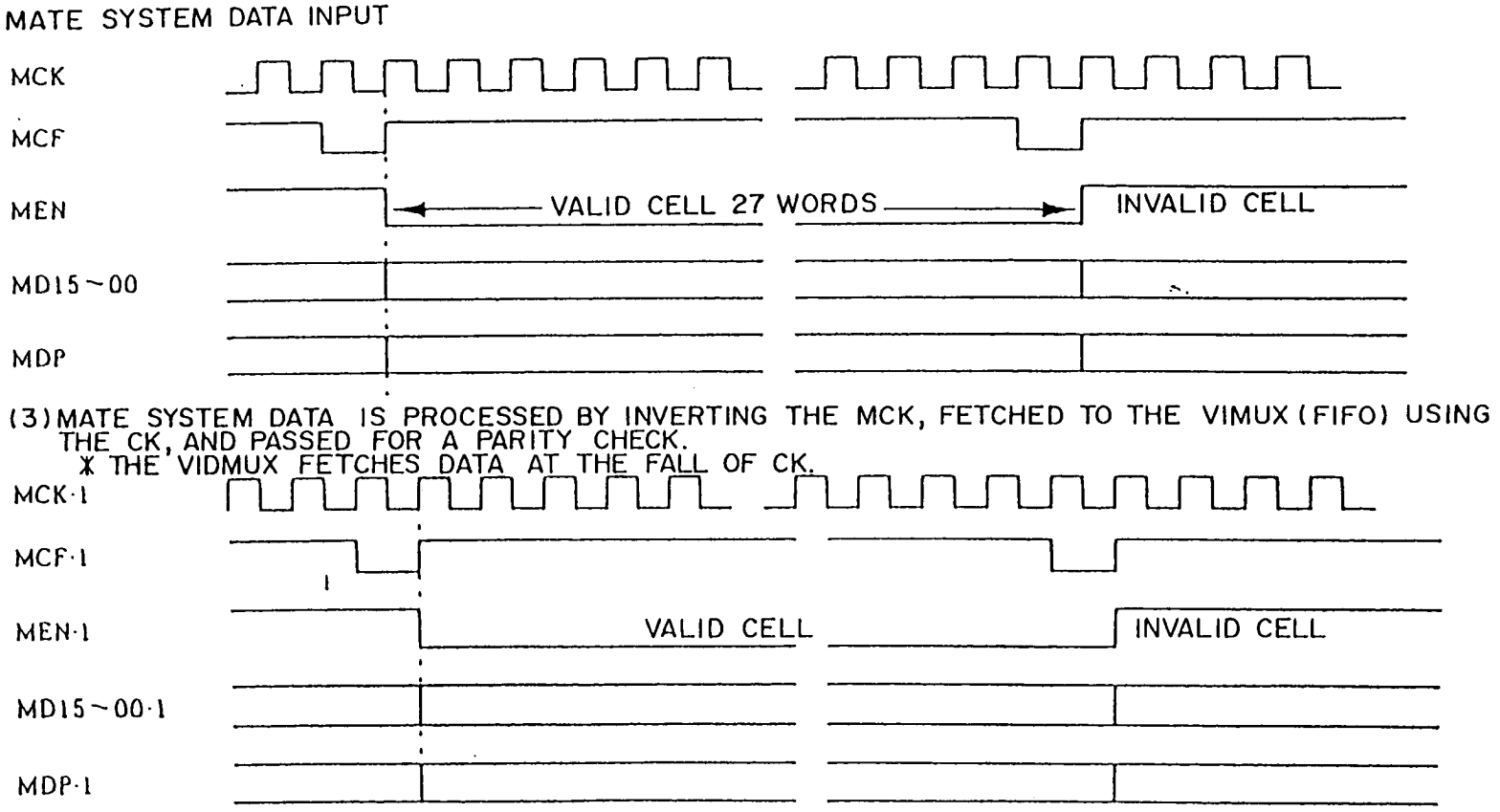

MATE SYSTEM DATA INPUT
MCK
MCF
MEN
VALID CELL 27 WORDS
INVALID CELL
MD15~00
MDP
(3) MATE SYSTEM DATA IS PROCESSED BY INVERTING THE MCK, FETCHED TO THE VIMUX (FIFO) USING THE CK, AND PASSED FOR A PARITY CHECK.
※ THE VIDMUX FETCHES DATA AT THE FALL OF CK.
MCK·1
MCF·1
MEN·1
VALID CELL
INVALID CELL
MD15~00·1
MDP·1

FIG. 637

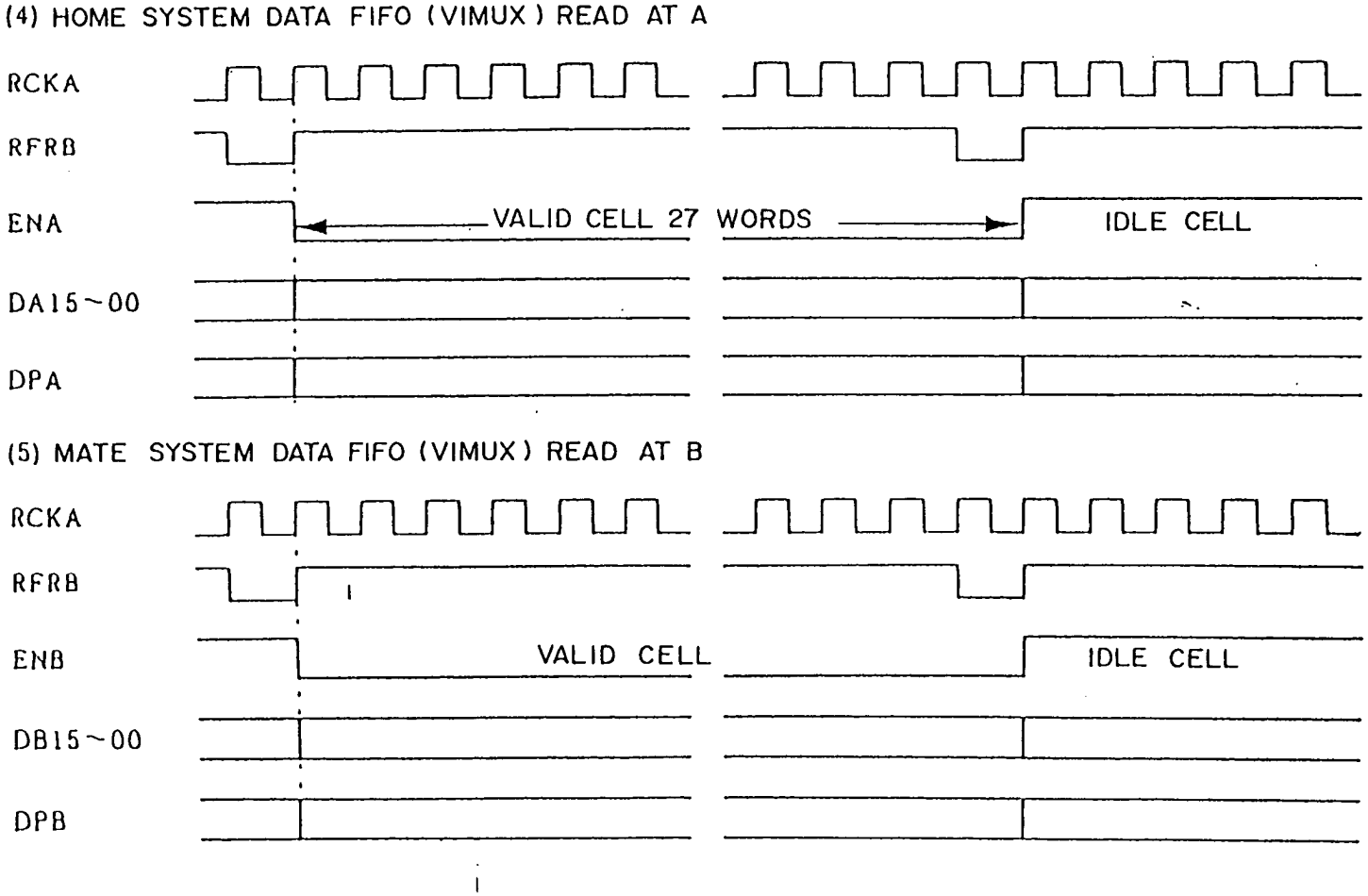
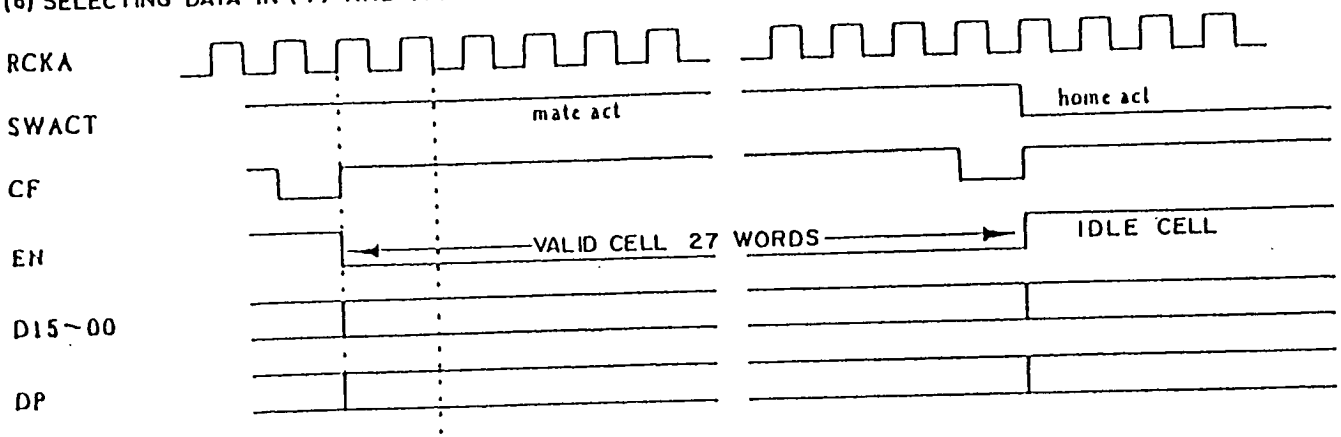
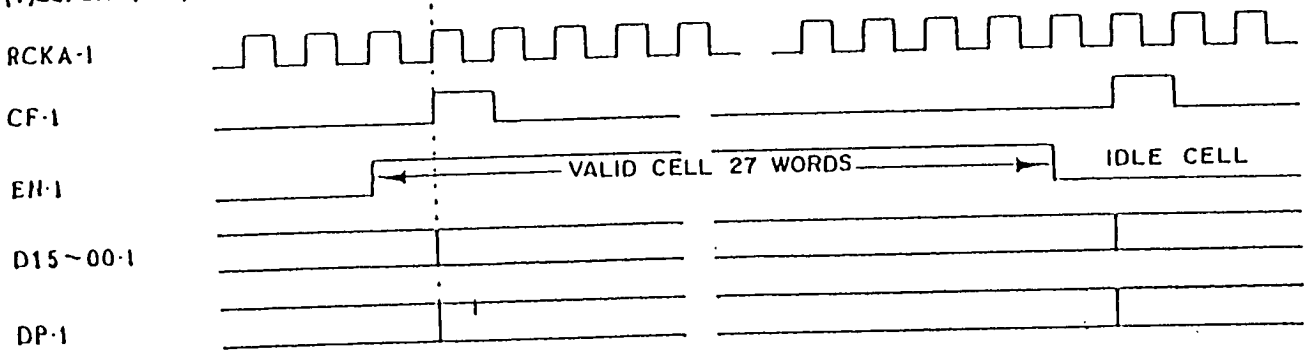

(4) HOME SYSTEM DATA FIFO (VIMUX) READ AT A
RCKA
RFRB
ENA
VALID CELL 27 WORDS
IDLE CELL
DA15~00
DPA
(5) MATE SYSTEM DATA FIFO (VIMUX) READ AT B
RCKA
RFRB
ENB
VALID CELL
IDLE CELL
DB15~00
DPB

FIG. 638

(6) SELECTING DATA IN (4) AND (5) THROUGH SWACT



(7)CSPCAD(S/P)16bit→48bit CONVERSION INPUT DATA



(8)CSPCAD(S/P)16bit→48bit CONVERSION OUTPUT DATA

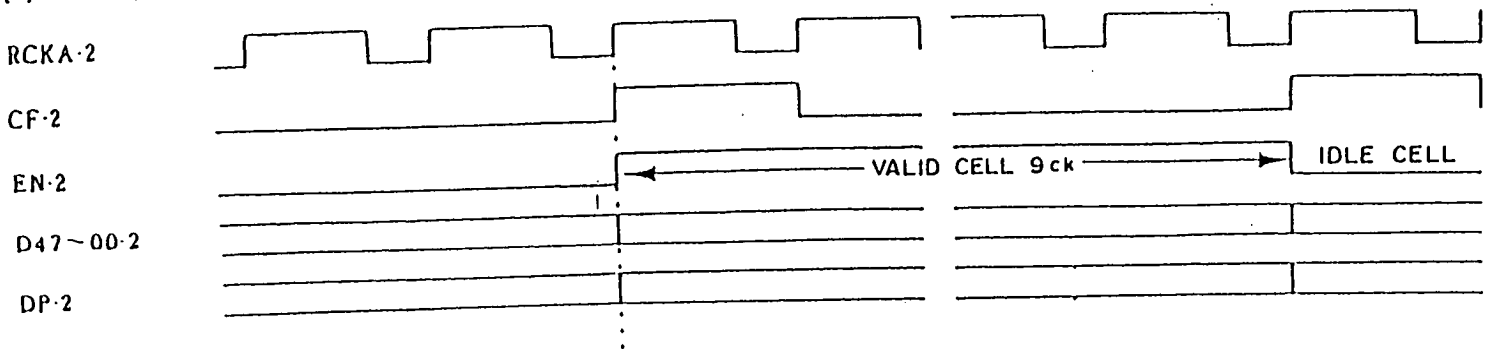


FIG. 639

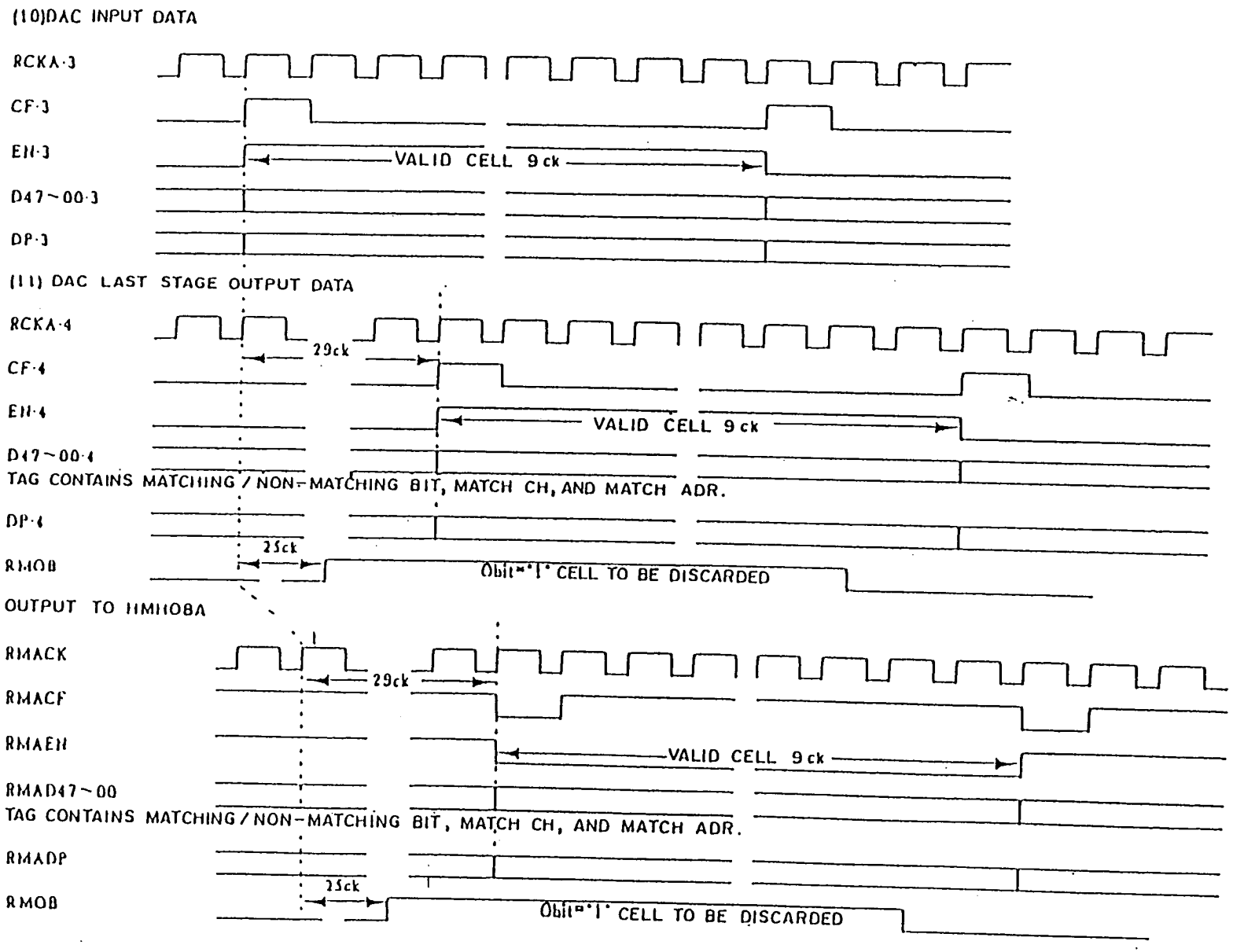

(10)DAC INPUT DATA
RCKA-3
CF-3
EN-3
VALID CELL 9ck
D47~00-3
DP-3
(11) DAC LAST STAGE OUTPUT DATA
RCKA-4
29ck
CF-4
EN-4
VALID CELL 9ck
D47~00-4
TAG CONTAINS MATCHING / NON-MATCHING BIT, MATCH CH, AND MATCH ADR.
DP-4
25ck
RMOB
Obit="1" CELL TO BE DISCARDED
OUTPUT TO HMH08A
RMACK
29ck
RMACF
RMAEN
VALID CELL 9ck
RMAD47~00
TAG CONTAINS MATCHING / NON-MATCHING BIT, MATCH CH, AND MATCH ADR.
RMADP
25ck
RMOB
Obit="1" CELL TO BE DISCARDED

FIG. 640

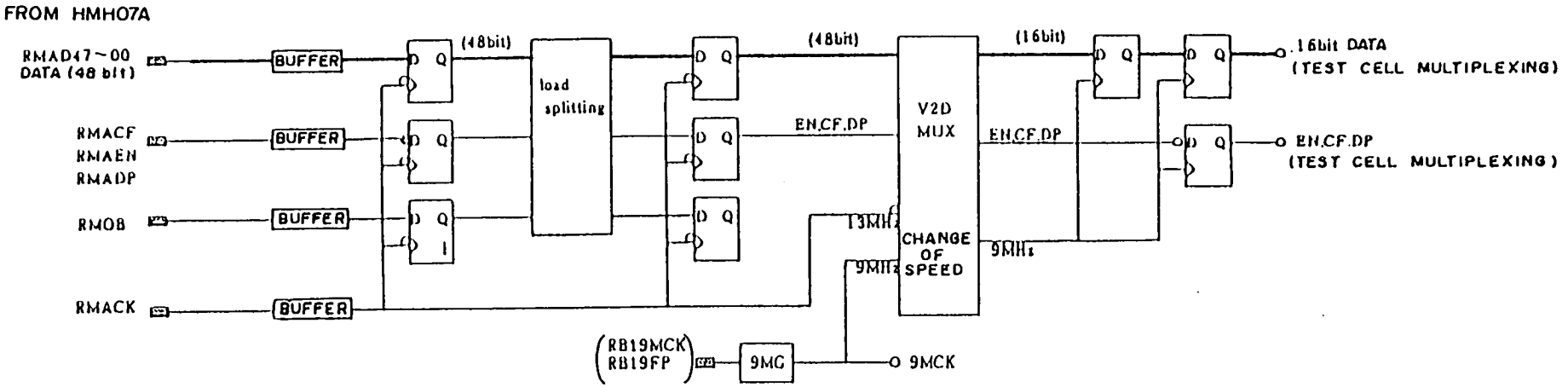

FROM HMH07A
RMAD47~00
DATA (48 bit)
RMACF
RMAEN
RMADP
RMOB
RMACK
BUFFER
(48bit)
load splitting
EN.CF.DP
V2D MUX
CHANGE OF SPEED
13MHz
9MHz
(16bit)
16bit DATA
(TEST CELL MULTIPLEXING)
EN.CF.DP
(TEST CELL MULTIPLEXING)
RB19MCK
RB19FP
9MG
9MCK

FIG. 641

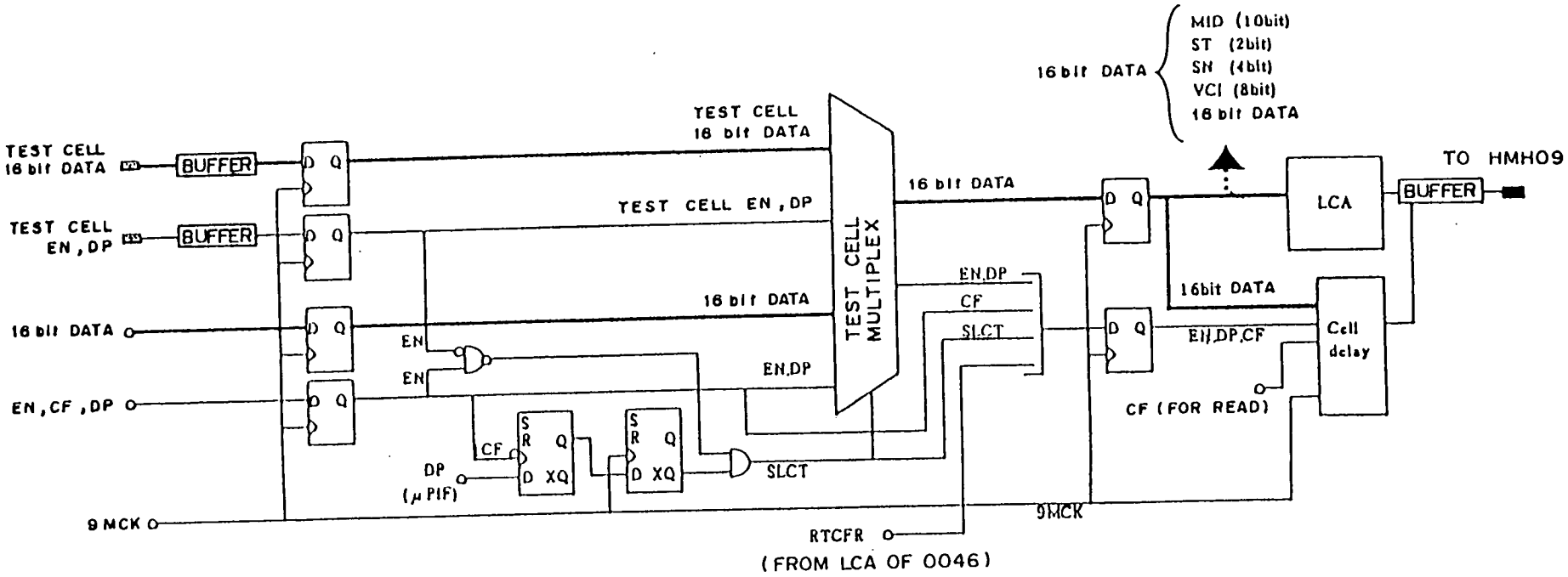

TEST CELL 16 bit DATA
BUFFER
TEST CELL EN , DP
BUFFER
16 bit DATA
EN , CF , DP
9 MCK
D Q
EN
EN
CF
DP (μ PIF)
S R Q D XQ
S R Q D XQ
SLCT
TEST CELL 16 bit DATA
TEST CELL EN , DP
16 bit DATA
EN.DP
TEST CELL MULTIPLEX
16 bit DATA
EN.DP
CF
SLCT
RTCFR
(FROM LCA OF 0046)
16 bit DATA
MID (10bit)
ST (2bit)
SN (4bit)
VCI (8bit)
16 bit DATA
LCA
TO HMH09
BUFFER
16bit DATA
EN,DP,CF
Cell delay
CF (FOR READ)
9MCK

FIG. 642

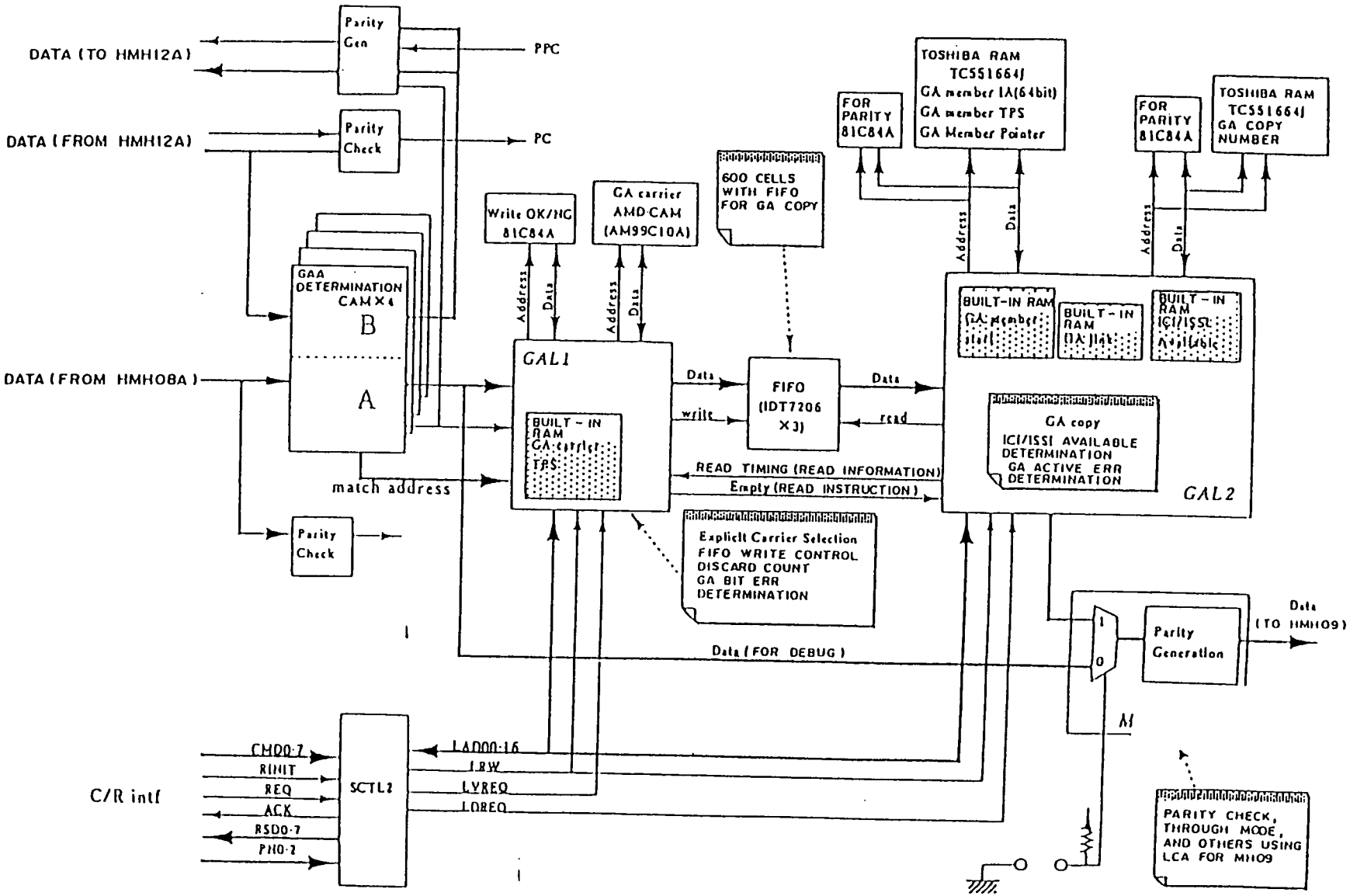

DATA (TO HMH12A)
Parity Gen
PPC
DATA (FROM HMH12A)
Parity Check
PC
TOSHIBA RAM TC551664J GA member IA(64bit) GA member TPS GA Member Pointer
FOR PARITY 81C84A
TOSHIBA RAM TC551664J GA COPY NUMBER
FOR PARITY 81C84A
Write OK/NG 81C84A
GA carrier AMD-CAM (AM99C10A)
600 CELLS WITH FIFO FOR GA COPY
Address
Data
GAA DETERMINATION CAM×4
B
A
DATA (FROM HMH08A)
GAL1
BUILT-IN RAM GA carrier TPS
Data
write
FIFO (IDT7206 ×3)
read
Data
BUILT-IN RAM GA Member
BUILT-IN RAM
BUILT-IN RAM ICI/ISSI
READ TIMING (READ INFORMATION)
Empty (READ INSTRUCTION)
GA copy ICI/ISSI AVAILABLE DETERMINATION GA ACTIVE ERR DETERMINATION
GAL2
match address
Parity Check
Explicit Carrier Selection FIFO WRITE CONTROL DISCARD COUNT GA BIT ERR DETERMINATION
Data (FOR DEBUG)
1
0
Parity Generation
Data (TO HMH09)
M
CHD0-7
RINIT
REQ
ACK
RSD0-7
PH0-2
C/R intf
SCTL2
LAD00-16
LRW
LVREQ
LOREQ
PARITY CHECK, THROUGH MODE, AND OTHERS USING LCA FOR MH09

FIG. 643

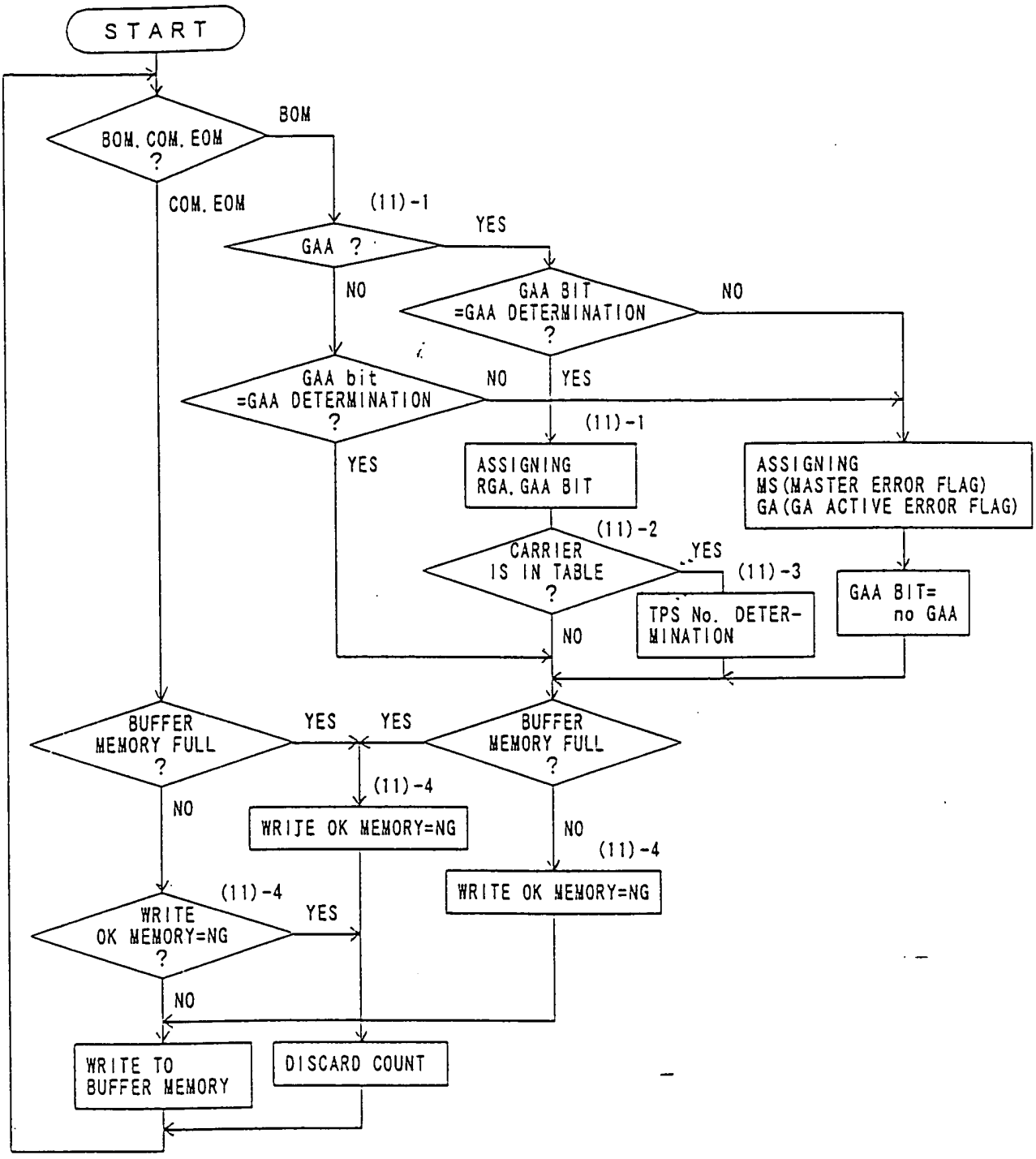

START
BOM. COM. EOM ?
BOM
COM. EOM
(11)-1
GAA ?
YES
NO
GAA BIT =GAA DETERMINATION ?
NO
GAA bit =GAA DETERMINATION ?
NO
YES
(11)-1
YES
ASSIGNING RGA. GAA BIT
ASSIGNING MS(MASTER ERROR FLAG) GA(GA ACTIVE ERROR FLAG)
(11)-2
CARRIER IS IN TABLE ?
YES
(11)-3
TPS No. DETER-MINATION
GAA BIT= no GAA
NO
BUFFER MEMORY FULL ?
YES
YES
BUFFER MEMORY FULL ?
(11)-4
WRITE OK MEMORY=NG
NO
NO
(11)-4
WRITE OK MEMORY=NG
(11)-4
WRITE OK MEMORY=NG ?
YES
NO
WRITE TO BUFFER MEMORY
DISCARD COUNT

FIG. 644

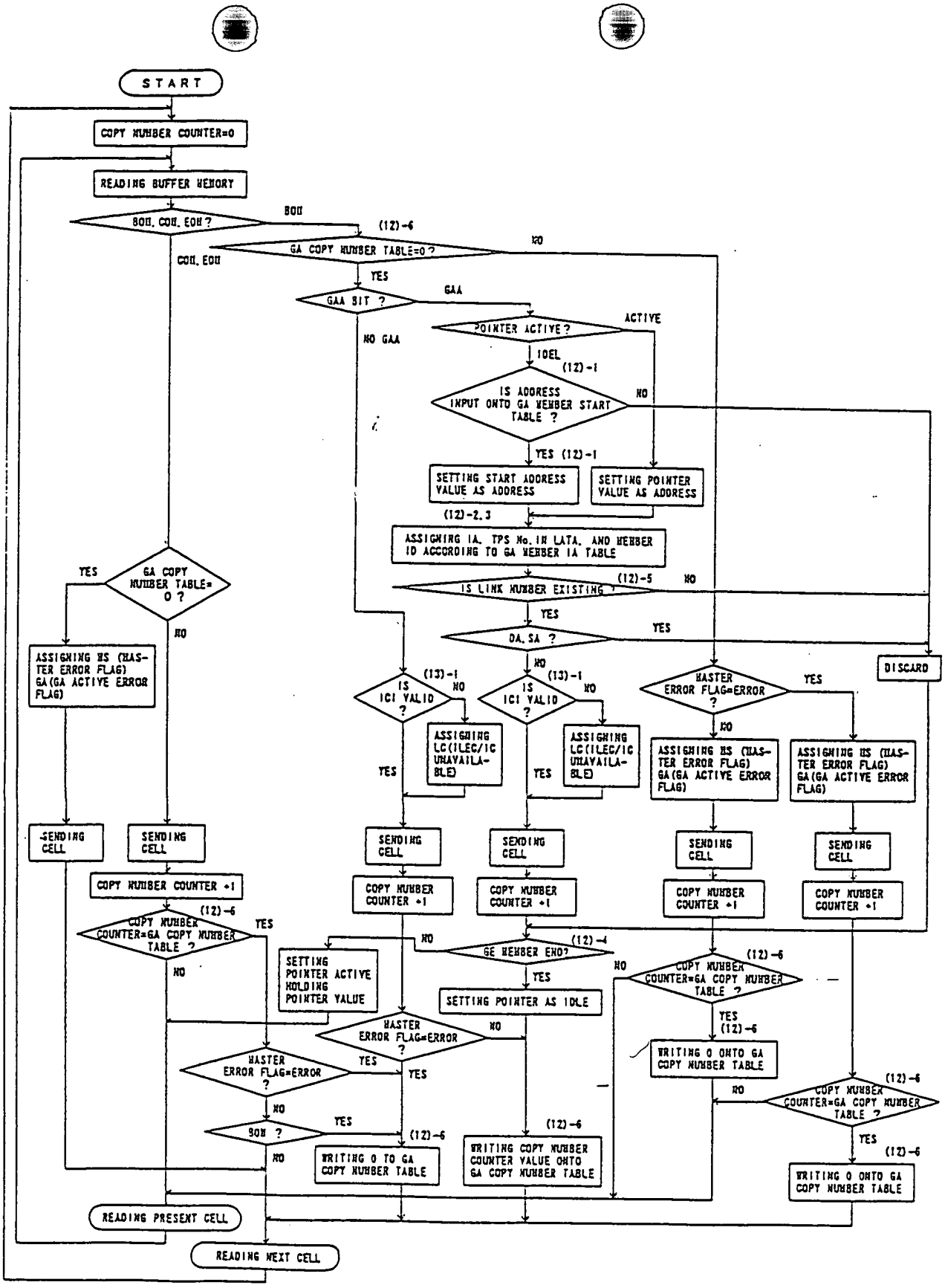

START
COPY NUMBER COUNTER=0
READING BUFFER MEMORY
BOH, COH, EOH ?
BOH
(12)-6
GA COPY NUMBER TABLE=0 ?
NO
COH, EOH
YES
GAA BIT ?
GAA
NO GAA
POINTER ACTIVE ?
ACTIVE
IDEL
(12)-1
IS ADDRESS INPUT ONTO GA MEMBER START TABLE ?
NO
YES (12)-1
SETTING START ADDRESS VALUE AS ADDRESS
SETTING POINTER VALUE AS ADDRESS
(12)-2, 3
ASSIGNING IA, TPS No. IN LATA, AND MEMBER ID ACCORDING TO GA MEMBER IA TABLE
(12)-5
IS LINK NUMBER EXISTING ?
NO
YES
DA, SA ?
YES
NO
DISCARD
YES
GA COPY NUMBER TABLE=0 ?
NO
ASSIGNING RS (MASTER ERROR FLAG) GA(GA ACTIVE ERROR FLAG)
(13)-1
IS ICI VALID ?
NO
ASSIGNING LC(ILEC/IC UNAVAILABLE)
YES
(13)-1
IS ICI VALID ?
NO
ASSIGNING LC(ILEC/IC UNAVAILABLE)
YES
MASTER ERROR FLAG=ERROR ?
YES
NO
ASSIGNING RS (MASTER ERROR FLAG) GA(GA ACTIVE ERROR FLAG)
ASSIGNING RS (MASTER ERROR FLAG) GA(GA ACTIVE ERROR FLAG)
SENDING CELL
SENDING CELL
SENDING CELL
SENDING CELL
SENDING CELL
COPY NUMBER COUNTER +1
COPY NUMBER COUNTER +1
COPY NUMBER COUNTER +1
COPY NUMBER COUNTER +1
(12)-6
COPY NUMBER COUNTER=GA COPY NUMBER TABLE ?
YES
NO
SETTING POINTER ACTIVE HOLDING POINTER VALUE
NO
(12)-4
GE MEMBER END?
YES
SETTING POINTER AS IDLE
(12)-6
COPY NUMBER COUNTER=GA COPY NUMBER TABLE ?
NO
YES
(12)-6
WRITING 0 ONTO GA COPY NUMBER TABLE
MASTER ERROR FLAG=ERROR ?
NO
YES
MASTER ERROR FLAG=ERROR ?
YES
YES
NO
BOH ?
YES
NO
(12)-6
WRITING 0 TO GA COPY NUMBER TABLE
(12)-6
WRITING COPY NUMBER COUNTER VALUE ONTO GA COPY NUMBER TABLE
(12)-6
COPY NUMBER COUNTER=GA COPY NUMBER TABLE ?
NO
YES
(12)-6
WRITING 0 ONTO GA COPY NUMBER TABLE
READING PRESENT CELL
READING NEXT CELL

FIG. 645

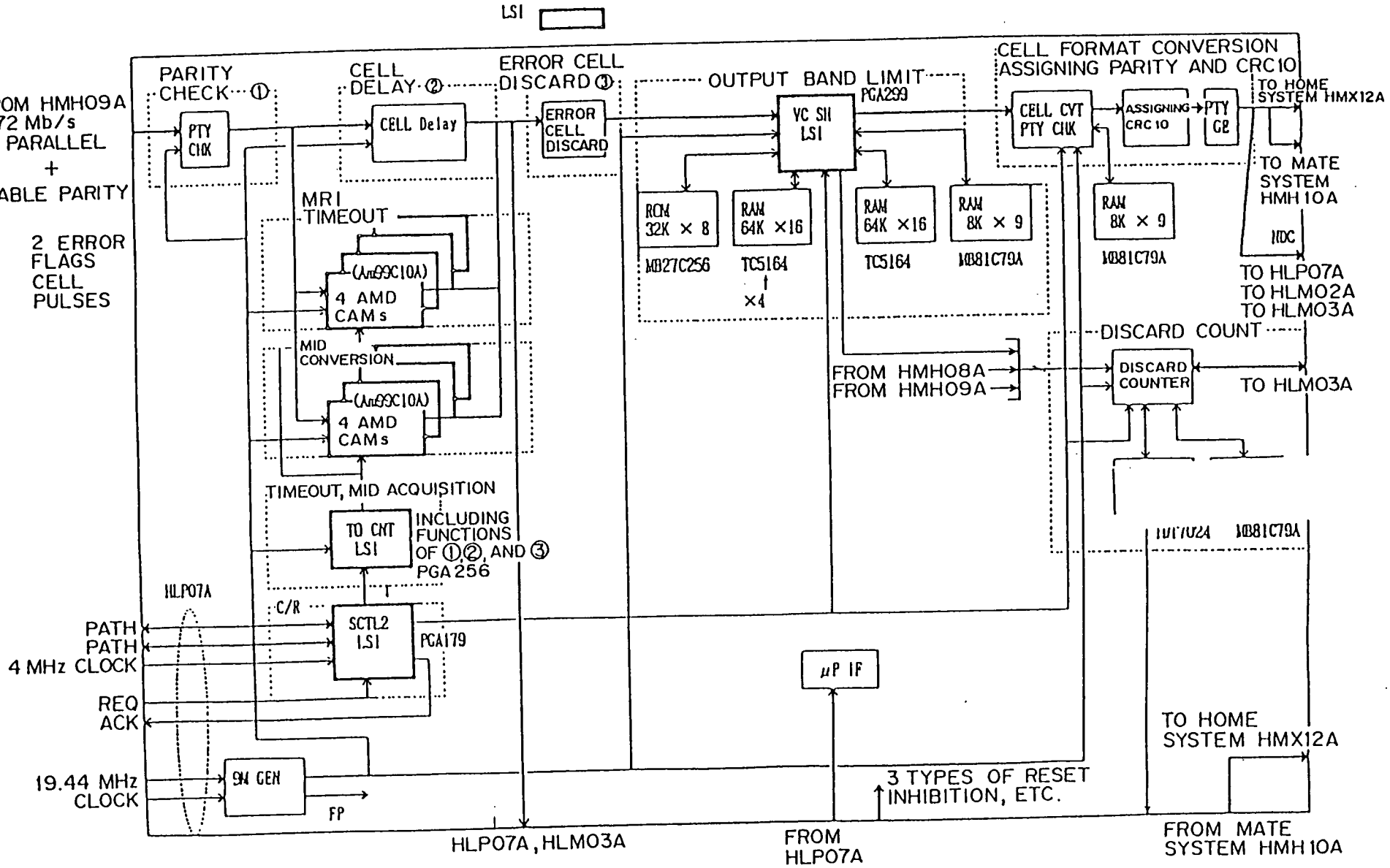

LSI
FROM HMH09A
9.72 Mb/s
16 PARALLEL
+
ENABLE PARITY
2 ERROR FLAGS CELL PULSES
PARITY CHECK ①
CELL DELAY ②
ERROR CELL DISCARD ③
PTY CHK
CELL Delay
ERROR CELL DISCARD
OUTPUT BAND LIMIT
VC SII LSI
PGA299
CELL FORMAT CONVERSION ASSIGNING PARITY AND CRC10
CELL CVT PTY CHK
ASSIGNING CRC 10
PTY GE
TO HOME SYSTEM HMX12A
TO MATE SYSTEM HMH10A
IIDC
TO HLP07A
TO HLM02A
TO HLM03A
ROM 32K × 8
MB27C256
RAM 64K ×16
TC5164
×4
RAM 64K ×16
TC5164
RAM 8K × 9
MB81C79A
RAM 8K × 9
MB81C79A
MRI TIMEOUT
(Am99C10A)
4 AMD CAMs
MID CONVERSION
(Am99C10A)
4 AMD CAMs
TIMEOUT, MID ACQUISITION
TO CNT LSI
INCLUDING FUNCTIONS OF ①,②, AND ③
PGA256
DISCARD COUNT
FROM HMH08A
FROM HMH09A
DISCARD COUNTER
TO HLM03A
HLP07A
C/R
SCTL2 LSI
PGA179
PATH
PATH
4 MHz CLOCK
REQ
ACK
μP IF
19.44 MHz CLOCK
9M GEN
FP
3 TYPES OF RESET INHIBITION, ETC.
TO HOME SYSTEM HMX12A
HLP07A, HLM03A
FROM HLP07A
FROM MATE SYSTEM HMH10A

FIG. 646

ITEM	FUNCTION	REMARKS
1	PARITY CHECK	PERFORMING PARITY CHECK ON DATA AND ENABLE.
2	MRI TIMEOUT	DETERMINING MRI TIMEOUT OF MESSAGE
3	MID CONVERSION	CONVERTING INPUT MID TO VCI AND MID OF OUTPUT LINK
4	CELL DELAY	TIME DELAY REQUIRED FOR TIMEOUT PROCESS AND MID CONVERSION PROCESS.
5	ERROR CELL DISCARD	RECEIVING ERROR FLAG AND DISCARDING CELL.
6	OUTPUT BAND LIMIT	LIMITING OUTPUT BAND BASED ON LIMITED BAND.
7	FORMAT CONVERSION	CONVERTING CELL FORMAT INTO ISSI OR ICI FORMAT.
8	GENERATING AND ASSIGNING CRC-10	PERFORMING CRC-10 OPERATION ON PAYLOAD EXCLUDING HEADER AND ASSIGNING OPERATION RESULT.
9	DISCARD COUNTER	RECEIVING DISCARDED CELLS FROM HMH08A, HMH09A, AND VC-SH II, COUNTING THEM, AND PASSING THEM TO LP-COM.
10	C/R UNIT	RECEIVING COMMANDS FROM HLP07A BY SCTL2 LSI, AND RETURNING RESPONSE.
11	MSCN, MSD UNIT	RECEIVING VARIOUS CONTROL SIGNALS AND DATA FROM μP UNIT AND CONTROLLING INTERNAL UNITS.
12	CLK Gen.	GENERATING 9.72 MHz CLOCK FROM 19.44 MHz CLOCK AND FRAME PULSE.

FIG. 647

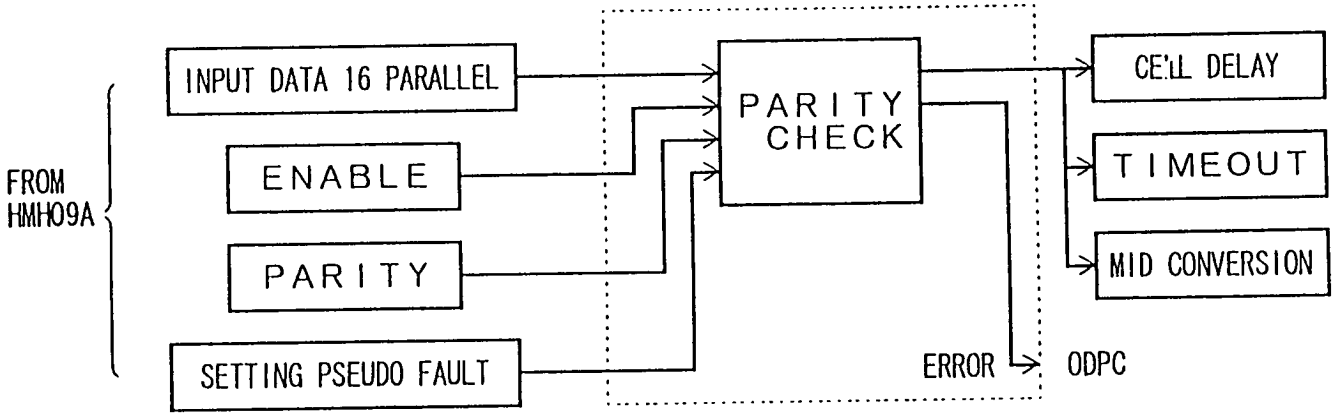

FROM HMH09A
INPUT DATA 16 PARALLEL
ENABLE
PARITY
SETTING PSEUDO FAULT
PARITY CHECK
ERROR
ODPC
CELL DELAY
TIMEOUT
MID CONVERSION

FIG. 648

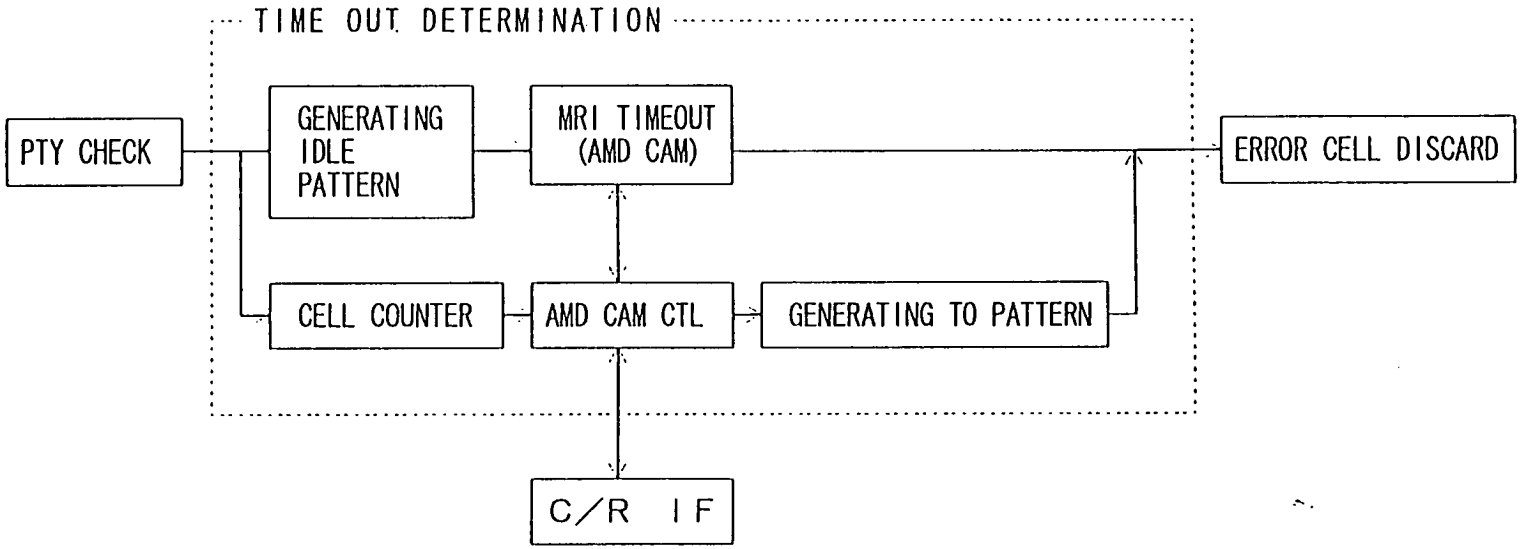

TIME OUT DETERMINATION
PTY CHECK
GENERATING IDLE PATTERN
MRI TIMEOUT (AMD CAM)
ERROR CELL DISCARD
CELL COUNTER
AMD CAM CTL
GENERATING TO PATTERN
C/R IF

FIG. 649

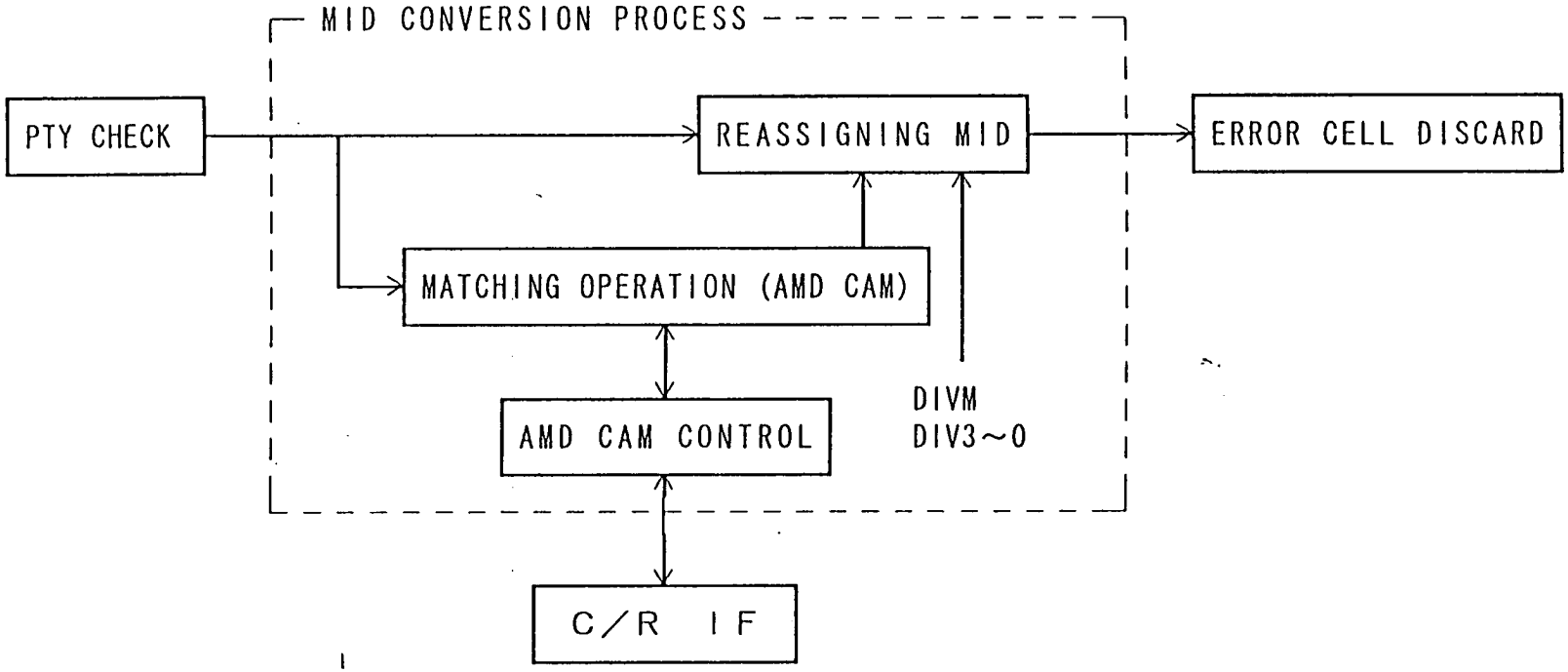

MID CONVERSION PROCESS
PTY CHECK
REASSIGNING MID
ERROR CELL DISCARD
MATCHING OPERATION (AMD CAM)
AMD CAM CONTROL
DIVM
DIV3~0
C/R IF

FIG. 650

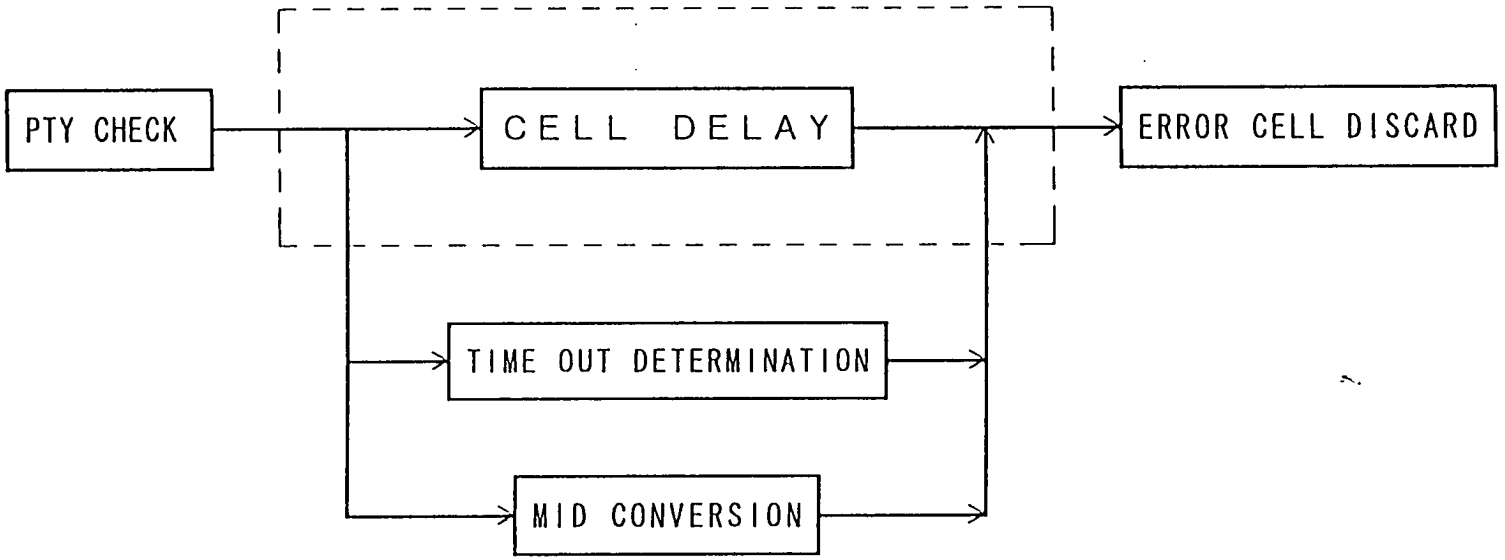

PTY CHECK
CELL DELAY
ERROR CELL DISCARD
TIME OUT DETERMINATION
MID CONVERSION

FIG. 651

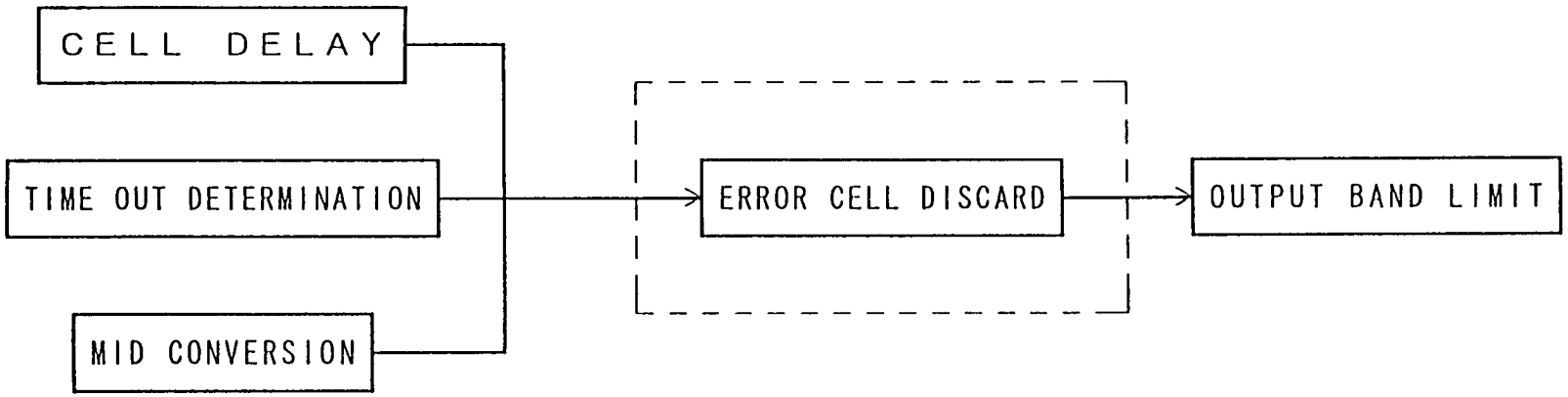

CELL DELAY
TIME OUT DETERMINATION
MID CONVERSION
ERROR CELL DISCARD
OUTPUT BAND LIMIT

FIG. 652

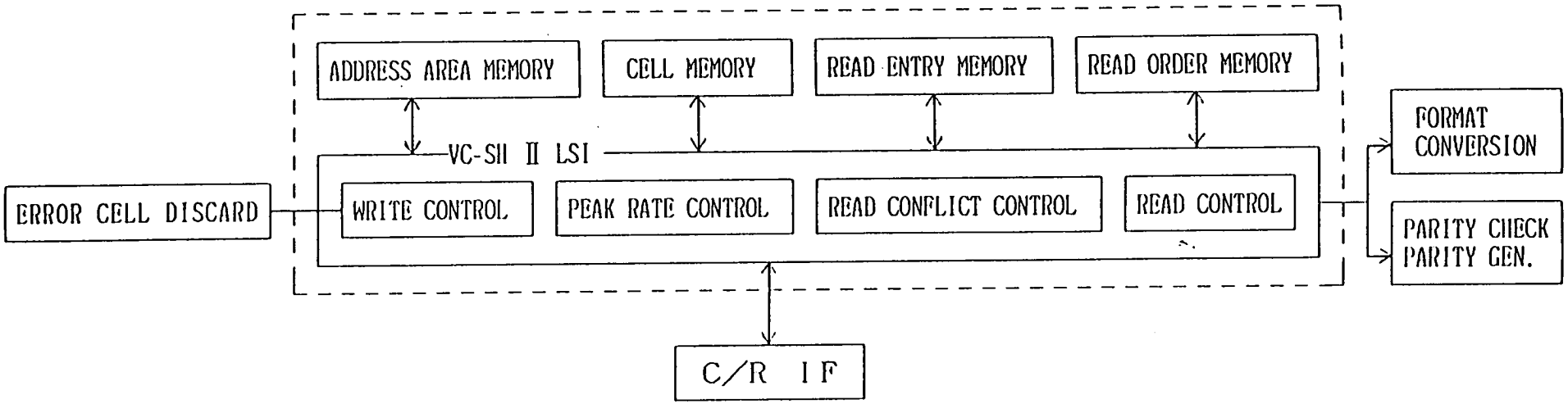
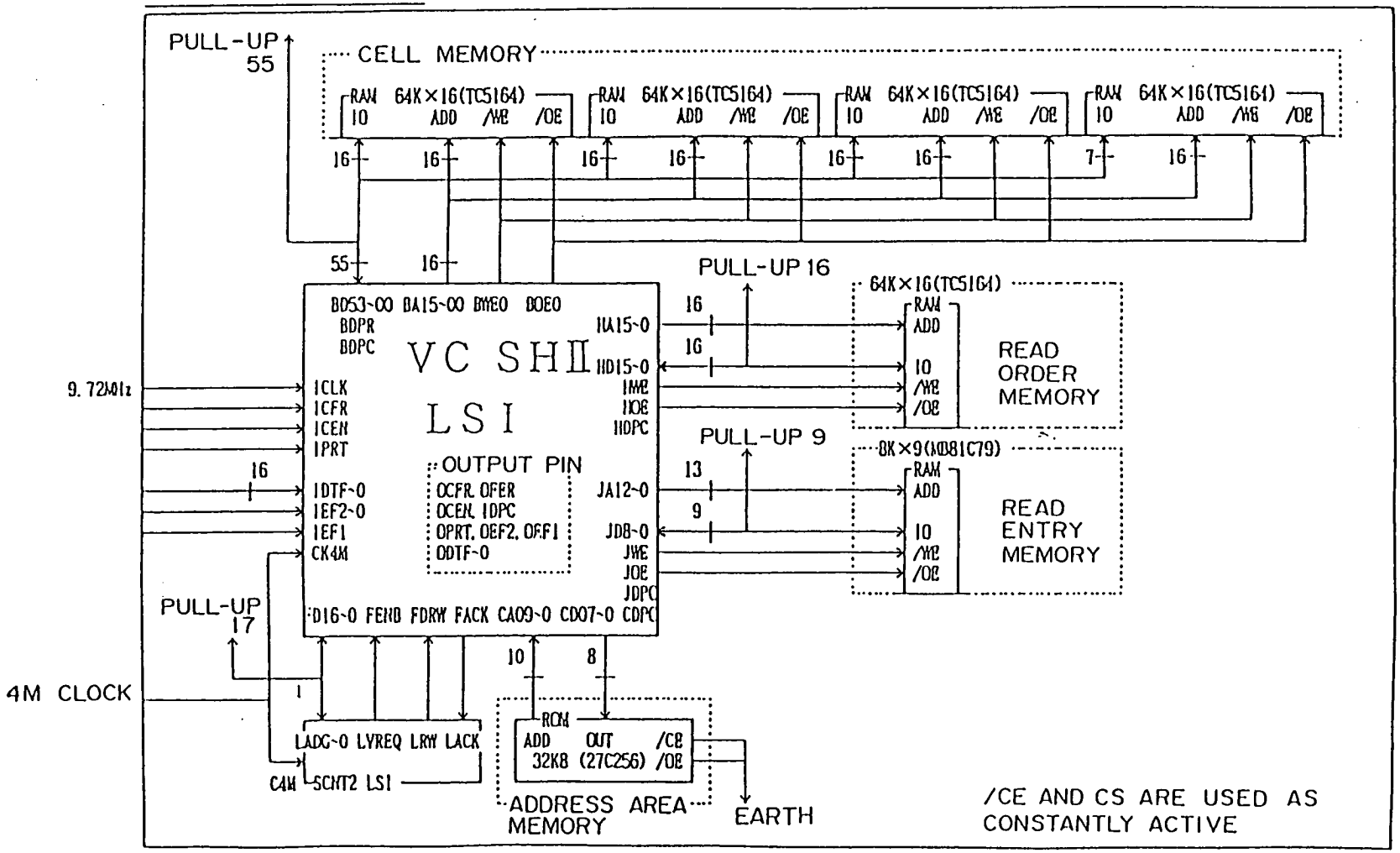

ADDRESS AREA MEMORY
CELL MEMORY
READ ENTRY MEMORY
READ ORDER MEMORY
VC-SII II LSI
ERROR CELL DISCARD
WRITE CONTROL
PEAK RATE CONTROL
READ CONFLICT CONTROL
READ CONTROL
FORMAT CONVERSION
PARITY CHECK PARITY GEN.
C/R IF

FIG. 653

OUTPUT BAND LIMIT (CONNECTION TO_VC-SH LSI)



GROUPING INTO VC-SH BLOCKS (IN PKG)

0: INPUT DATA AND OUTPUT DATA
1: CELL MEMORY ADDRESS, /WE, /OE
2~4: CELL MEMORY DATA AND ERROR FLAG
5: ADDRESS AREA MEMORY
6: READ ORDER MEMORY AND READ ENTRY MEMORY
7: SCNT 2 DATA AND CONTROL
8: PARITY CHECK, RESET, CONTROL
9: SCAN PIN, TEST MONITOR OUTPUT (NOT SHOWN IN BLOCK DIAGRAM ABOVE)

FIG. 654

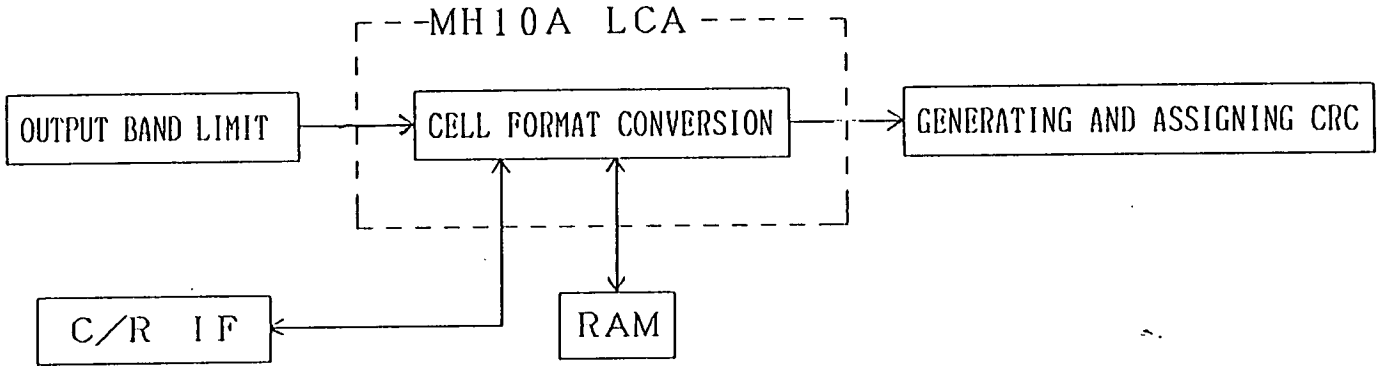

MH10A LCA
OUTPUT BAND LIMIT
CELL FORMAT CONVERSION
GENERATING AND ASSIGNING CRC
C/R IF
RAM

FIG. 655

7. COMMON PROCESS (INDEPENDENT OF BOM, COM, OR EOM)

① TEST CELL WHEN CELL 01 WORD b15 (INPUT VCI HIGHER ORDER BIT) IS 1, GW CELL WHEN b14 IS 1, AND SB CELL WHEN b14 IS 0.

② WRITING 03F0(H) TO CELL 01 WORD

③ WRITING 0011(b) TO CELL 02 WORD b15-12.

④ ASSIGNING CELL 02 WORD b6-4 (LINK ID) AS ADDRESS OF EXTERNAL RAM. WHEN b7 (TYPE BIT) OF READ DATA IS 1, ICI CELL IS ASSUMED AND 1(b) IS WRITTEN TO CELL 02 WORD b8. b8 IS NOT REWRITTEN WHEN b7 OF READ DATA IS 0.

2. IDENTIFYING SEGMENT TYPE

① BOM WHEN CELL 03 WORD b15-14 IS 10, COM WHEN 00, AND EOM WHEN 01. WHEN 11, PROCESS FOR BOM IS PERFORMED. (WHEN b15 IS 1, PROCESS FOR BOM IS PERFORMED.)

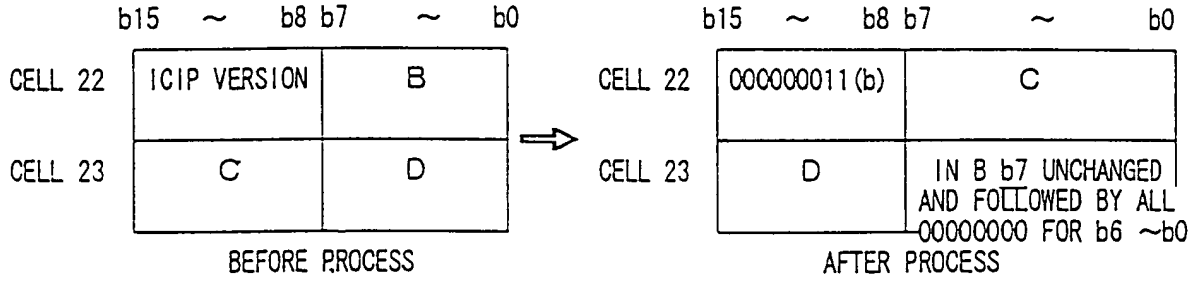
3. WHEN CELL IS BOM OF ICI

① WRITING 0000000(b) IS WRITTEN TO CELL 14 WORD b9-3.

② WHEN CELL 14 WORD b15-10 (PROTOCOL ID) IS 48 (DEC) OR 60 (DEC) AND IT IS TEST CELL OR GW CELL, PROCESS TERMINATES.

③ IF ② ABOVE IS NOT SATISFIED, IT IS USER CELL AND READ DATA b5-b0 IN 1-④ ABOVE IS WRITTEN TO 14 WORD b15-10 (PROTOCOL ID).

④ CELL 22 WORD AND 23 WORD ARE REWRITTEN AS FOLLOWS.



⑤ 0 IS WRITTEN TO ALL BITS OF CELL 24 WORD AND 25 WORD.

4. WHEN CELL IS BOM OF ISSI

① WHEN CELL 14 WORD b15-10 (SERVICE TYPE) IS 48 (DEC) OR 60 (DEC) AND IT IS TEST CELL OR GW CELL, 00000001(b) IS WRITTEN TO CELL 15 WORD AND b15-8.

② IF ① ABOVE IS NOT SATISFIED, IT IS USER CELL AND READ DATA b5-b0 IN 1-④ ABOVE IS WRITTEN TO 14 WORD b15-10 (SERVICE TYPE), AND 0001000(b) IS WRITTEN TO CELL 14 WORD b9-3.

③ WRITING 0000001(b) IS WRITTEN TO CELL 15 WORD b7-0 (PROTOCOL DISCRIMINATOR).

④ CELL 22 WORD AND 23 WORD ARE REWRITTEN AS FOLLOWS.

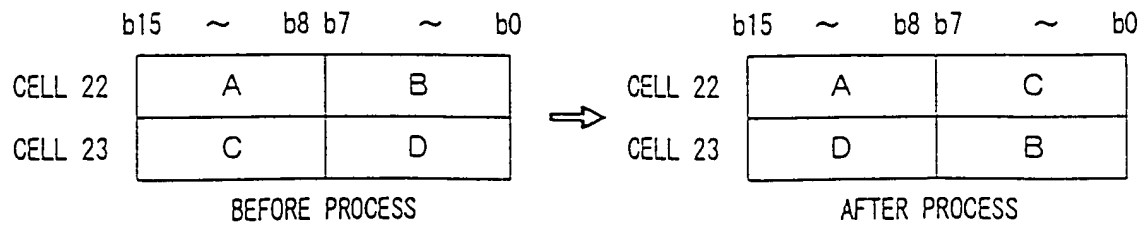


FIG. 656

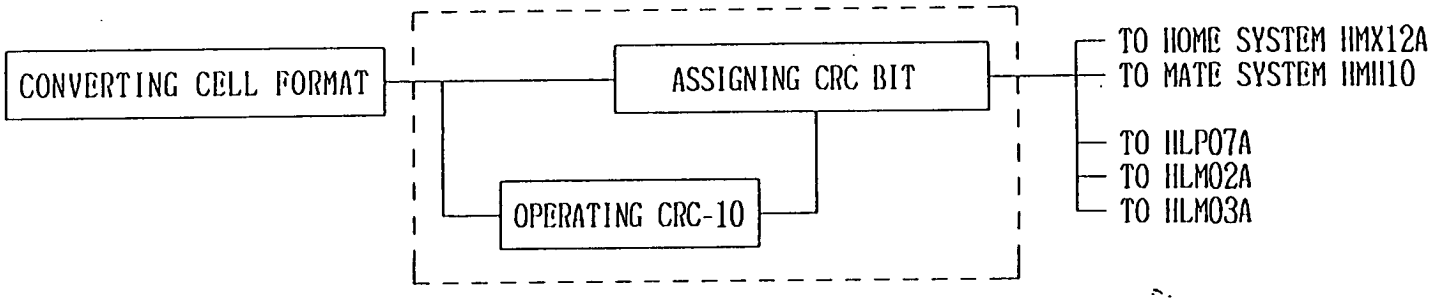

CONVERTING CELL FORMAT
ASSIGNING CRC BIT
OPERATING CRC-10
TO HOME SYSTEM HMX12A
TO MATE SYSTEM HMH10
TO HLP07A
TO HLM02A
TO HLM03A

FIG. 657

GENERATION POLYNOMIAL FOR CRC-10 $\Rightarrow X^{10}+X^{9}+X^{5}+X^{4}+X+1$

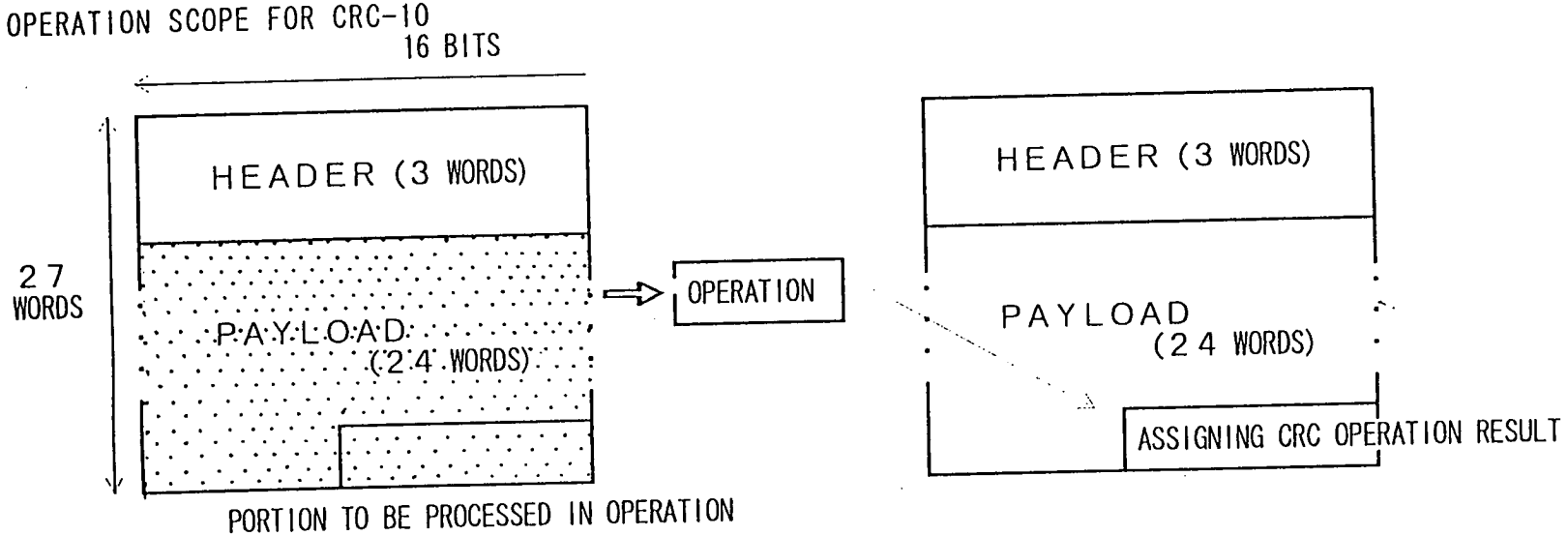


FIG. 658

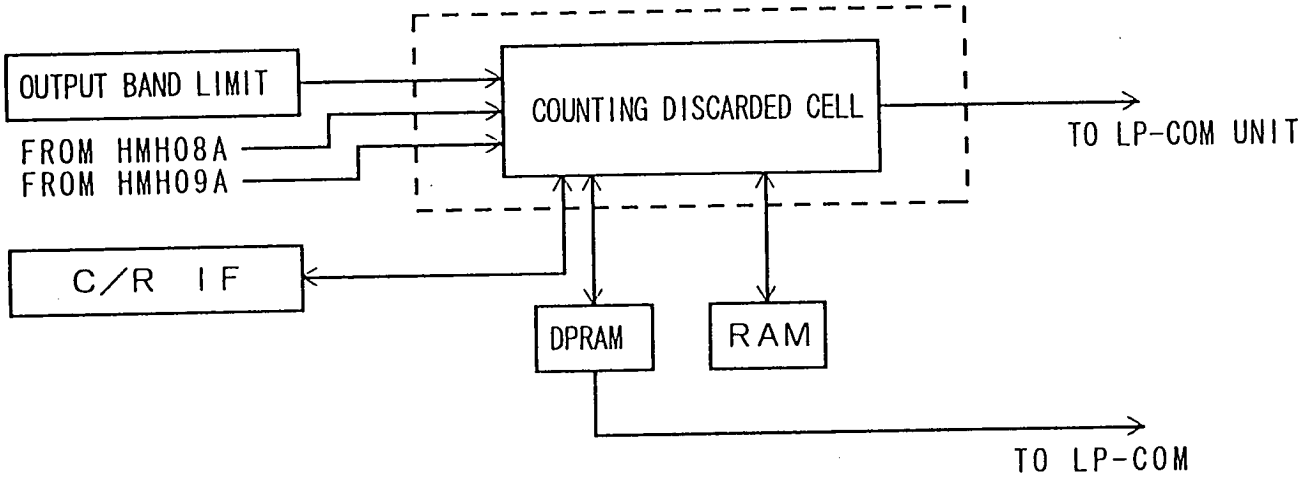

OUTPUT BAND LIMIT
FROM HMH08A
FROM HMH09A
COUNTING DISCARDED CELL
TO LP-COM UNIT
C/R IF
DPRAM
RAM
TO LP-COM

FIG. 659

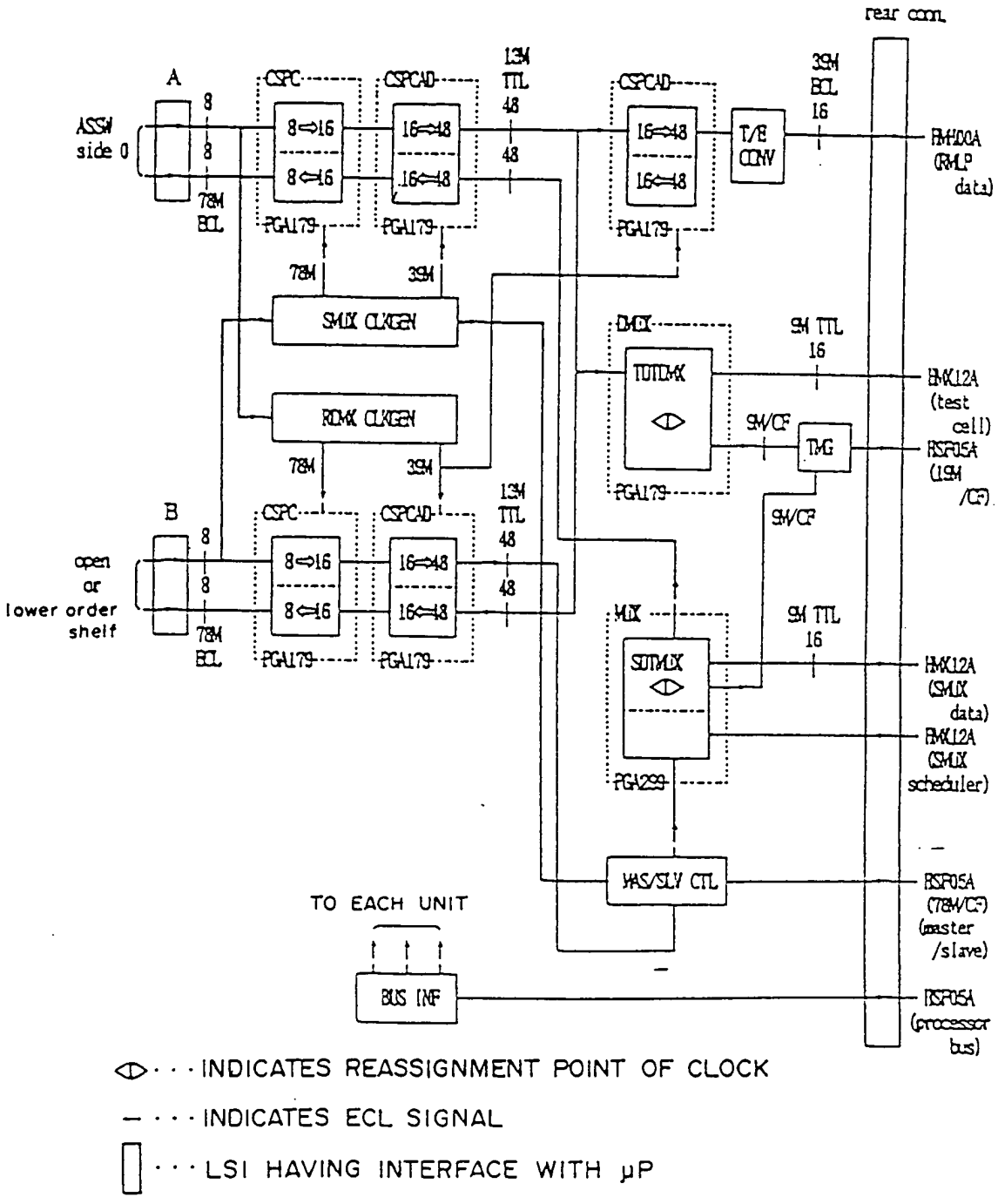

rear conn.
A
ASSM side 0
8
8
78M ECL
CSPC
8⇔16
8⇐16
PGA179
CSPCAD
16⇔48
16⇐48
PGA179
13M TTL 48
48
CSPCAD
16⇔48
16⇐48
PGA179
T/E CONV
39M ECL 16
FMH00A (RMLP data)
78M
39M
SMUX CLKGEN
RDMX CLKGEN
78M
39M
B
open or lower order shelf
8
8
78M ECL
CSPC
8⇔16
8⇐16
PGA179
CSPCAD
16⇔48
16⇐48
PGA179
13M TTL 48
48
DMUX
TUTLMX
PGA179
SM TTL 16
FMX12A (test cell)
SM/CF
TMG
RSF05A (13M /CF)
SM/CF
MUX
SUTMUX
PGA299
SM TTL 16
FMX12A (SMUX data)
FMX12A (SMUX scheduler)
MAS/SLV CTL
RSF05A (78M/CF) (master /slave)
TO EACH UNIT
BUS INF
RSF05A (processor bus)
◁▷ · · · INDICATES REASSIGNMENT POINT OF CLOCK
— · · · INDICATES ECL SIGNAL
▯ · · · LSI HAVING INTERFACE WITH μP

FIG. 660

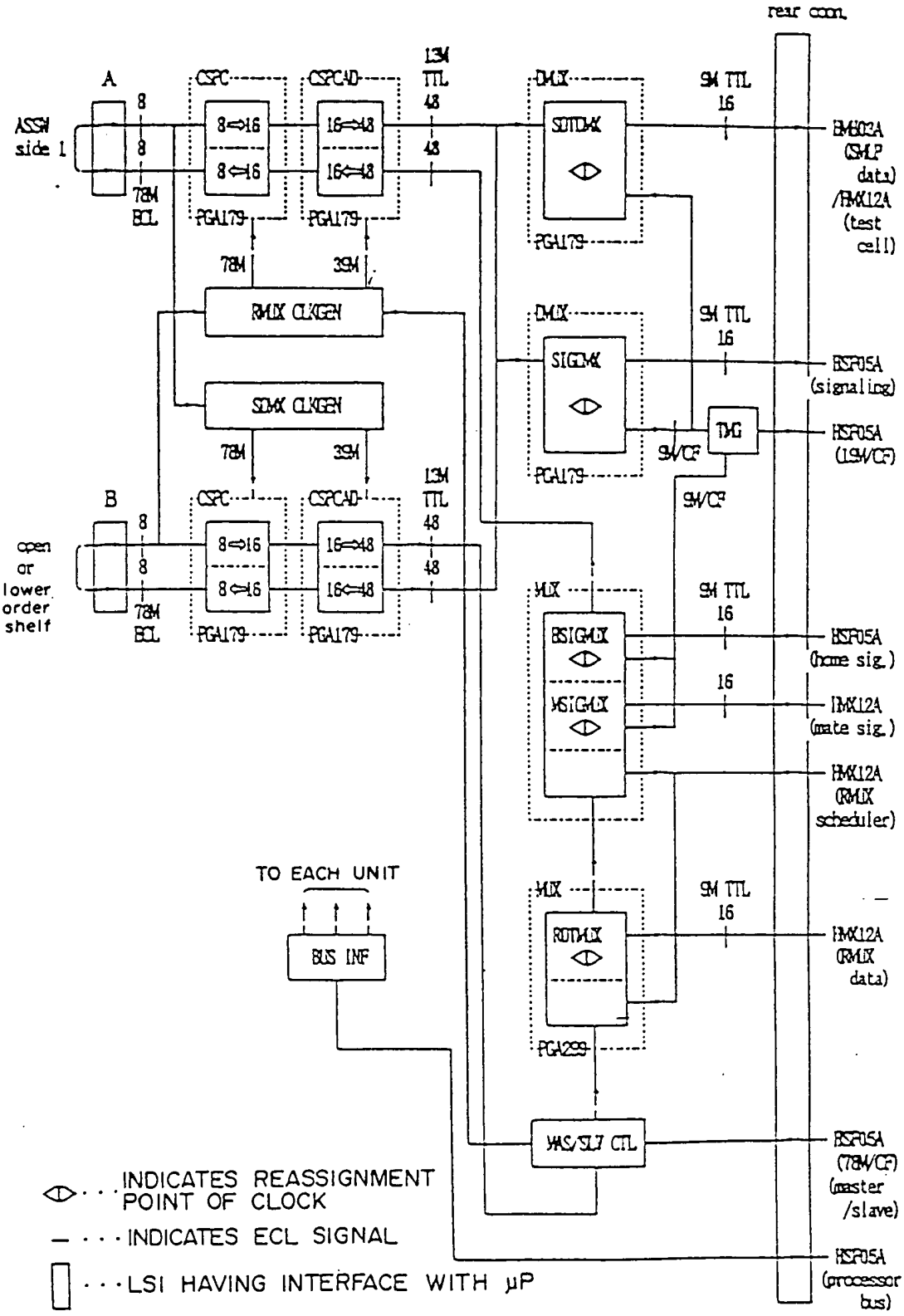

rear conn.
A
B
ASSM side 1
open or lower order shelf
8
8
78M ECL
CSPC
CSPCAD
8⇔16
16⇔48
8⇐16
16⇐48
PGA179
13M TTL
48
78M
39M
RMUX CLKGEN
SDMX CLKGEN
DMUX
SDTDMX
SIGDMX
TMG
SM TTL
16
SM/CF
MUX
BSIGMUX
MSIGMUX
RDTMUX
PGA299
MAS/SLV CTL
TO EACH UNIT
BUS INF
EM603A (SMLP data) /HMX12A (test cell)
HSP05A (signaling)
HSP05A (LSM/CF)
HSP05A (home sig.)
HMX12A (mate sig.)
HMX12A (RMUX scheduler)
HMX12A (RMUX data)
HSP05A (78M/CF) (master /slave)
HSP05A (processor bus)
INDICATES REASSIGNMENT POINT OF CLOCK
INDICATES ECL SIGNAL
LSI HAVING INTERFACE WITH μP

FIG. 661

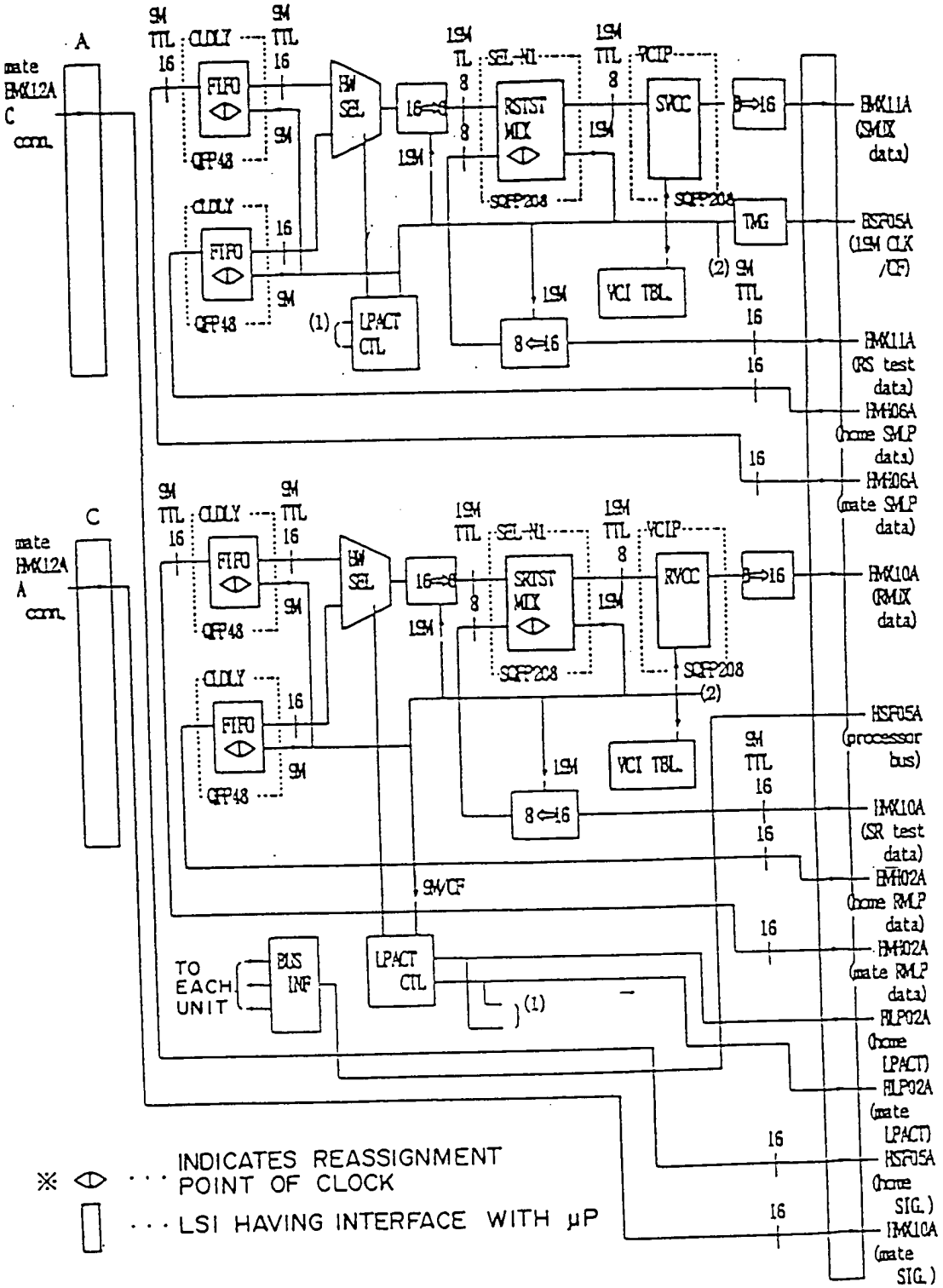

A
mate HMK12A C conn.
C
mate HMK12A A conn.
FIFO
QFP48
SEL
RSTST MUX
SVCC
RVCC
VCI TBL.
LPACT CTL
BUS INF
TMG
SQFP208
TO EACH UNIT
SMVCF
HMK11A (SMUX data)
HSF05A (LSM CLK /CF)
HMK11A (RS test data)
HMH06A (home SMLP data)
HMH06A (mate SMLP data)
HMK10A (RMUX data)
HSF05A (processor bus)
HMK10A (SR test data)
HMH02A (home RMLP data)
HMH02A (mate RMLP data)
HLP02A (home LPACT)
HLP02A (mate LPACT)
HSF05A (home SIG.)
HMK10A (mate SIG.)
※ ◇ ... INDICATES REASSIGNMENT POINT OF CLOCK
▯ ... LSI HAVING INTERFACE WITH μP

FIG. 662

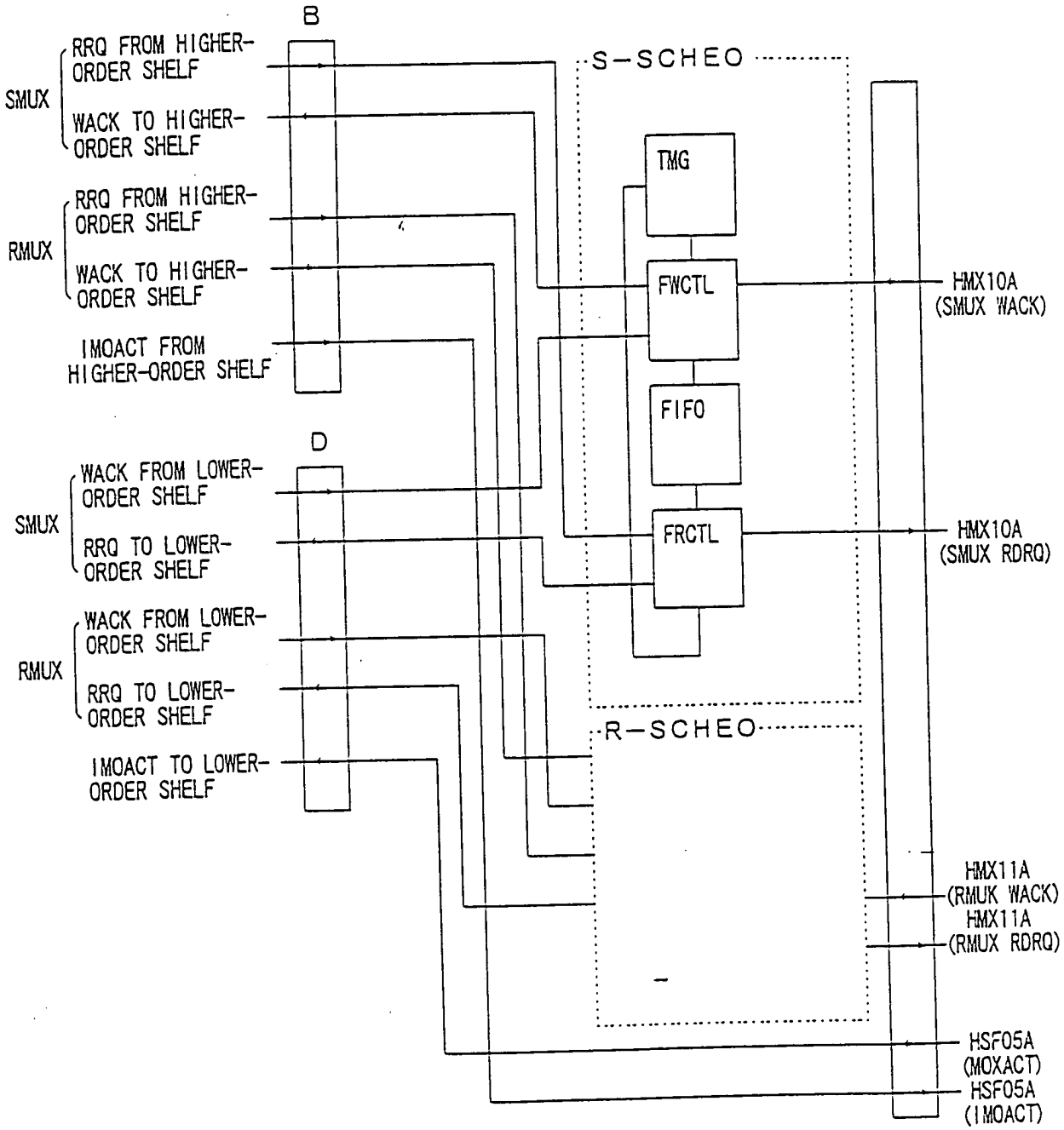

B
SMUX
RRQ FROM HIGHER-ORDER SHELF
WACK TO HIGHER-ORDER SHELF
RMUX
RRQ FROM HIGHER-ORDER SHELF
WACK TO HIGHER-ORDER SHELF
IMOACT FROM HIGHER-ORDER SHELF
D
SMUX
WACK FROM LOWER-ORDER SHELF
RRQ TO LOWER-ORDER SHELF
RMUX
WACK FROM LOWER-ORDER SHELF
RRQ TO LOWER-ORDER SHELF
IMOACT TO LOWER-ORDER SHELF
S-SCHEO
TMG
FWCTL
FIFO
FRCTL
R-SCHEO
HMX10A (SMUX WACK)
HMX10A (SMUX RDRQ)
HMX11A (RMUK WACK)
HMX11A (RMUX RDRQ)
HSF05A (MOXACT)
HSF05A (IMOACT)

FIG. 663

6,052,368 6/2/2000

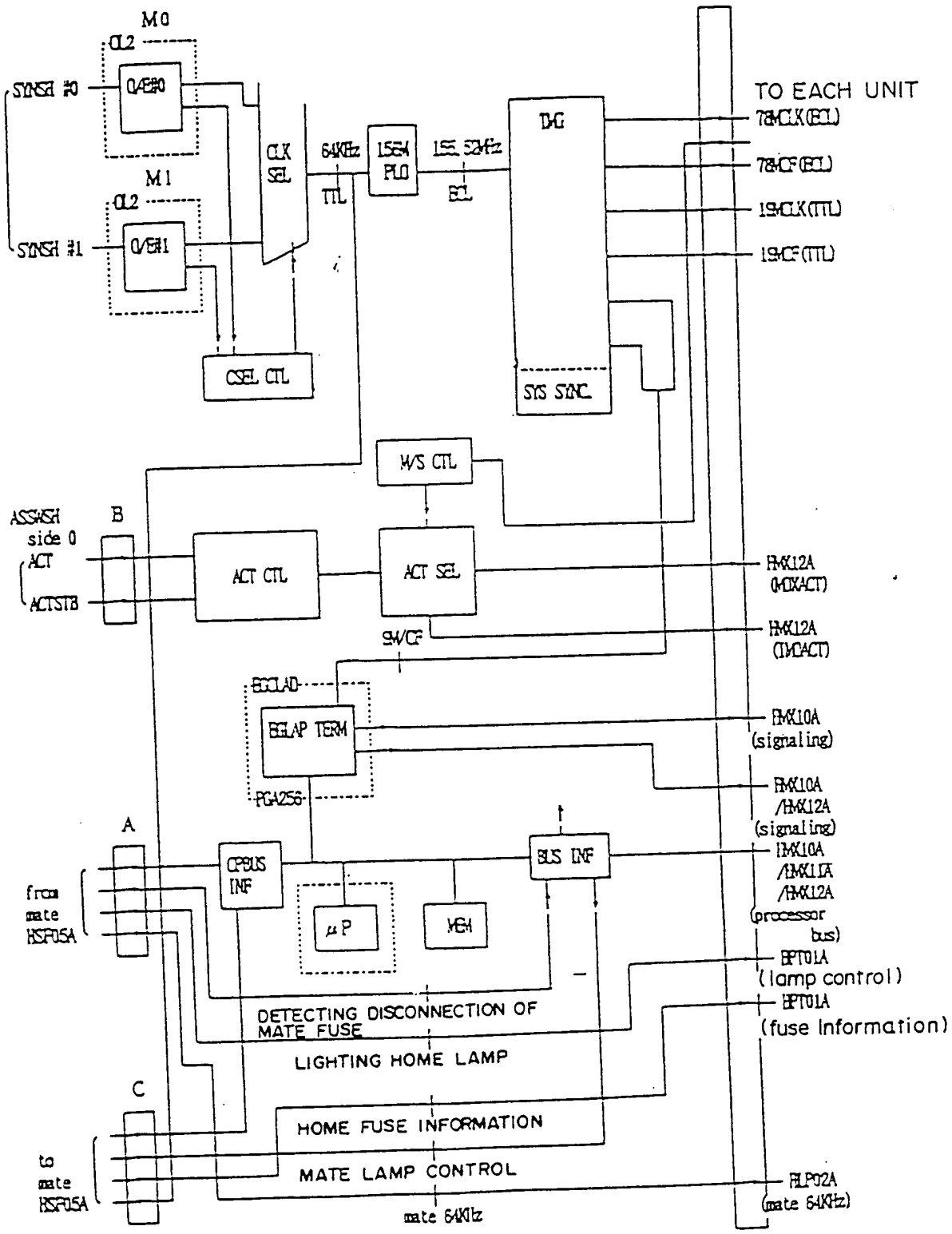


FIG. 664

6,963,620 - 12/2/2005

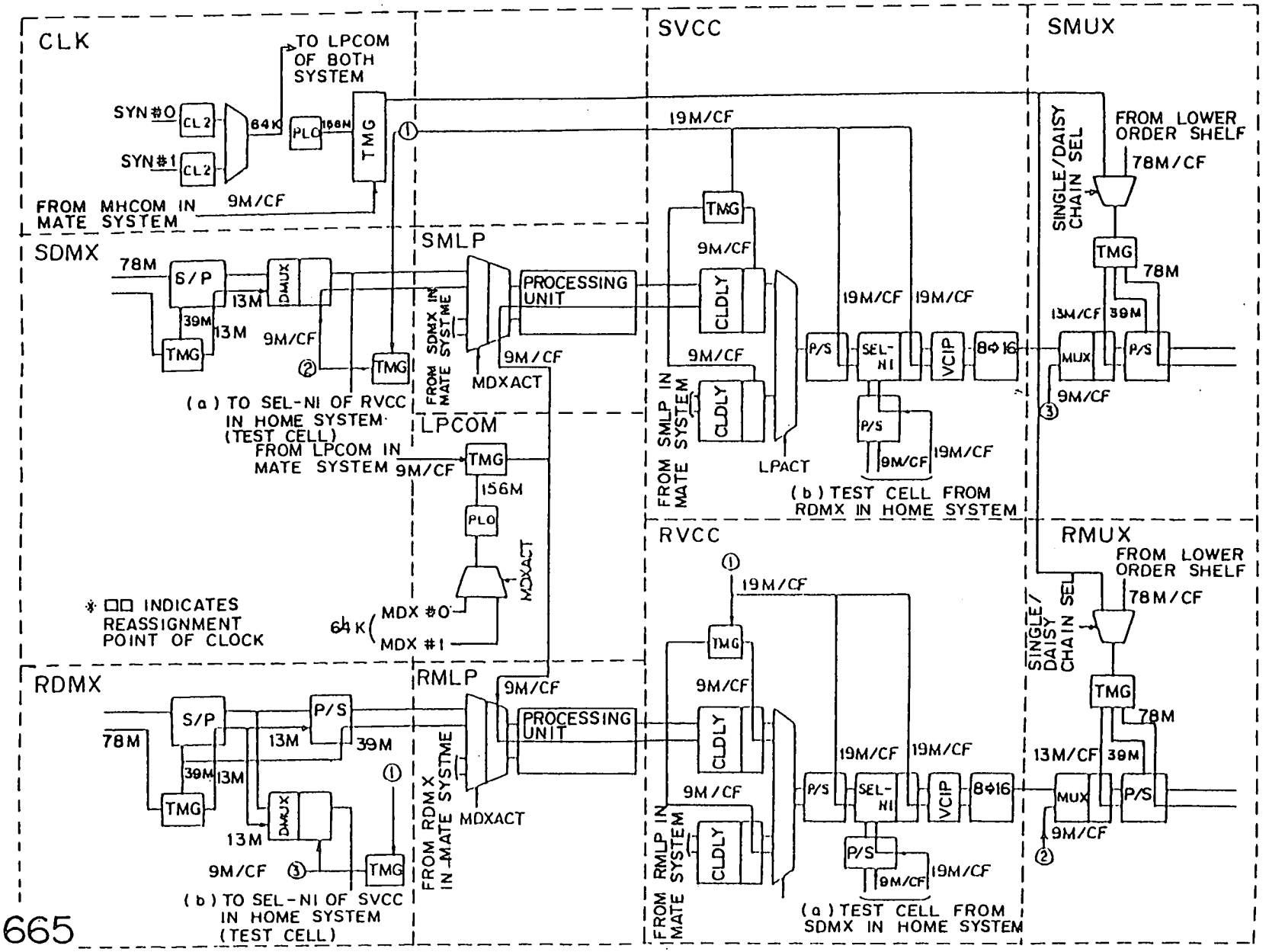


FIG. 665

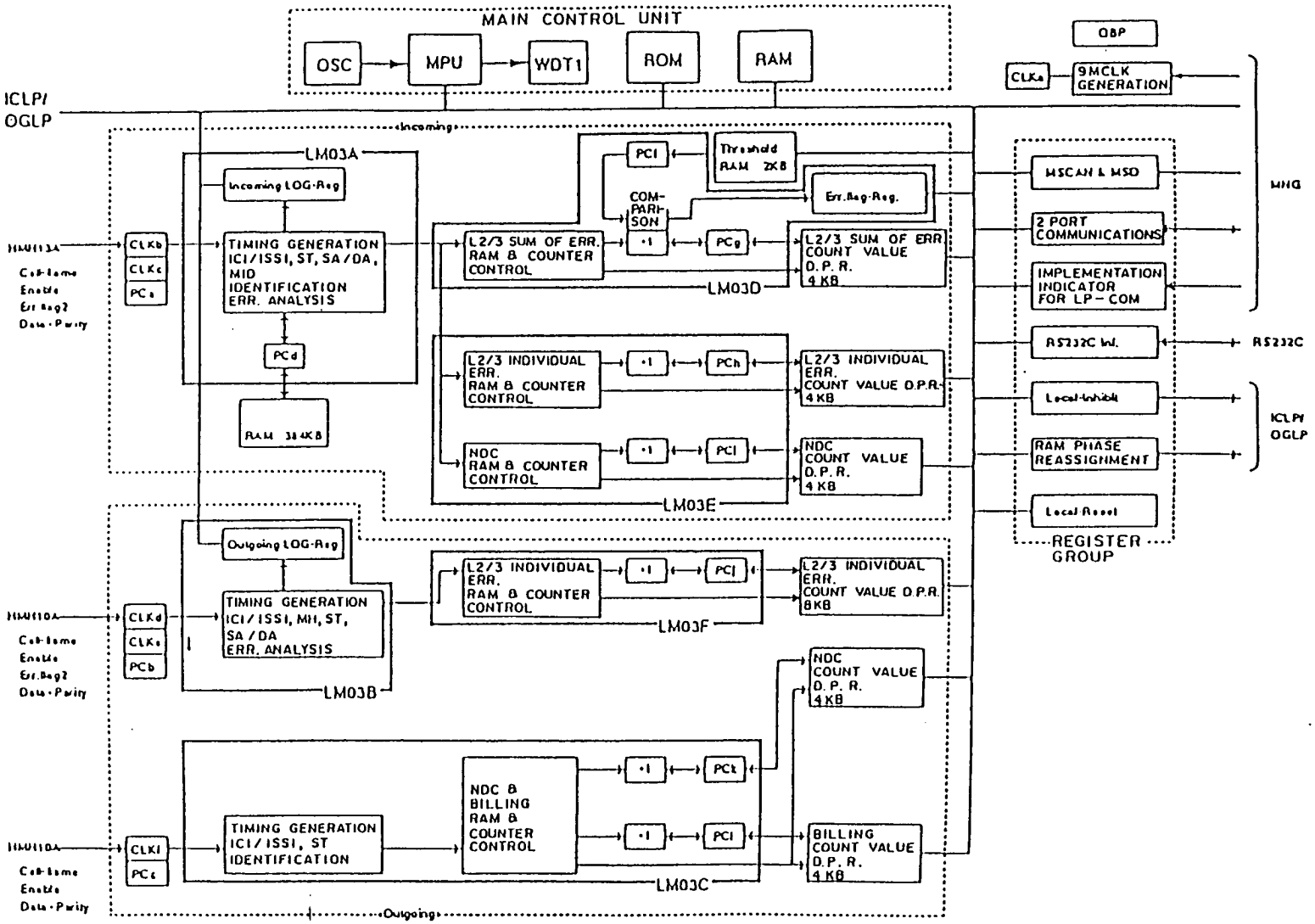

MAIN CONTROL UNIT
OSC
MPU
WDT1
ROM
RAM
OBP
CLKa
9MCLK GENERATION
ICLP/ OGLP
Incoming
LM03A
Incoming LOG-Reg
TIMING GENERATION ICI/ISSI, ST, SA/DA, MID IDENTIFICATION ERR. ANALYSIS
PCd
RAM 384KB
CLKb
CLKc
PCa
PCI
Threshold RAM 2KB
COM-PARI-SON
Err.Reg-Reg.
L2/3 SUM OF ERR. RAM B COUNTER CONTROL
+1
PCg
L2/3 SUM OF ERR COUNT VALUE D.P.R. 4KB
LM03D
L2/3 INDIVIDUAL ERR. RAM B COUNTER CONTROL
PCh
L2/3 INDIVIDUAL ERR. COUNT VALUE D.P.R. 4KB
NDC RAM B COUNTER CONTROL
NDC COUNT VALUE D.P.R. 4KB
LM03E
Outgoing LOG-Reg
TIMING GENERATION ICI/ISSI, MH, ST, SA/DA ERR. ANALYSIS
CLKd
CLKe
PCb
L2/3 INDIVIDUAL ERR. RAM B COUNTER CONTROL
L2/3 INDIVIDUAL ERR. COUNT VALUE D.P.R. 8KB
LM03F
LM03B
NDC COUNT VALUE D.P.R. 4KB
TIMING GENERATION ICI/ISSI, ST IDENTIFICATION
CLKf
PCc
NDC B BILLING RAM B COUNTER CONTROL
PCk
BILLING COUNT VALUE D.P.R. 4KB
LM03C
Outgoing
MSCAN & MSD
2 PORT COMMUNICATIONS
IMPLEMENTATION INDICATOR FOR LP-COM
RS232C I/F
RAM PHASE REASSIGNMENT
Local Reset
REGISTER GROUP
MNG
RS232C
ICLP/ OGLP

FIG. 666

BLOCK		FUNCTIONS
MAIN CONTROL UNIT	MPU	16BIT MICROPROCESSOR (80C186-10)
	RAM	FOR FIRMWARE WORK 128K ×16BIT SRAM
	ROM	FOR STORING FIRMWARE 64K×16BIT EPROM
	OCS	16MHz OSCILLATOR
REGISTER GROUP	MSCN & MSD	MSCN:AREA THROUGH WHICH NG OF EACH CHECK (REFER TO LIST IN FIGURE 6.1.2) IS REPORTED TO HLP07A.
		MSD: AREA THROUGH WHICH PSEUDO FAULT IS SET FROM HLP07A
	2PORT COMMUNICATIONS	ACTIVATING/RELEASING INTERRUPTION MADE DURING COMMUNICATIONS TO HLP07A.
	LP-COM IMPLEMENTATION	INDICATING IMPLEMENTATION OF LP-COM AND OTHER PWCB (HLP07A AND HLM02A).
	RS232C INF	INTERFACE WITH WORK STATION FOR DEBUGGING
	LOCAL-INHIBIT	INITIALIZE INSTRUCTION FOR PM/TM COUNT VALUE STORING RAM
	RAM PHASE REASSIGNMENT	HARDWARE ACCESS PHASE INSTRUCTION FOR PM/TM COUNT VALUE STORING TWO PHASE CONSTRUCTION RAM
	LACAL-RESET	INTERNAL RESET
CLK GENERATION		GENERATING 9MCLK USING 19MCLK AND 19MFP FROM HLP07A.
OBP		CONVERTING ON BOARD POWER 048V INTO +5V

FIG. 667

BLOCK		FUNCTION
INCOMING		COUNTING L2/3 SUM OF ERROR, L2/3 INDIVIDUAL ERROR. NETWORK DATA COLLECTION AT INCOMING TERMINAL.
	TIMING GENERATION	GENERTING EACH TIMING ACCORDING TO 9MFLK, CELL-FRAME (CF), AND ENABLE (EN) SIGNAL.
	ICI/ISSI, ST SA/DA, MID IDENTIFICATION	IDENTIFYING SOURCE ICI/ISSI, SEGMENT TYPE, SA/DA, AND MID FROM CELL DATA.
	ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (EF).
	INCOMING LOG-REG.	AREA THROUGH WHICH ERROR TYPE, SOURCE ICI/ISSI, SA, AND DA ARE REPORTED TO FIRMWARE WHEN LOG OBJECT ERROR HAS OCCURRED
	SA/DA ACCUMULATION RAM	RAM ACCUMULATING SA AND DA TO COLLECT LOG.
	THRESHOLD RAM	SETTING THRESHOLD OF L2/3 SUM OF ERROR AT INITIALIZATION.
	L2/3 SUM OF ERR. COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUE OF L2/3 SUM OF EEROR.
	ERR. FLAG-REG.	AREA THROUGH WHECH SUM OF ERROR VALUE EXCEEDING THRESHOLD IS REPORTED TO FIRMWARE.
	L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR.
	NDC COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUE RELATED TO NETWORK DATA COLLECTION
OUTGOING		COUNTING L2/3 INDIVIDUAL ERROR, NETWORK DATA COLLECTION, AND BILLING PROCESSES AT OUTGOING TERMINAL.
	TIMING GENERATION	GENERATING EACH TIMING ACCORDING TO 9MCLK, CELL-FRAME(CF), AND ENABLE (EN) SIGNAL.
	ICI/ISSI, MH ST, SA/DA, MID IDENTIFICATION	IDENTIFYING DESTINATION ICI/ISSI, DESTINATION MH, SEGMENT TYPE, SA/DA, AND MID ACCORDING TO CELL DATA.
	ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (EF) SIGNAL
	OUTGOING LOG-REG.	AREA THROUGH WHICH ERROR TYPE, DESTINATION ICI/ISSI, SA, AND DA ARE REPORTED TO FIRMWARE WHEN LOG OBJECT ERROR HAS OCCURRED
	L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR.
	NDC COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUE RELATED TO NETWORK DATA COLLECTION.
	BILLING COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUES RELATED TO BILLING OPERATIONS.

FIG. 668

0,356,526

CHECK NAME	CHECK OBJECT
CLKa	19M CLOCK FROM HLP07A, AND DISCONNECTION OF FRAME PULSE
CLKb	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF CELL FRAME FROM INCOMING LP
CLKc	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF ERROR FLAG 2 FROM INCOMING LP
CLKd	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF CELL FRAME FROM OUTGOING LP
CLKe	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF ERROR FLAG 2 FROM OUTGOING LP
CLKf	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF CELL FRAME FRAME FROM OUTGOING LP
WDTI	TIME OUT OF WATCHDOG TIMER, AND DISCONNECTION MPU OUTPUT 8M CLOCK
PCa	DATA FROM INCOMING LP, PARITY CHECK OF ENABLE
PCb	DATA FROM OUTGOING LP, PARITY CHECK OF ENABLE
PCc	DATA FROM OUTGOING LP, PARITY CHECK OF ENABLE
PCd	PARITY CHECK OF SA/DA ACCUMULATION RAM
PCf	PARITY CHECK OF THRESHOLD RAM
PCg	PARITY CHECK OF L2/3 SUM F ERR. COUNT VALUE D.P.RAM
PCh	PARITY CHECK IF INCOMING L2/3 INDIVIDUAL ERR. COUNT VALUE D.P.RAM
PCi	PARITY CHECK OF INCOMING NDC COUNT VALUE D.P.RAM
PCj	PARITY CHECK OF OUTGOING L2/3 INDIVIDUAL ERR. COUNT VALUE D.P.RAM
PCk	PARITY CHECK OF OUTGOING NDC COUNT VALUE D.P.RAM
PCl	PARITY CHECK OF BILLING COUNT VALUE D.P.RAM

FIG. 669

CHECK NAME	CHECK CONDITIONS
PCd	NOTIFICATION OF LOG-REQUIRED ERROR FROM INCOMING LP
PCf	NOTIFICATION OF ERROR RELATED TO L2/3 SUM OF ERROR FROM INCOMING LP
PCg	NOTIFICATION OF ERROR RELATED TO L2/3 SUM OF ERROR FROM INCOMING LP
PCh	NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM INCOMING LP
PCi	NOTIFICATION OF NDC INDIVIDUAL COUNT ERROR FROM INCOMING LP
PCj	NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM OUTGOING LP

FIG. 670

GROUP	ITEM	LEVEL	CHECK	No	ERROR GENE-RATING CELL	ACTION
A	1	L 2	MRI. TIME OUT	2	EOM (PSEUDO EOM)	COUNT
B	1	L 2	INVALID PAYLOAD CRC CODE	3	BOM, COM, EOM	DISCARD COUNT
C	1	L 2	PAYLOAD LENGTH REEOR	4	BOM, COM, EOM	DISCARD COUNT
D	1	L 2	BOM WITH UNEXPECTED MID	5	BOM	COUNT
	2	L 2	EOM WITH UNEXPECTED MID	5	EOM	DISCARD COUNT
E	1	L 2	UNEXPECTED SN ERROR	6	COM, EOM	DISCARD COUNT
F	1	L 3	INVALID BASIZE FIELD VALUE	7	BOM	DISCARD COUNT
	2	L 3	INVALID DA TYPE	8	BOM	DISCARD COUNT
	3	L 3	INVALID SA TYPE	9	BOM	DISCARD COUNT
	4	L 3	INVALID SERVICE TYPE (ISSI)	11	BOM	DISCARD COUNT LOG
	5	L 3	INVALID PROTOCOL ID (ICI)	11	BOM	DISCARD COUNT LOG
	6	L 3	INVALID PROTOCOL DESCRIMINATOR	13	BOM	DISCARD COUNT LOG
	7	L 3	HOP COUNT = 0	15	BOM	DISCARD COUNT LOG
	8	L 3	INVALID INGRESS INTERFACE TYPE	16	BOM	DISCARD COUNT LOG
	9	L 3	BETAG MISMATCH	18	EOM	DISCARD COUNT
G	1	UNIQUE	MID ASSIGNED ERROR	20	BOM	DISCARD COUNT
	2	UNIQUE	EXCEED MAXIMUM NUMBER OF CDU	21	BOM	DISCARD COUNT
	3	UNIQUE	ROUTING ERROR	22	BOM	DISCARD COUNT
	4	UNIQUE	BASIZE ≠ LENGTH	23	EOM	DISCARD COUNT
	5	UNIQUE	ENCAPSULATION ERROR	24	SSM	DISCARD COUNT

FIG. 671

6656260 2122260

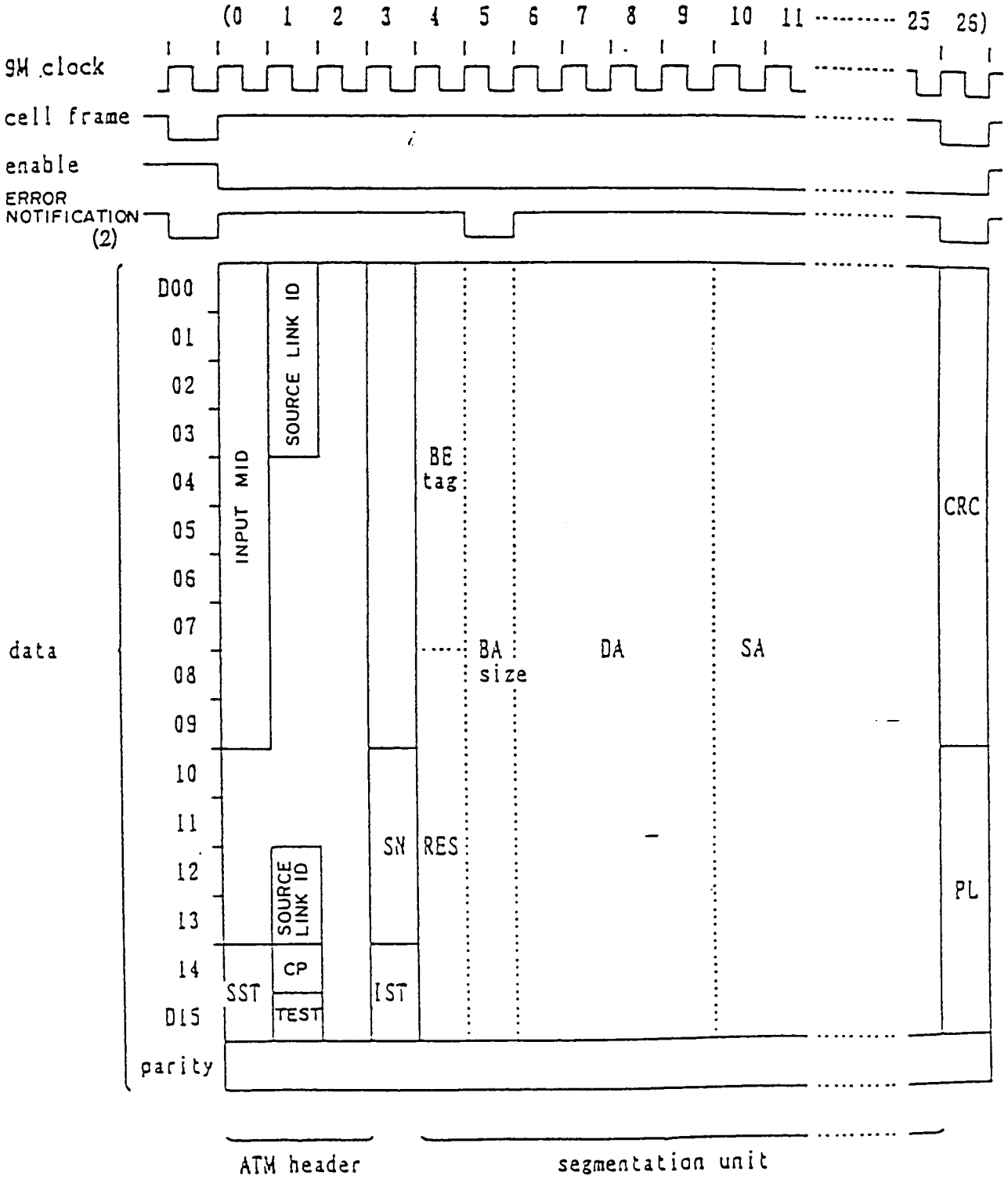


FIG. 672

SIGNAL NAME	POLARITY	EXPLANATION
9M CLOCK	—	ALL SIGNALS STARTING WITH REFERENCE CLOCK ARE CHANGED AT RISE OF MAIN CLOCK.
CELL FRAME	⇨	SIGNAL INDICATING BOUNDARY OF CELL. L FOR ONLY LAST 1 τ OF CELL.
ENABLE	⇨	SIGNAL INDICATING VALID/INVALID CELL. ALL CELL AREAS ARE L WHEN VALID.
ERROR NOTIFICATION (2)	⇨	SIGNAL INDICATING ERROR TYPE. DETAILED EXPLANATION IS GIVEN LATER AND ERROR IS REPRESENTED BY L.
DATA	PLUS	16 PARALLEL DATA + PARITY. PARITY IS ODD PARITY FOR ALL 17 BITS OF 16 BIT PARALLEL DATA + ENABLE.

FIG. 673

	SST	IST
Inter-BOM	1 0	1 0
SIP-BOM	1 0	0 0
COM	0 0	0 0
EOM	0 1	0 1
SIP-SSM	1 1	0 1

FIG. 674

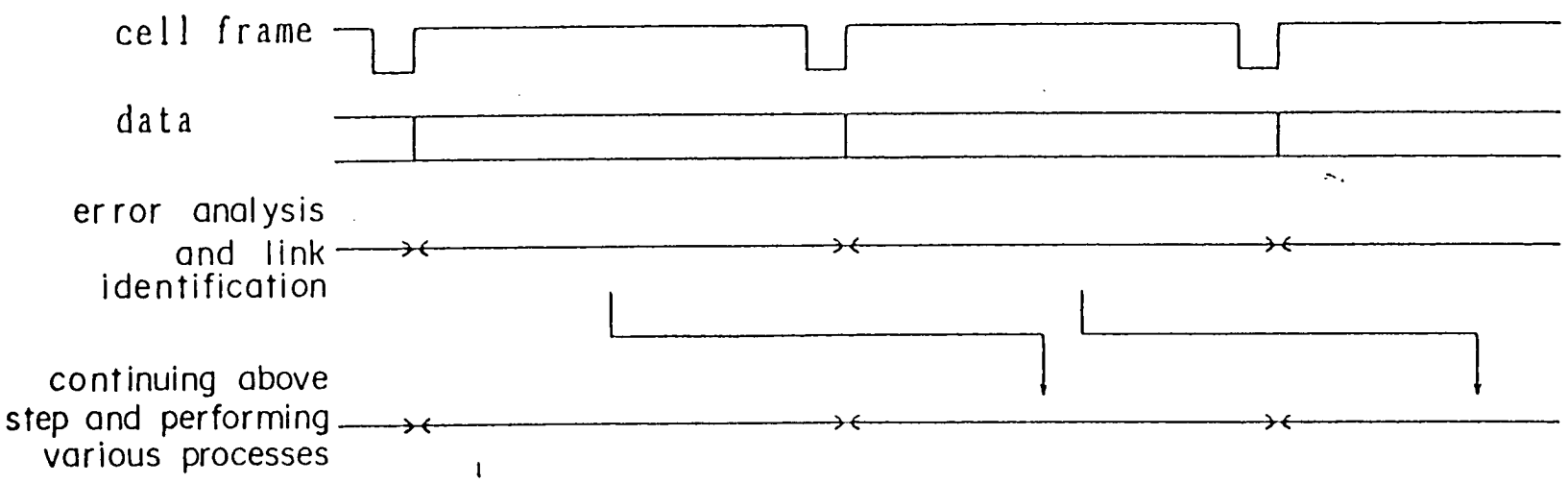

cell frame
data
error analysis and link identification
continuing above step and performing various processes

FIG. 675

Group	Item	Level	Check	No.	Error generating cell	Action
A	1	L2	MRI time out	1	EOM(Pseudo-EOM)	Count
B	1	L2	MID currently active	4	BOM	Count
	2	L2	EOM with unapproved MID	4	EOM	Count of discard
C	1	L2	Unexpected SN error	5	BOM, COM, EOM	Count of discard
D	1	L3	ISSI/ICI Unavailable	7	BOM	Count Log of discard
E	1	Unique	Exceed maximum number of CDU	8	BOM	Count of discard
	2	Unique	Encapsulation Error	1	SSM	Count of discard

FIG. 676

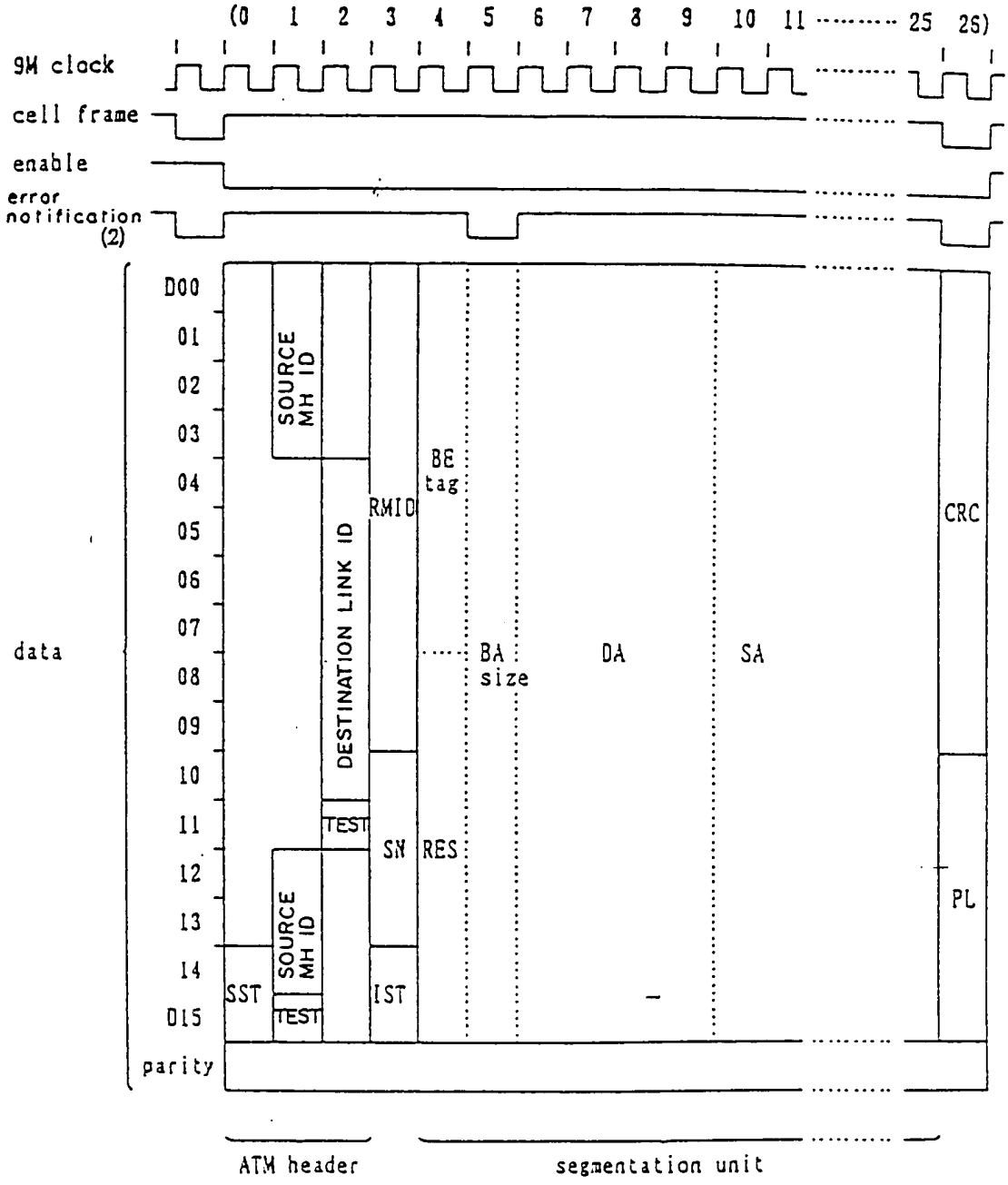

(0 1 2 3 4 5 6 7 8 9 10 11 ..... 25 26)
9M clock
cell frame
enable
error notification (2)
data
D00
01
02
03
04
05
06
07
08
09
10
11
12
13
14
D15
parity
SOURCE MH ID
DESTINATION LINK ID
RMID
BE tag
CRC
BA size
DA
SA
TEST
SN
RES
PL
SST
SOURCE MH ID
TEST
IST
ATM header
segmentation unit

FIG. 677

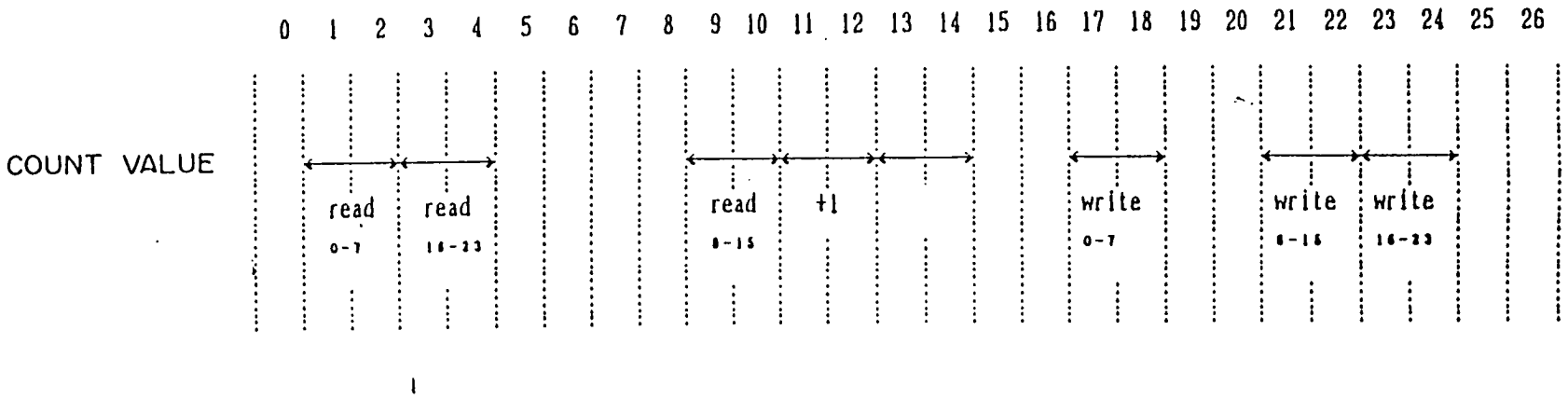

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
COUNT VALUE
read
0-7
read
16-23
read
8-15
+1
write
0-7
write
8-15
write
16-23

FIG. 678

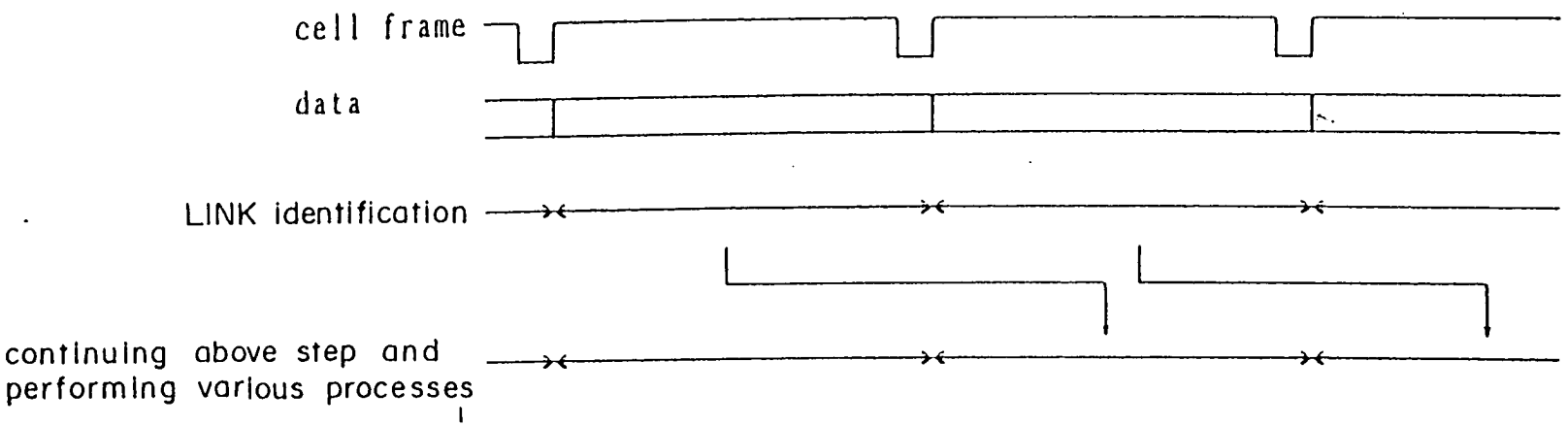

cell frame
data
LINK identification
continuing above step and performing various processes

FIG. 679

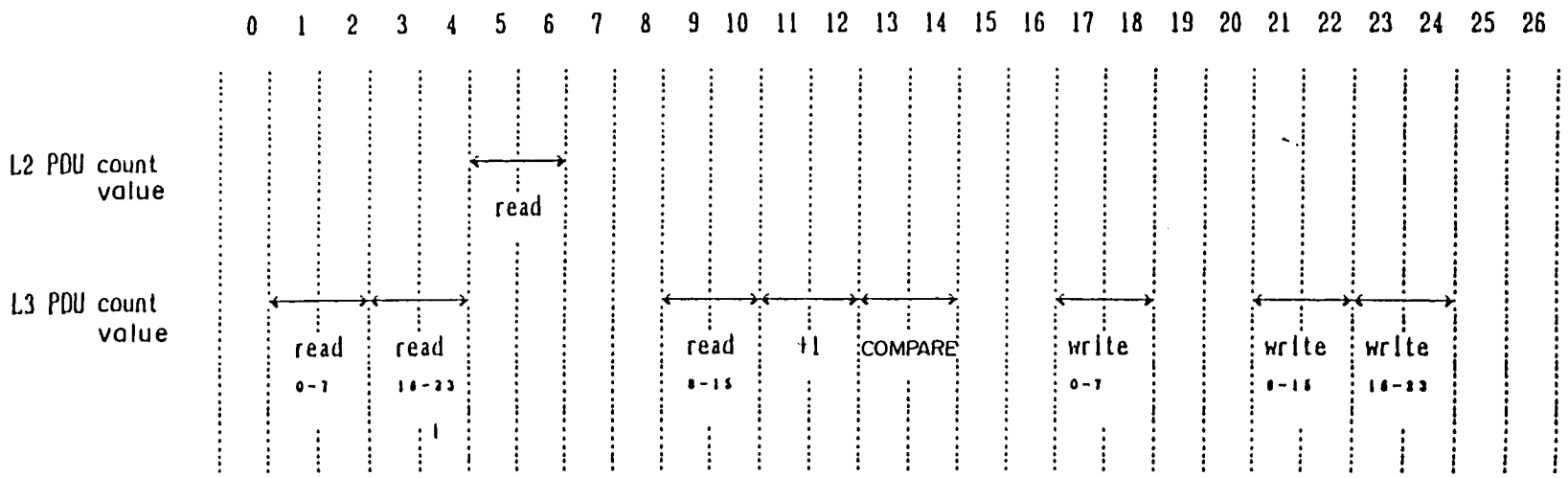

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
L2 PDU count value
L3 PDU count value
read
read
0-7
read
16-23
read
8-15
+1
COMPARE
write
0-7
write
8-15
write
16-23

FIG. 680

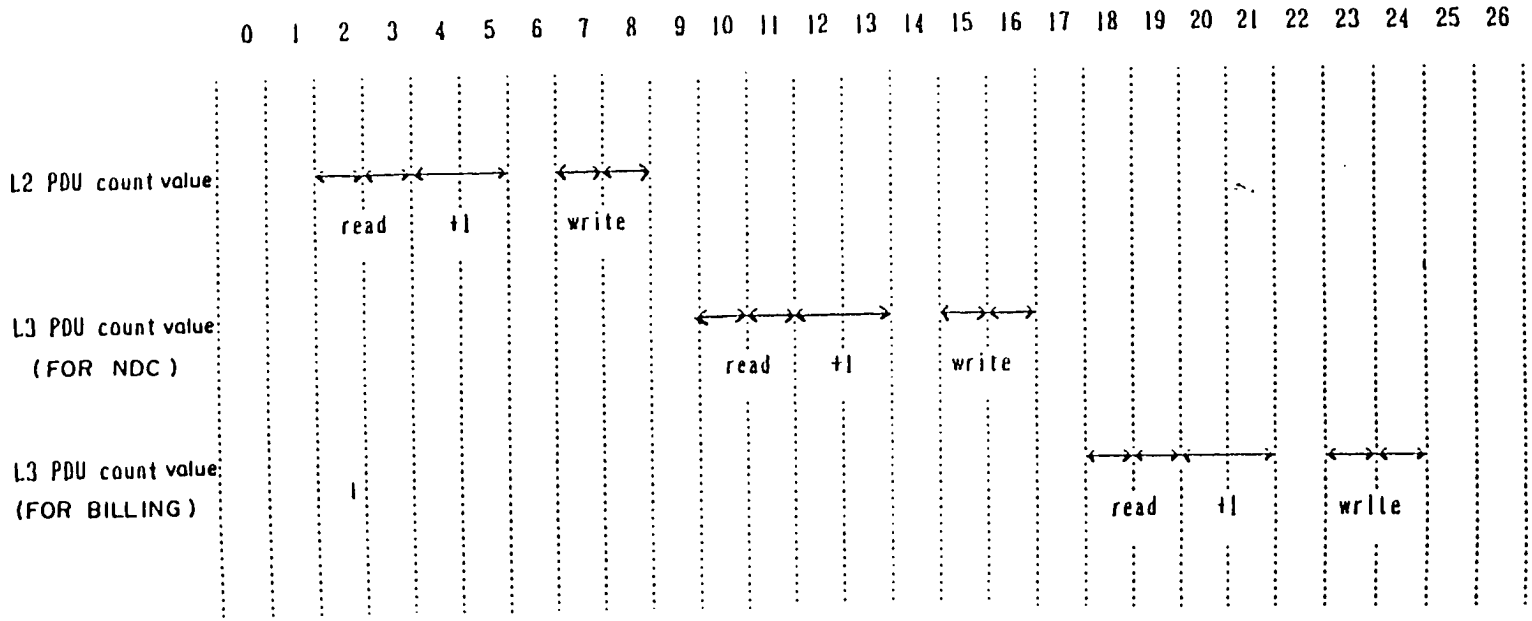

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
L2 PDU count value
read
+1
write
L3 PDU count value
(FOR NDC)
read
+1
write
L3 PDU count value
(FOR BILLING)
read
+1
write

FIG. 681

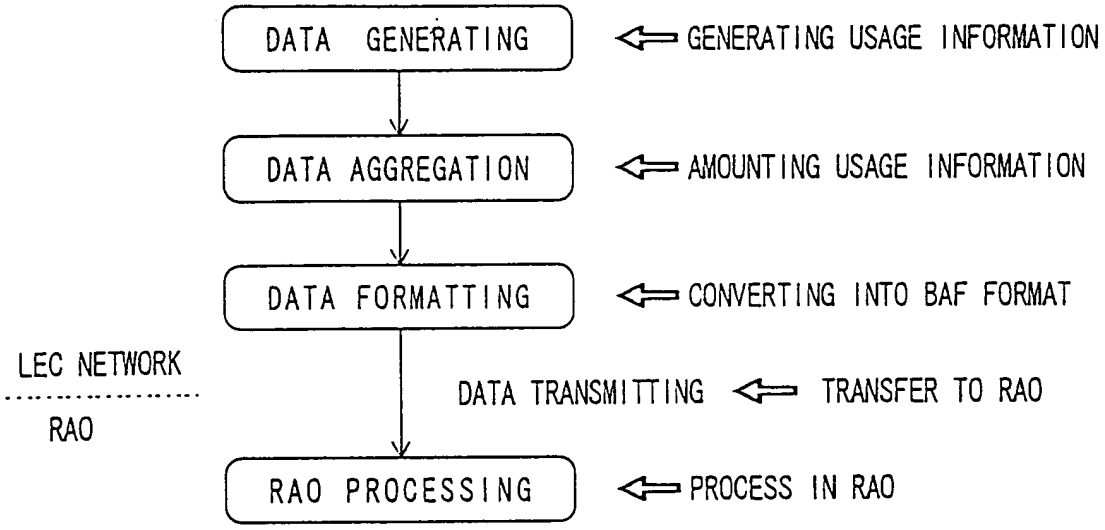

DATA GENERATING
GENERATING USAGE INFORMATION
DATA AGGREGATION
AMOUNTING USAGE INFORMATION
DATA FORMATTING
CONVERTING INTO BAF FORMAT
LEC NETWORK
RAO
DATA TRANSMITTING
TRANSFER TO RAO
RAO PROCESSING
PROCESS IN RAO

FIG. 682

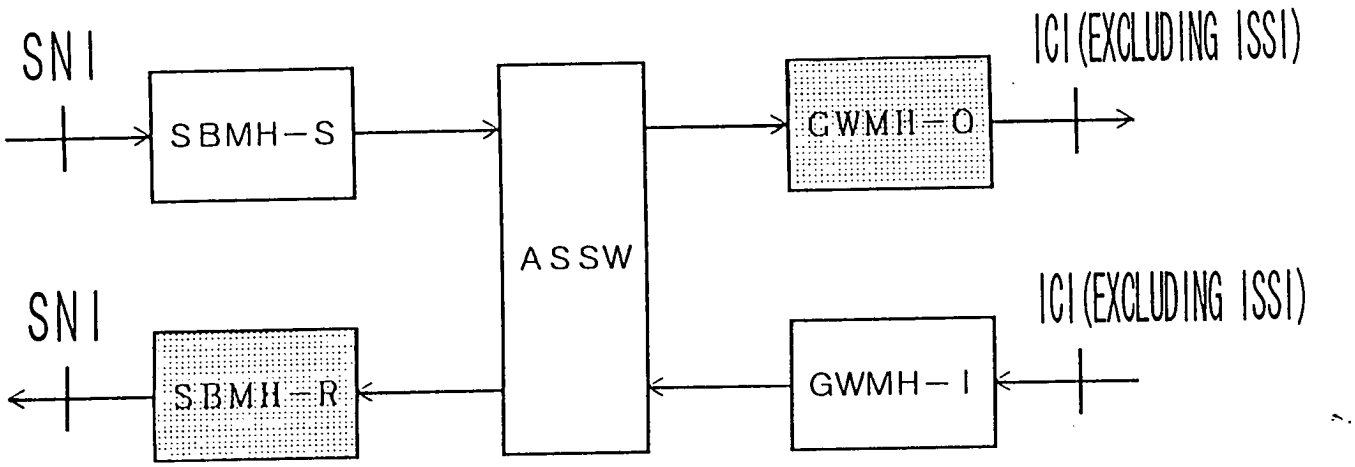

SNI
SBMH-S
ASSW
GWMH-O
ICI (EXCLUDING ISSI)
SNI
SBMH-R
GWMH-I
ICI (EXCLUDING ISSI)

FIG. 683

	FIGURE	LEC Network Function	SA	DA	SNI Add	Incoming NW ID	Incoming ICI TPS ID	Outgoing NW ID	Outgoing ICI TPS ID	Carrier ID	Cond Code	Packet Count	Seg. Count	Ingress Inf Type
INDIVIDUAL ADDRESS DATA TRANSFER	1	Orig. XA-SMDS (ICI)	O	O		*	*	O	O		O	O	O	O (CIC)
	2	Source Function for Exchange SMDS (ICI)	O	O		*	*	O	O		O	O	O	O (NBCA)
	7	Term. XA-SMDS (SNI)	O	O		O	O				O	O	O	O (CIC)
	8	Dest. Function for Exchange SMDS (SNI)	O	O		O	O				O	O	O	O (NBCA)
GROUP ADDRESS DATA TRANSFER	1	Orig. XA-SMDS (ICI)	O	O	O	*	*	O	O		O	O	O	O
	2	Source Function for Exchange SMDS and Orig. XA-SMDS (ICI)	O	O	O	*	*	O	O		O	O	O	O
	3	Term. XA-SMDS (ICI)	O	O	O	O	O	O	O		O	O	O	O
	4	Dest. Function for Exchange SMDS (ICI)	O	O	O	O	O	O	O		O	O	O	O
	5	Dest. Function for Orig. XA-SMDS (ICI)	O	O	O	O	O	O	O		O	O	O	O
	6	Source Function for Term. XA-SMDS (ICI)	O	O	O	O	O	O	O		O	O	O	O
	7	Term. XA-SMDS (SNI)	O	O	O	O	O			O	O	O	O	O
	8	Dest. Function for Exchange SMDS (SNI)	O	O	O	O	O			O	O	O	O	O
	9	Dest. Function for Term. XA-SMDS (SNI)	O	O	O	O	O			O	O	O	O	O

O : REQUIRED. * : SETTING 0. NO MARK : NOT REQUIRED.

FIG. 684

IP)+RDA(ICIP)+RSA+RCA

0	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
1	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
2	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
⋮	⋮
FFFD	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
FFFE	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
FFFF	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit

FIG. 685

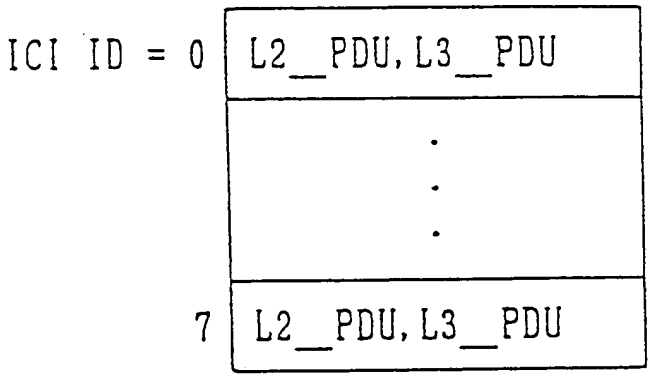


FIG. 686

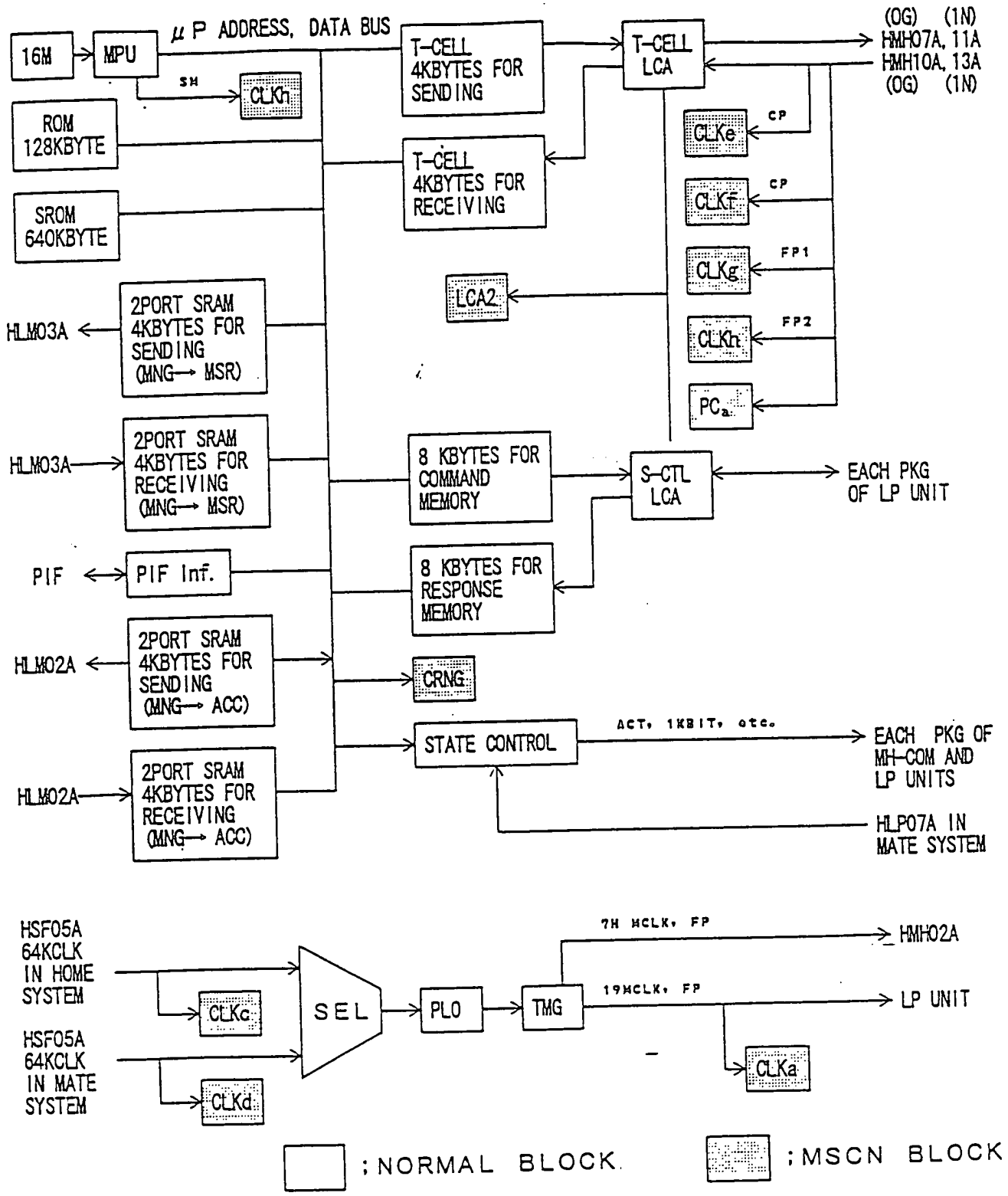

16M
MPU
μP ADDRESS, DATA BUS
5M
CLKh
ROM 128KBYTE
SROM 640KBYTE
T-CELL 4KBYTES FOR SENDING
T-CELL 4KBYTES FOR RECEIVING
T-CELL LCA
(OG) (1N)
HMH07A, 11A
HMH10A, 13A
(OG) (1N)
CLKe
CP
CLKf
CP
CLKg
FP1
CLKh
FP2
PCa
LCA2
HLM03A
2PORT SRAM 4KBYTES FOR SENDING (MNG→MSR)
HLM03A
2PORT SRAM 4KBYTES FOR RECEIVING (MNG→MSR)
8 KBYTES FOR COMMAND MEMORY
S-CTL LCA
EACH PKG OF LP UNIT
PIF
PIF Inf.
8 KBYTES FOR RESPONSE MEMORY
HLM02A
2PORT SRAM 4KBYTES FOR SENDING (MNG→ACC)
CRNG
STATE CONTROL
ACT, 1KBIT, etc.
EACH PKG OF MH-COM AND LP UNITS
HLM02A
2PORT SRAM 4KBYTES FOR RECEIVING (MNG→ACC)
HLP07A IN MATE SYSTEM
HSF05A 64KCLK IN HOME SYSTEM
CLKc
SEL
PLO
TMG
7H HCLK, FP
HMH02A
19HCLK, FP
LP UNIT
CLKa
HSF05A 64KCLK IN MATE SYSTEM
CLKd
; NORMAL BLOCK
; MSCN BLOCK

FIG. 687

BLOCK NAME	FUNCTION
16M	GENERATING 16 MHz CLOCK FOR MICROPROCESSOR
MPU	μP (80C186)
ROM	STORING FIRMWARE FOR MPU
FOR SENDING T-CELL	MEMORY FOR SENDING TEST CELL
FOR RECEIVING T-CELL	MEMORY FOR RECEIVING TEST CELL
T-CELL LCA	SENDING TEST CELL FOR HMH01A AND 03A, (ASSIGNING ODD PARITY, ADJUSTING TIMING), RECEIVING TEST CELL FROM HMH02A AND 06A, MAKING PARITY CHECK, ETC.
SRAM	WORK MEMORY FOR MPU
FOR SENDING 2 PORT SRAM MNG →MSR	DATA SENDING MEMORY FOR MSR-FIRMWARE
FOR RECEIVING 2 PORT SRAM MNG ←MSR	DATA RECEIVING MEMORY FROM MSR-FIRMWARE
FOR SENDING 2 PORT SRAM MNG →ACC	DATA SENDING MEMORY FOR ACC-FIRMWARE
FOR RECEIVING 2 PORT SRAM MNG ←ACC	DATA RECEIVING MEMORY FROM ACC-FIRMWARE
INF inf	CONTROLLING INTERFACE WITH INF
FOR COMMAND MEMORY	SRAM FOR SENDING COMMAND
FOR RESPONSE MEMORY	SRAM FOR RECEIVING RESPONSE
S-CTL LCA	CONTROLLING COMMAND AND RESPONSE FOR LP UNIT
STATE CONTROL	CONTROLLING ACT, INHBIT, ETC. CONTROLLING OCS TO MATE SYSTEM
SEL	SELECTING 64 KHz CLOCK RECEIVED FROM MH-COM OF HOME AND MATE SYSTEMS.
PLO	SELECTING 155 MHz CLOCK IN SYNCHRONISM WITH 64 MHz CLOCK.
TMG	GENERATING 78 MHz AND 19 MHz CLOCKS FROM 155 MHz CLOCK.

FIG. 688

BLOCK NAME	FUNCTION
CLKb	μP OPERATION 8 M CLOCK DISCONNECTION
CLKe	DISCONNECTION OF SENDING CELL FRAME (COMMON BETWEEN ICLP AND OGLP)
CLKf	DISCONNECTION OF RECEIVING CELL FRAME (COMMON BETWEEN ICLP AND OGLP)
CLKg	DISCONNECTION OF ERROR FLAG 1 (COMMON BEWEEN ICLP AND OGLP)
CLKh	DISCONNECTION OF ERROR FLAG 2 (COMMON BEWEEN ICLP AND OGLP)
PCa	RECEIVING CELL DATA PARITY NG (COMMON BEWEEN ICLP AND OGLP)
LCA2	HLP07A LCA CONFIGURATION NG
CRNG	ABNORMAL COMMAND AND RESPONSE AT S-CTL1
CLKc	HOME SYSTEM 64K CLOCK DISCONNECTION
CLKd	MATE SYSTEM 64K CLOCK DISCONNECTION
CLKa	19M CLOCK/FRAME PULSE DISCONNECTION

FIG. 689

MESH AT RECEVING UNIT		REMARKS	MESH AT SENDING UNIT		REMARKS
VPI	VCI		VPI	VCI	
"000"H	"03FC"H	COMMUNICATIONS CELL IN #0 SYSTEM	"0AA"H	"0000"H ~ "03FF"H	VPI : BSGC CARD NUMBER VCI : BSGC PORT NUMBER "03FF"H, "03FB"H FOR TEST USE
"000"H	"03FD"H	COMMUNICATIONS CELL IN #1 SYSTEM			

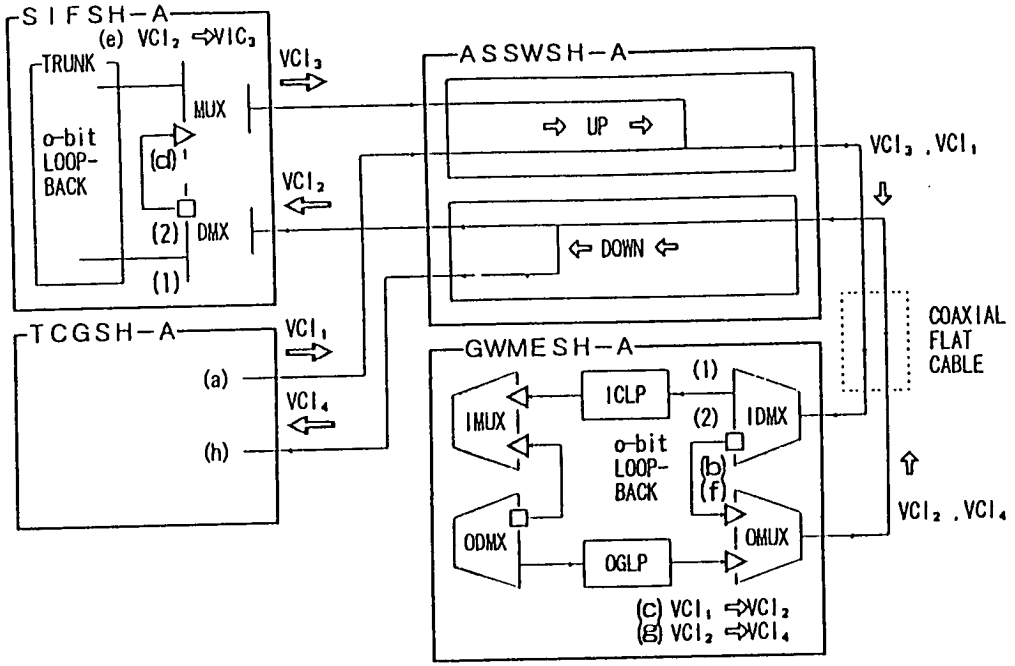
FIG. 690

ITEM	FAULT TYPE	NOTIFICATION METHOD	NOTIFYING SYSTEM	TEST DEVICE	ACTION					PROCEDURE	REMARKS
					ASSW SYSTEM SWITCH	FAULT BLOCK	FAULT MASSAGE	ALM LIGHTING	DIAGNOSTICS PROCESS		
1	HARDWARE FAULT EXCLUDING SIGNAL PROCESSING UNIT AND OMUX.	HOME SYSTEM	ACT	ACT MHCOM	○	○	○	○	○ PREVIOUSLY ACT	②	DIAGNOSTICS IS ACTIVATED BY MATE SYSTEM.
			SBY	SBY MHCOM	—	○	○	○	○ SBY	①	
2	HARDWARE FAULT OF SIGNAL PROCESSING UNIT AND OMUX.	MATE SYSTEM E-MSCN	ACT	SBY MHCOM	—	○	○	○	○ SBY	③	
			SBY	ACT MHCOM	○	○	○	○	○ PREVIOUSLY ACT	④	
3	OBP FAULT	MATE SYSTEM E-MSCN	ACT	SBY MHCOM	—	○	○	○	○ SBY	③	
			SBY	ACT MHCOM	○	○	○	○	○ PREVIOUSLY ACT	④	
4	MATE POWER SOURCE PWCB FAULT (FUSE DISCONNECTION)	MATE SYSTEM E-MSCN	ACT	SBY POWER SOURCE PWCB	—	○	○	○	○ SBY	③	IMCOM PROVIDED BY POWER SOURCE PWCB IS BLOCKED, AND ASSWSH-A IN HOME SYSTEM IS ALSO BLOCKED.
			SBY	ACT POWER SOURCE PWCB	○	○	○	○	○ PREVIOUSLY ACT	④	

FIG. 691

VPI	VCI	UL	TAGA	TAGB	TAGC	COM	SIG	0
ALL '0'	03FA OR 03FB	0	2.4G HW NUMBER (0-3 FOR CARD NUMBER OF ASSW HMX03A)	622M HW NUMBER (0-3 FOR HW NUMBER IN ASSW HMX03A)	155M HW NUMBER (0-3 FOR SH NUMBER OF GWMESH)	0	0	1

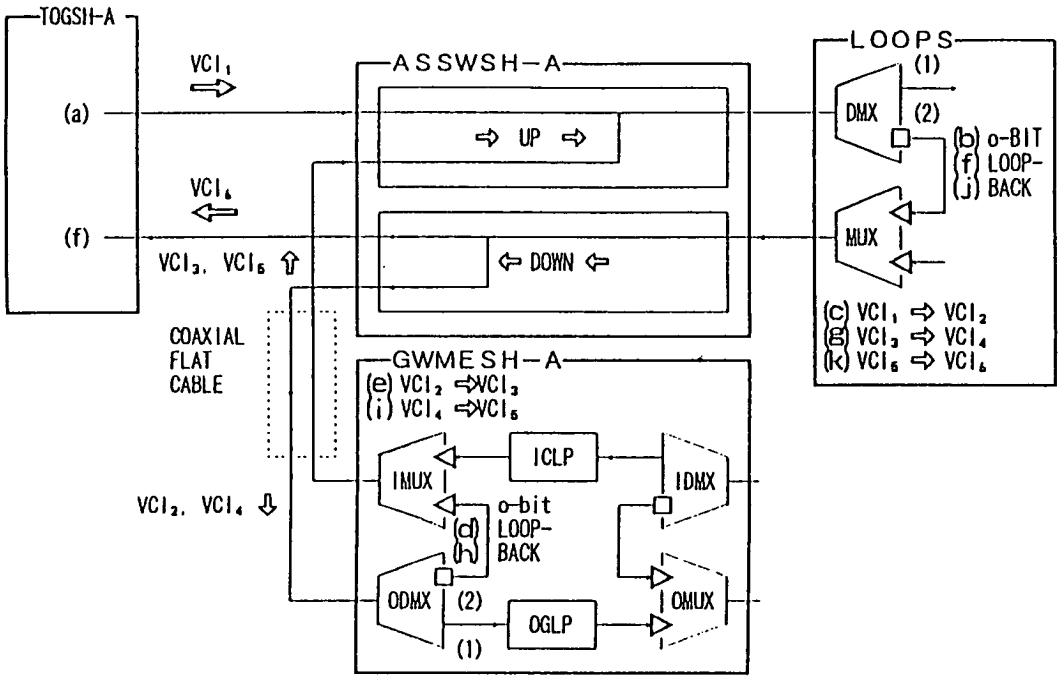
FIG. 692



(a) GENERATING TEST CELL(O BIT IS 1) OF VCI_1 AND SWITCHING TAG FOR IDMX FROM, TCGSH-A
(b) DROPPING CELL OF O-BIT=1 AT IDMX AND LOOPING IT BACK TO OMUX.
(c) CONVERTING $VCI=VCI_1$ INTO VCI_2 AT OMUX AND PROCESSING IA AS TEST CELL OF SWITCHING TAG FOR TRUNK.
(d) DROPPING CELL OF O-BIT=1 AT DMX OF SIFSH-A HAVING TRUNK AND LOOPING IT BACK TO MUX.
(e) CONVERTING $VCI=VCI_2$ INTO VCI_3 AT MUX AND PROCESSING IS AS TEST CELL OF SWITCHING TAG FOR IDMX.
(f) DROPPING CELL OF O-BIT=1 AT IDMX AND LOOPING IT BACK TO OMUX.
(g) CONVERTING $VCI=VCI_3$ INTO VCI_4 AT OMUX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR TCGSH-A.
(h) CHECKING CONTENTS OF TEST CELL AT TCGSH-A.

NOTE : DROP ONLY FOR □ :O-BIT=1 ◁ ▷: VCC

FIG. 693



(a) GENARATING TEST CELL (O BIT IS 1) OF VCI_1 AND SWITCHING TAG FOR LOOP FROM TCGSH-A
(b) DROPPING CELL OF O-BIT=1 AT LOOP AND LOOPING IT BACK TO MUX.
(c) CONVERTING VCI=VCI_1 INTO VCI_2 AT MUX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR ODMX.
(d) DROPPING CELL OF O-BIT=1 AT ODMX AND LOOPING IT BACK TO IMUX.
(e) CONVERTING VCI=VCI_2 INTO VCI_3 AT IMUX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR LOOP.
(f) DROPPING CELL OF O-BIT=1 AT LOOP AND LOOPING IT BACK TO MUX.
(g) CONVERTING VCI=VCI_3 INTO VCI_4 AT MUX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR ODMX.
(h) DROPPING CEL OF O-BIT=1 AT ODMX AND LOOPING IT BACK TO IMUX.
(i) CONVERTING VCI=VCI_4 INTO VCI_5 AT IUX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR LOOP.
(j) DROPPING CELL OF O-BIT=1 AT LOOP AND LOOPING IT BACK TO MUX.
(k) CONVERTING VCI=VCI_5 INTO VCI_6 AT MUX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR TCGSH-A.
(l) CHECKING CONTENTS OF TEST CELL AT TCGSH-A

NOTE : DROP ONLY FOR □ :O-BIT=1 ◁ ▷: VCC

FIG. 694

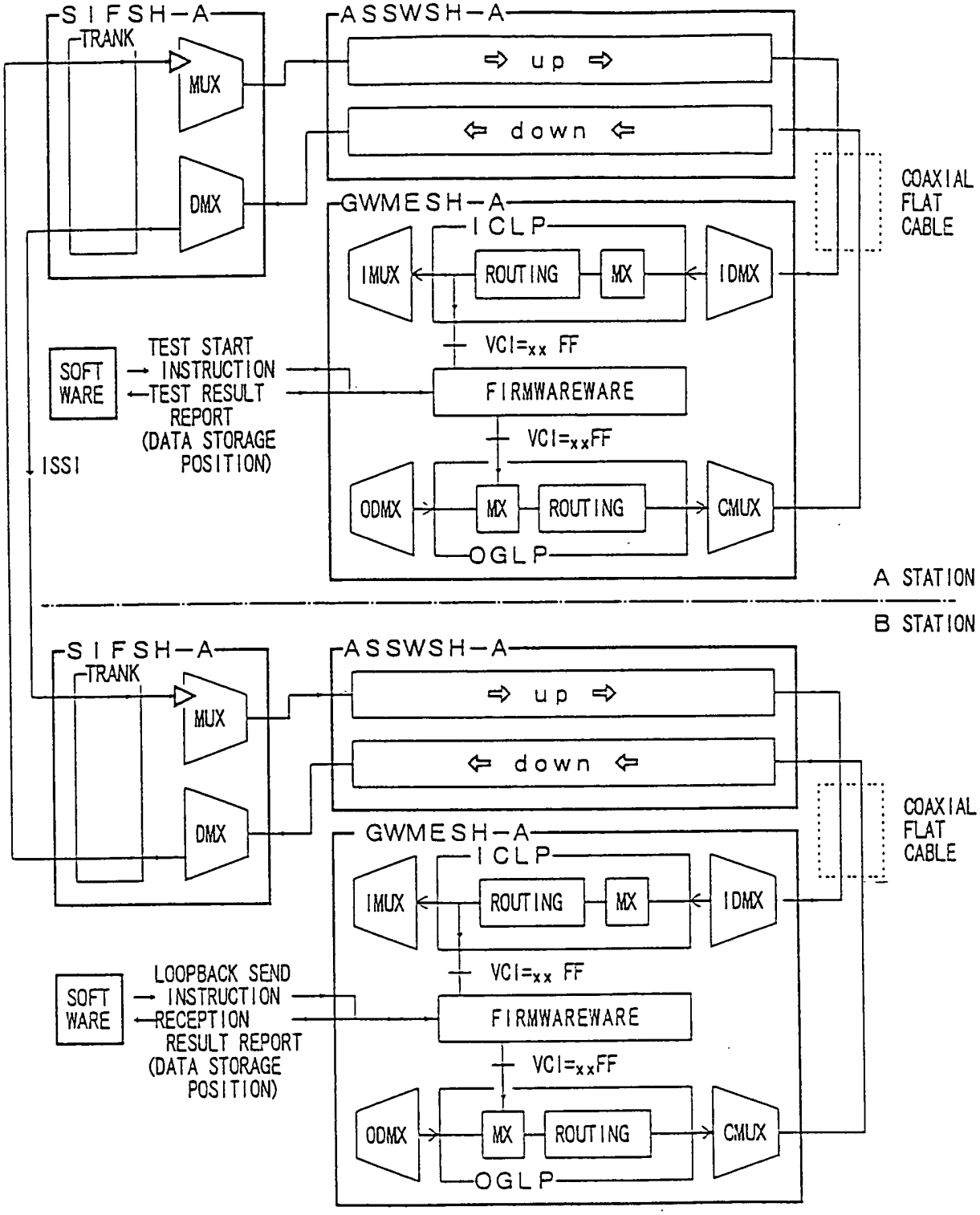

SIFSH-A
TRANK
MUX
DMX
ASSWSH-A
⇨ up ⇨
⇦ down ⇦
COAXIAL FLAT CABLE
GWMESH-A
ICLP
IMUX
ROUTING
MX
IDMX
VCI=xx FF
SOFT WARE
TEST START
→ INSTRUCTION
←TEST RESULT REPORT
(DATA STORAGE POSITION)
FIRMWAREWARE
VCI=xxFF
ISSI
ODMX
MX
ROUTING
CMUX
OGLP
A STATION
B STATION
SIFSH-A
TRANK
MUX
DMX
ASSWSH-A
⇨ up ⇨
⇦ down ⇦
COAXIAL FLAT CABLE
GWMESH-A
ICLP
IMUX
ROUTING
MX
IDMX
VCI=xx FF
SOFT WARE
LOOPBACK SEND
→ INSTRUCTION
←RECEPTION RESULT REPORT
(DATA STORAGE POSITION)
FIRMWAREWARE
VCI=xxFF
ODMX
MX
ROUTING
CMUX
OGLP

FIG. 697

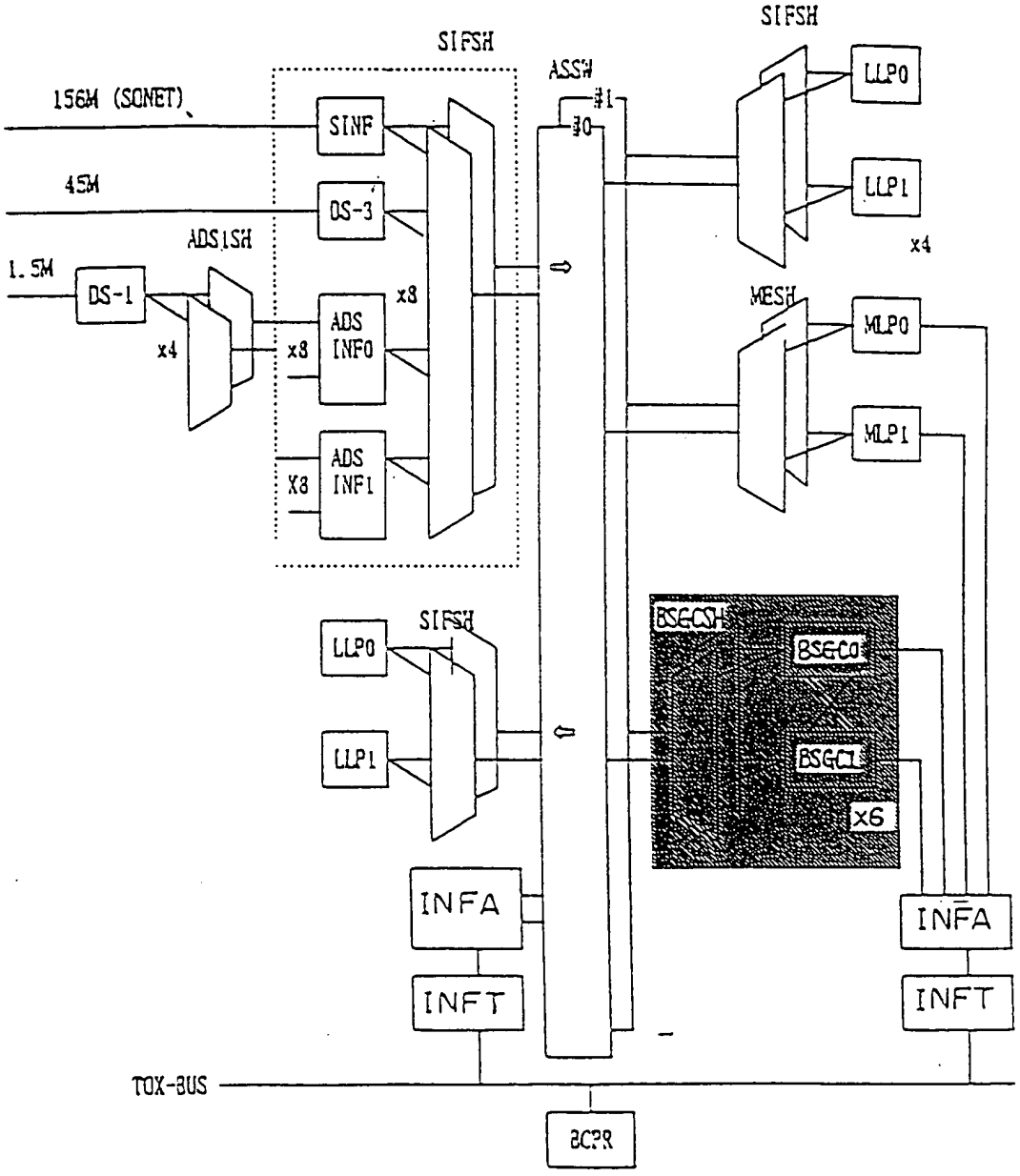

SIFSH
SIFSH
ASSW
#1
#0
156M (SONET)
SINF
45M
DS-3
ADSISH
1.5M
DS-1
x4
x8
ADS INF0
x8
ADS INF1
X8
LLP0
LLP1
x4
MESH
MLP0
MLP1
SIFSH
LLP0
LLP1
BSGCSH
BSGC0
BSGC1
x6
INFA
INFT
INFA
INFT
TOX-BUS
BCPR

FIG. 698

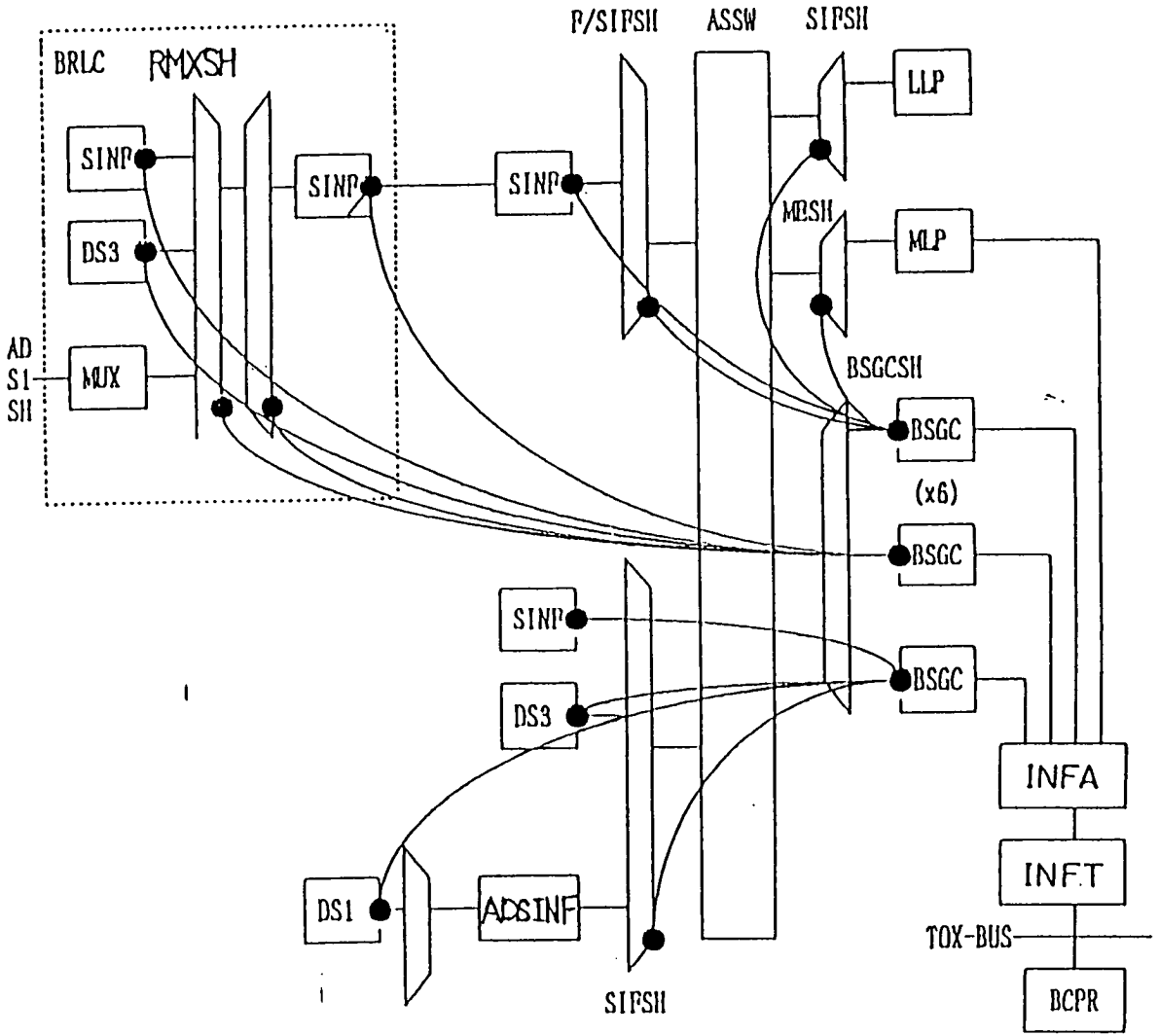

BRLC
RMXSH
SINP
SINP
SINP
DS3
MUX
AD
S1
SH
P/SIPSH
ASSW
SIPSH
LLP
MBSH
MLP
BSGCSH
BSGC
(x6)
BSGC
SINP
BSGC
DS3
INFA
INFT
TOX-BUS
BCPR
DS1
ADSINF
SIPSH

FIG. 699

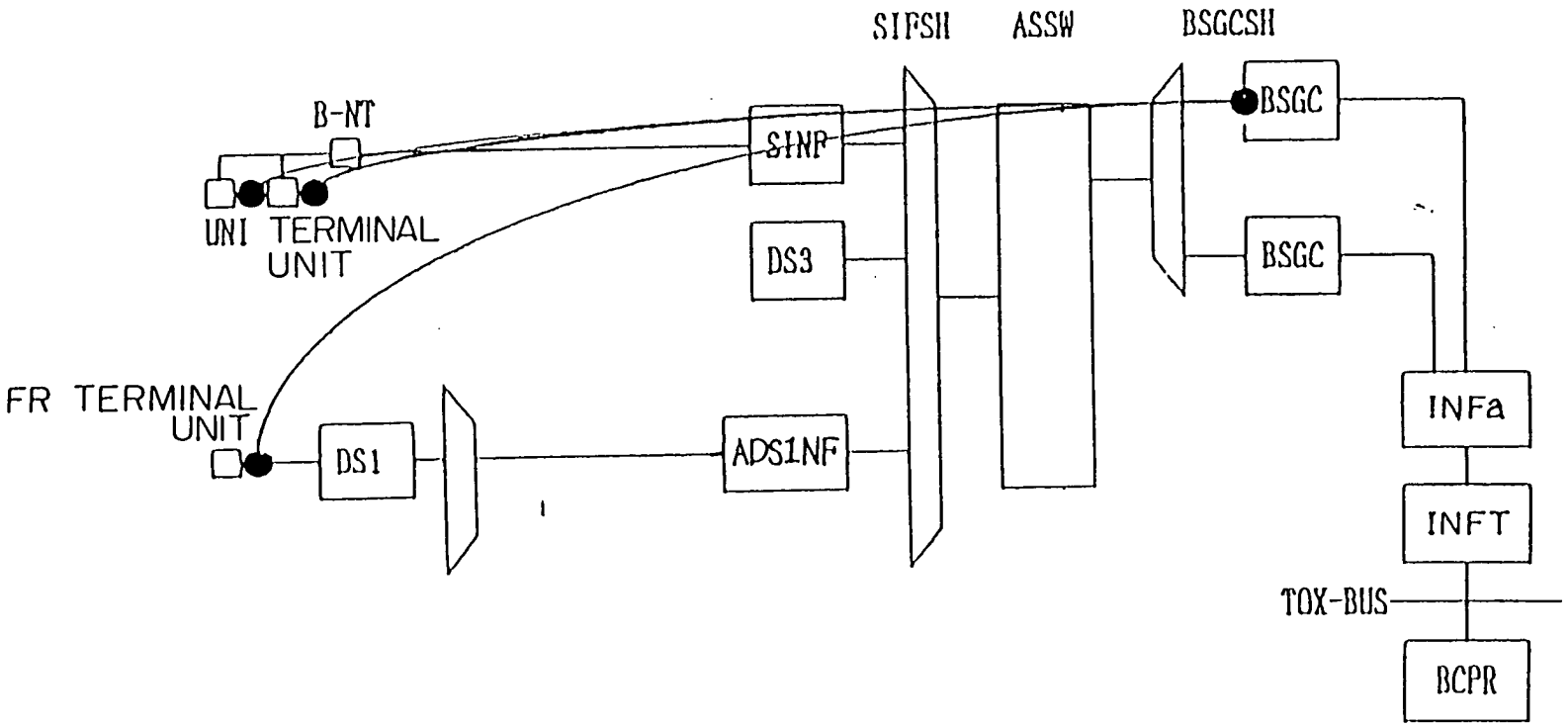
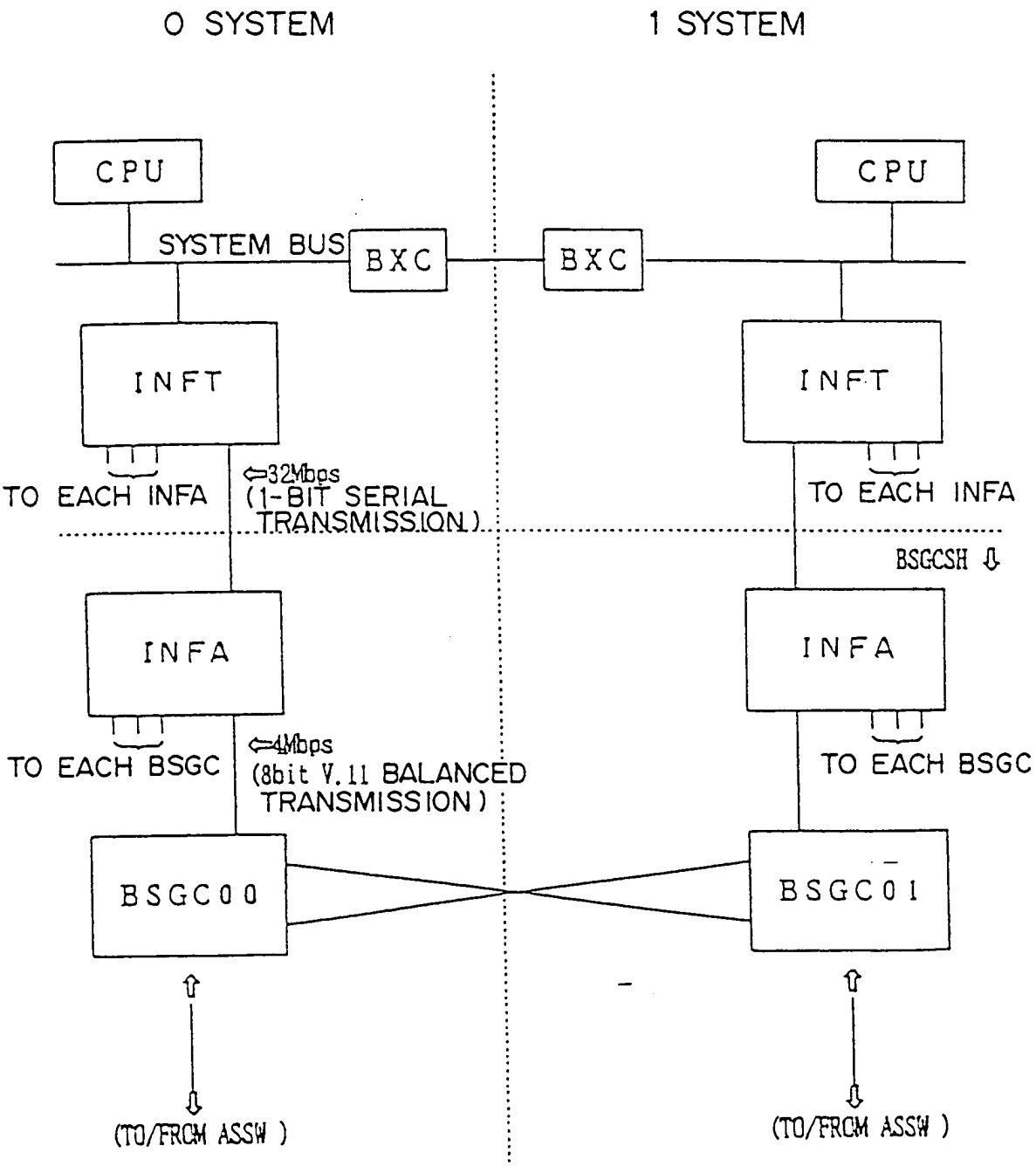

SIFSH
ASSW
BSGCSH
B-NT
SINP
BSGC
UNI TERMINAL UNIT
DS3
BSGC
FR TERMINAL UNIT
DS1
ADS1NF
INFa
INFT
TOX-BUS
BCPR

FIG. 700

NO	ITEM		SPECIFICATION	REMARKS
1	BSGC CARD	PROCESSOR	MBL80186(16 BIT MICRO PROCESSOR)	
2		REDUNDANCY	DUPLICATION	
3		MEMORY CAPACITY	ROM 256 K BYTE (BANK SWITCH) S-RAM 32 K BYTE D-RAM 896 K BYTE	
4		MAXIMUM NUMBER OF SIMULTANEOUS LINK CONNECTIONS	256 CHANNEL (TO BE EXTENDE INTO 1024 CHANNEL*)	
5		SBIF LSI	INF FOR CONTROLLING MB651623	
6		CARP1/2 LSI	CLAD FOR CONTROLLING MBCG31134, MB630615	
7		MUX	CELL MULTIPLEX LSI MBCG31204-639	
8		ACT CONTROL	DEPENDING ON ACT OF INF	
9		NUMBER OF PCB	1 PCB	
10	COM	VCC	TAG CONVERSION MEMORY MBCG21503	
11		SELN1	O&M FOR CONTROLLING MBCG21XXX	
12		MUX	CELL MULTIPLEX LSI MBCG31204-639	
13		DMUX	CELL DEMULTIPLEX LSI MBCG31204-638	
14		ACT CONTROL	DEPENDING ON ACT OF SWITCH	
15		NUMBER OF PCB	5 PCB	
16	SHELF	SHELF CONFIGURATION	LOADED WITH ONE SYSTEM 6 BSGC AND 1 COM	
17		DUPLEX CROSS CONNECTION	CROSS CONNECTION OF BSGC AND COM	
18		FUNCTIONS	①TERMINATING INTRA-STATION DEVICE LINK ②META-SIGNAL COMMUNICATIONS PORT CONTROL ③SUBSCRIBER TERMINAL UNIT SIGNALING PORT CONTROL ④SVC PORT CONTROL OF DS1FR ⑤SETTING VCC (ONLY STARTING NUMBER BSGC)	

FIG. 701



※ FOUR BSGCs ARE CONNECTABLE FOR AN INFA.
BSGCSH ACCOMMODATES 6BSGCs

FIG. 702

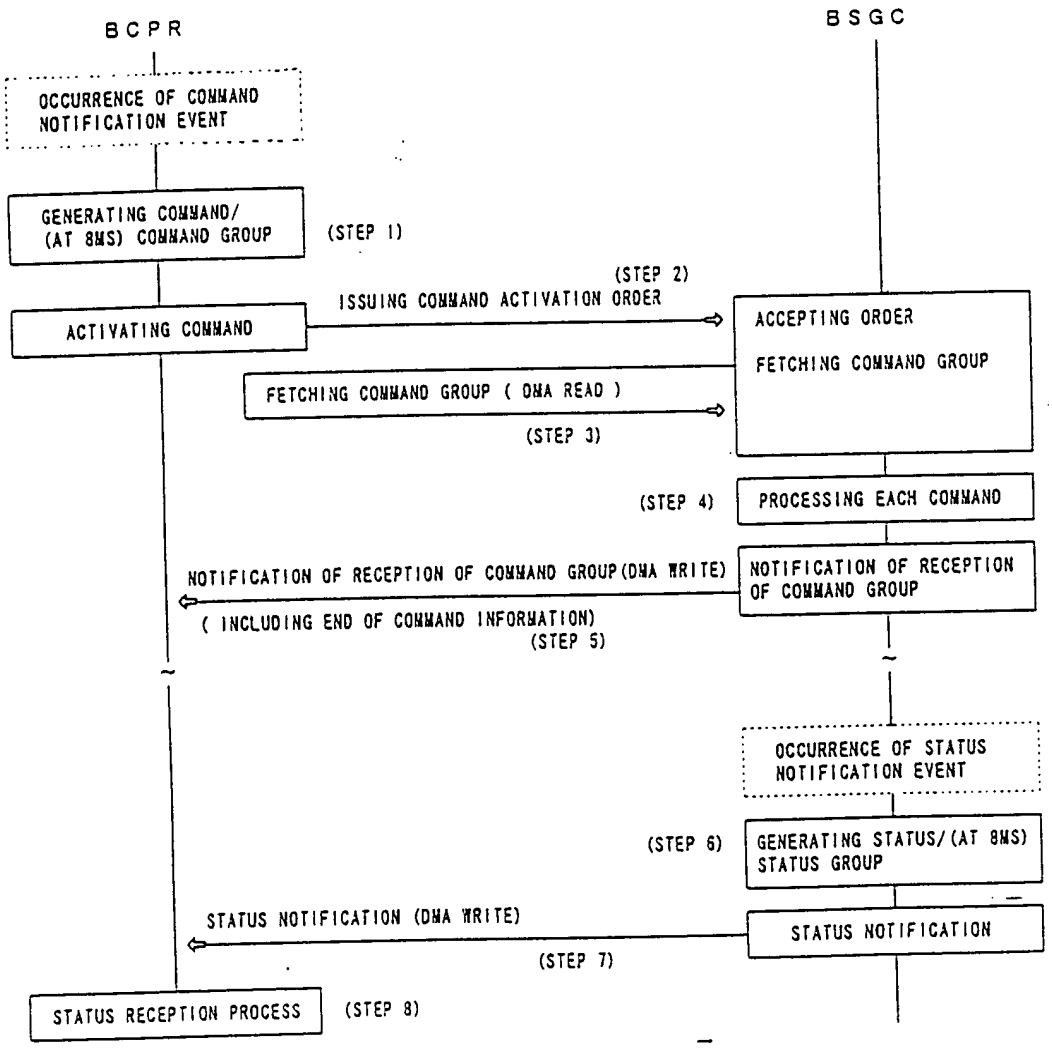
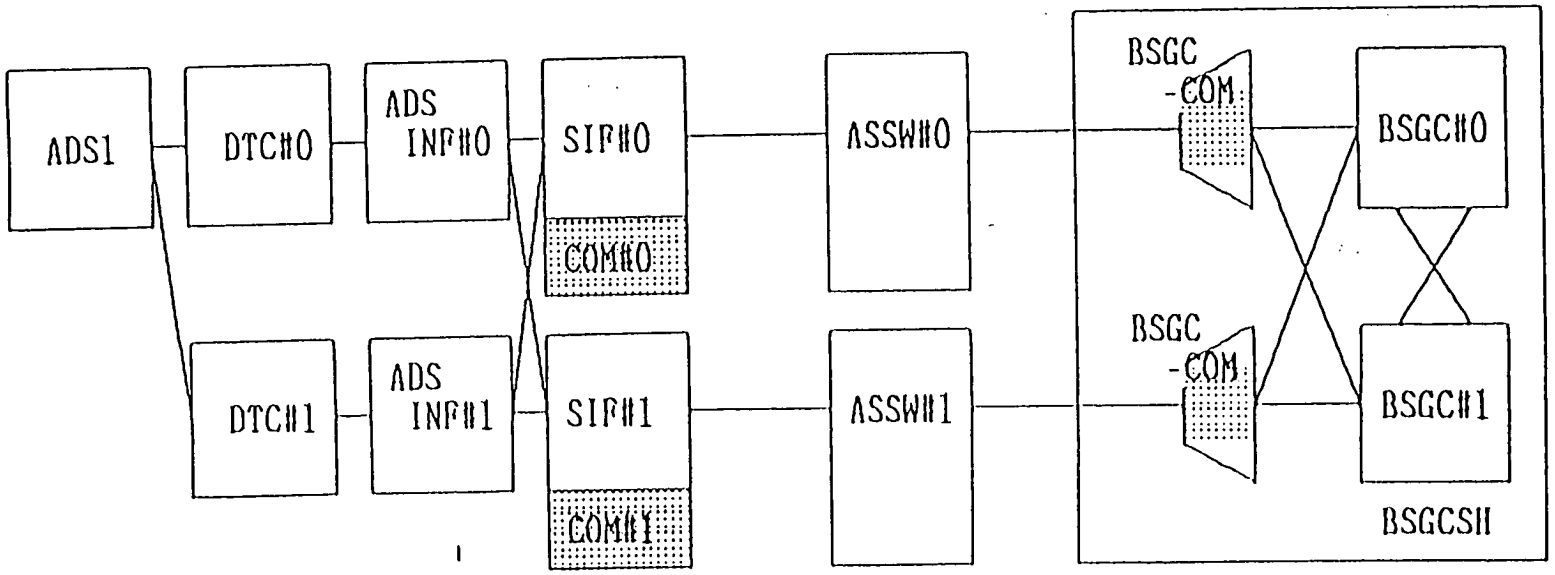

BCPR
BSGC
OCCURRENCE OF COMMAND NOTIFICATION EVENT
GENERATING COMMAND/ (AT 8MS) COMMAND GROUP
(STEP 1)
(STEP 2)
ISSUING COMMAND ACTIVATION ORDER
ACTIVATING COMMAND
ACCEPTING ORDER
FETCHING COMMAND GROUP
FETCHING COMMAND GROUP (DMA READ)
(STEP 3)
(STEP 4)
PROCESSING EACH COMMAND
NOTIFICATION OF RECEPTION OF COMMAND GROUP(DMA WRITE)
(INCLUDING END OF COMMAND INFORMATION)
(STEP 5)
NOTIFICATION OF RECEPTION OF COMMAND GROUP
OCCURRENCE OF STATUS NOTIFICATION EVENT
(STEP 6)
GENERATING STATUS/(AT 8MS) STATUS GROUP
STATUS NOTIFICATION (DMA WRITE)
(STEP 7)
STATUS NOTIFICATION
STATUS RECEPTION PROCESS
(STEP 8)

FIG. 703



note) 1. ▒: LOADED BY VCC
2. ACT OF BSGCCOM IS DEPENDENT ON SWITCH
3. ACT OF BSGC IS DEPENDENT ON INDIVIDUAL SYSTEM SPECIFICATION OF INF.

FIG. 704

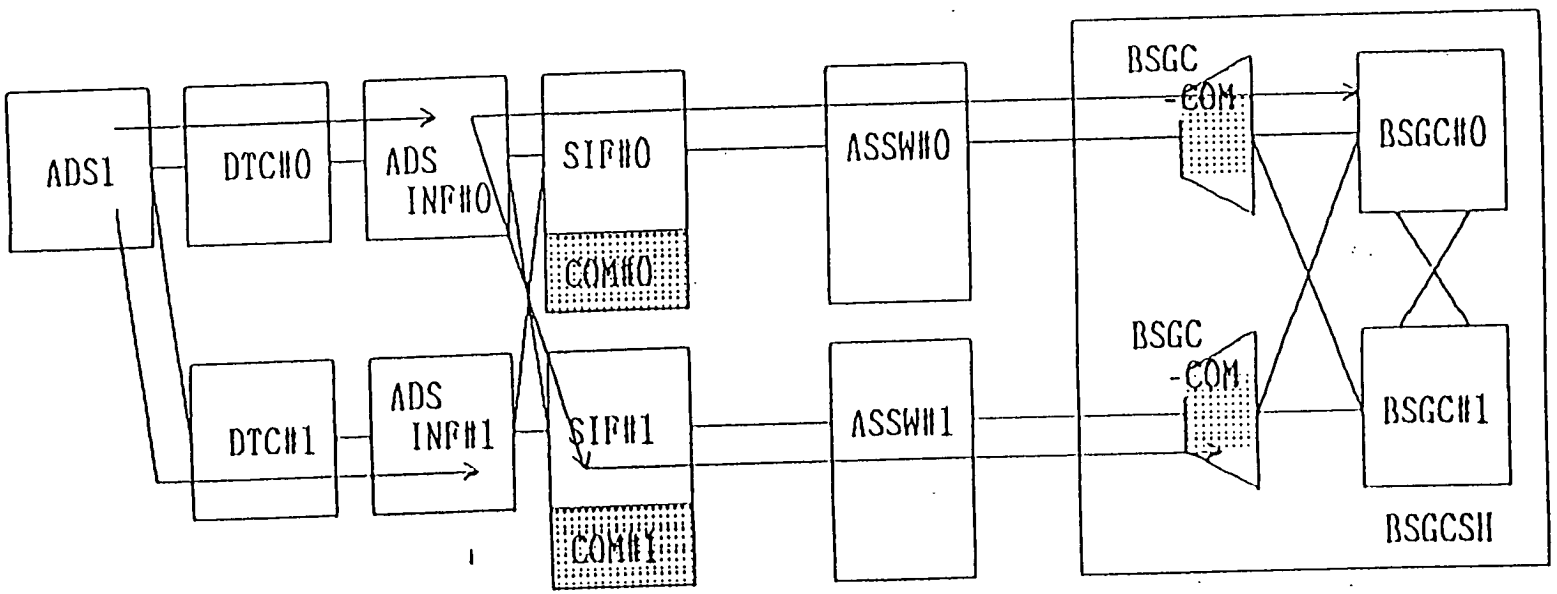

ADS1
DTCH0
ADS INFH0
SIFH0
COMH0
ASSWH0
BSGC -COM
BSGCH0
DTCH1
ADS INFH1
SIFH1
COMH1
ASSWH1
BSGC -COM
BSGCH1
BSGCSH

FIG. 705

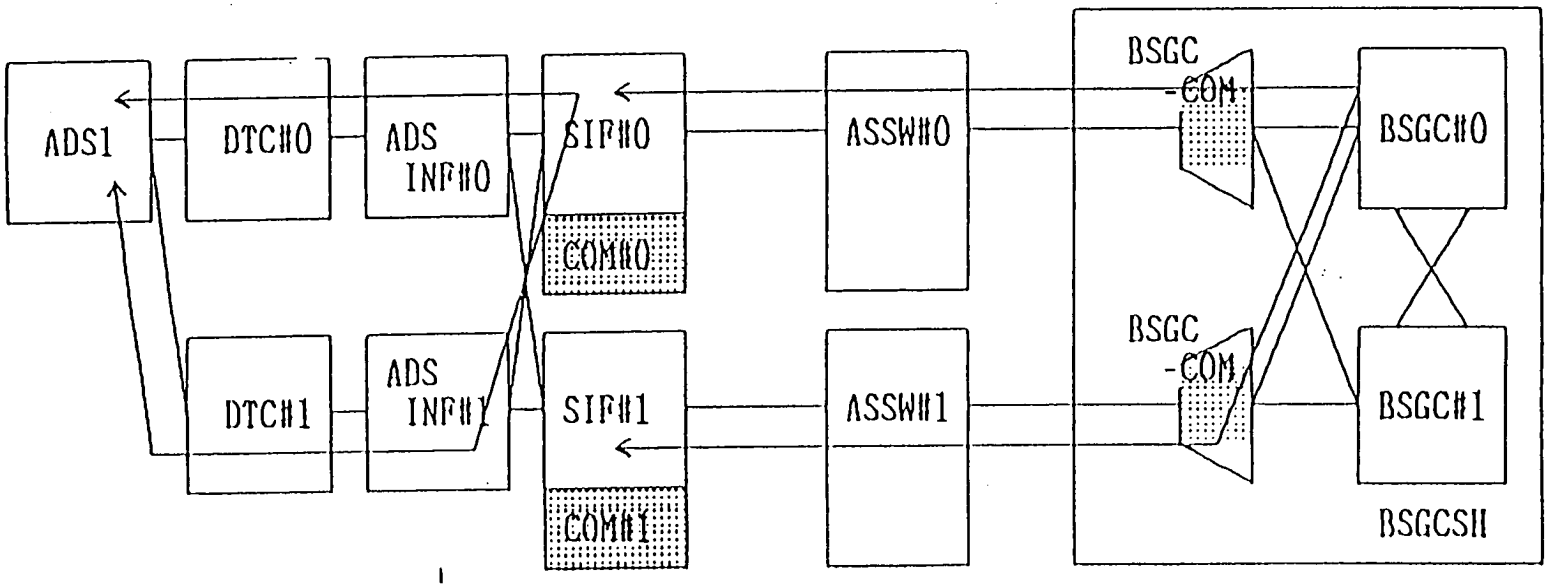

ADS1
DTCH0
ADS INFH0
SIFH0
COMH0
ASSWH0
BSGC -COM
BSGCH0
DTCH1
ADS INFH1
SIFH1
COMH1
ASSWH1
BSGC -COM
BSGCH1
BSGCSH

FIG. 706

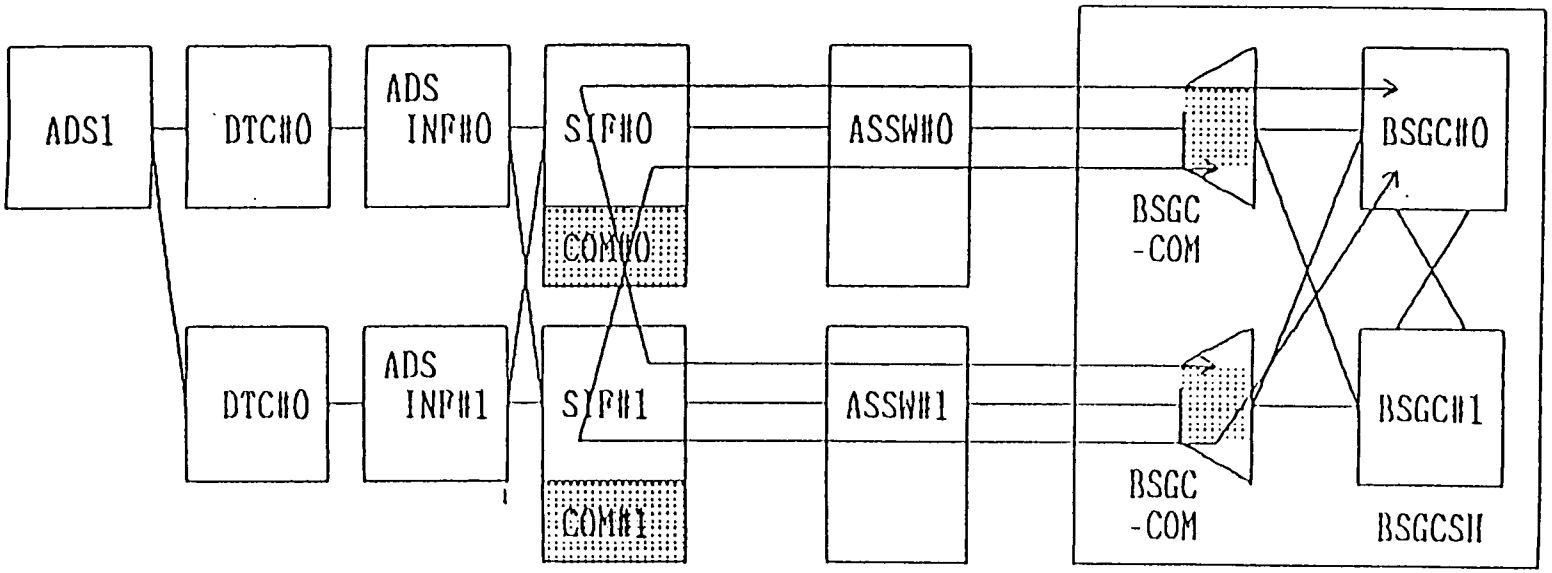

ADS1
DTCH0
ADS
INFH0
SIFH0
COMH0
ASSWH0
BSGC
-COM
BSGCH0
DTCH0
ADS
INFH1
SIFH1
COMH1
ASSWH1
BSGC
-COM
BSGCH1
BSGCSH

FIG. 707

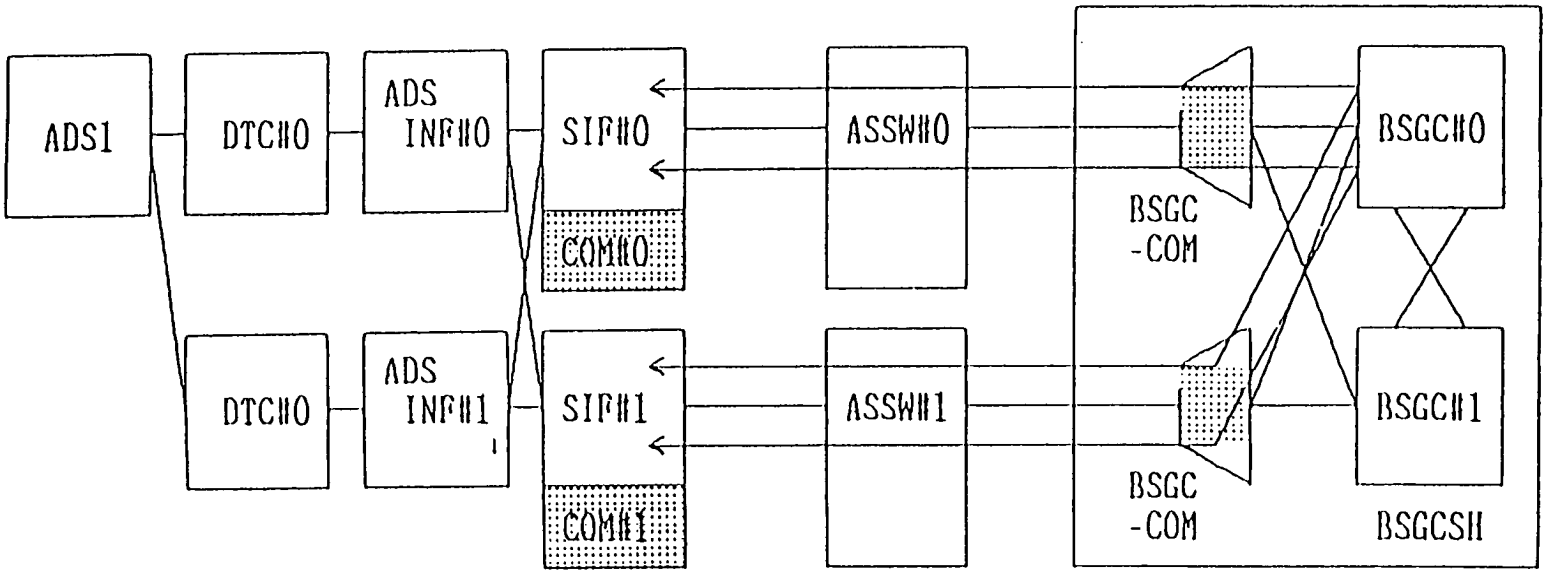

ADS1
DTCH0
ADS INFH0
SIFH0
COMH0
ASSWH0
BSGC -COM
BSGCH0
DTCH0
ADS INFH1
SIFH1
COMH1
ASSWH1
BSGC -COM
BSGCH1
BSGCSH

FIG. 708

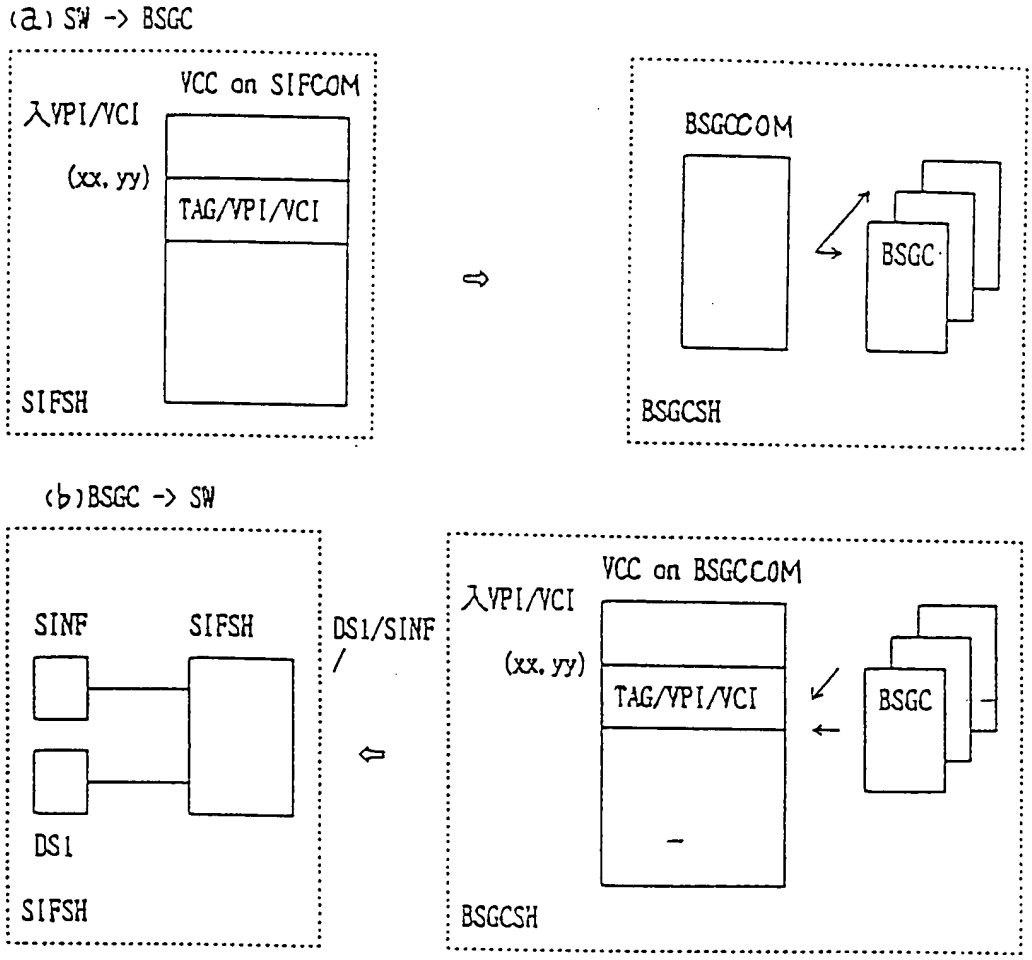

(a) SW -> BSGC
VCC on SIFCOM
入VPI/VCI
(xx, yy)
TAG/VPI/VCI
SIFSH
BSGCCOM
BSGC
BSGCSH
(b) BSGC -> SW
SINF
SIFSH
DS1
SIFSH
DS1/SINF
/
VCC on BSGCCOM
入VPI/VCI
(xx, yy)
TAG/VPI/VCI
BSGC
BSGCSH

FIG. 709

(a) IN HOST/BRLC

VPI(H)	VCI(H)	USE
FROM 00 TO 3F	FROM 0000 TO 001F	REQUIREMENT RESERVE E.G. FOR SIGNALING FOR OAM CELL
	FROM 0020 TO 03EF	USER CELL E.G. FOR ATM-UNI, CE, FR
	FROM 03F0 TO 03FE	SYSTEM RESERVE FOR INTRA-STATION LAP SIF-COM #0 : VPI=00, VCI=03FC SIF-COM #1 : VPI=00, VCI=03FD RMX-COM #0 : VPI=3F, VCI=03F0 RMX-COM #1 : VPI=3F, VCI=03F1 DS3, SINF : VPI=00, VCI=03FE DS1 : VPI=AA, VCI=03FE AA: 5 LOWER ORDER BITS ARE FOR DS1 UNIT NUMBER FOR TEST : VPI=00, VCI=03FA, 03FB
	03FF	USER CELL (EXCLUSIVELY FOR SMDS)

(b) IN UNBILICAL LINK

VPI(H)	VCI(H)	USE
FROM 00 TO XX	FROM 0000 TO 001F	REQUIREMENT RESERVE E.G. FOR SIGNALING FOR OAM CELL
	FROM 0020 TO 03EF	USER CELL E.G. FOR ATM-UNI, CE, FR
3F	FROM 0020 TO 03EF	FOR INTRA LAP OF SIMPLEX DEVICE IN BRLC
	FROM 03F0 TO 03F7	FOR INTRA LAP OF DUPLEX DEVICE IN BRLC

FIG. 710

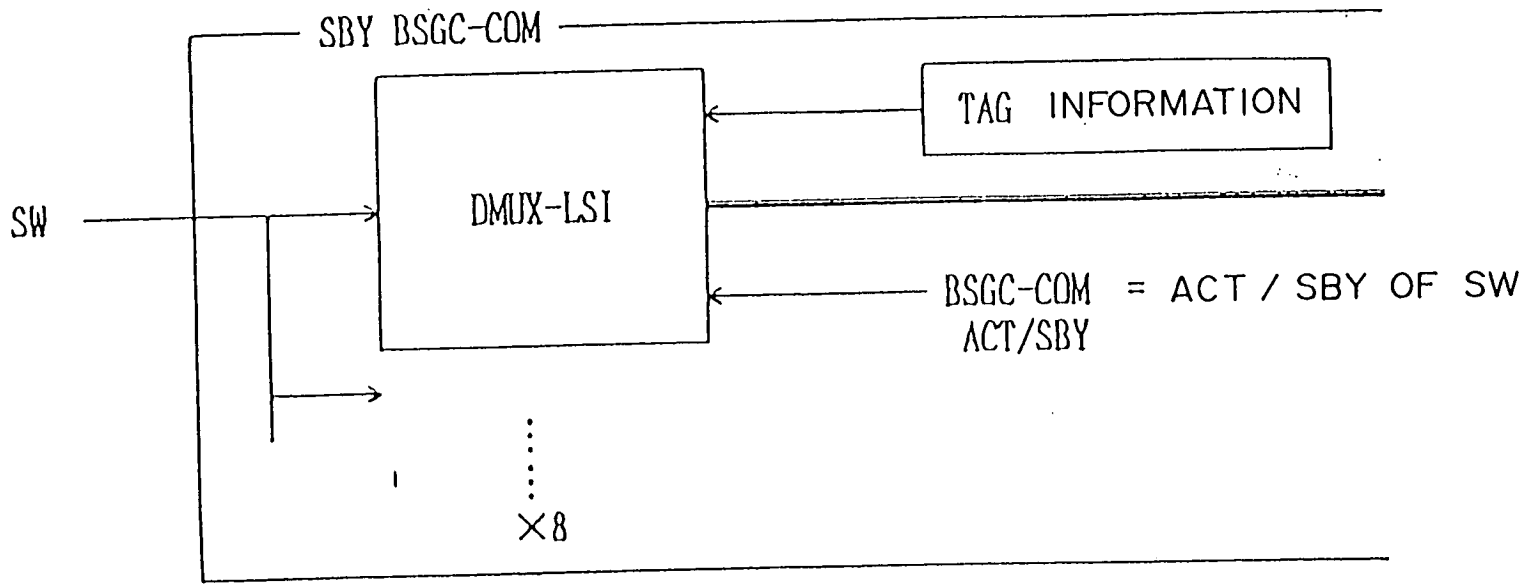

SBY BSGC-COM
TAG INFORMATION
SW
DMUX-LSI
BSGC-COM = ACT / SBY OF SW
ACT/SBY
×8

FIG. 711

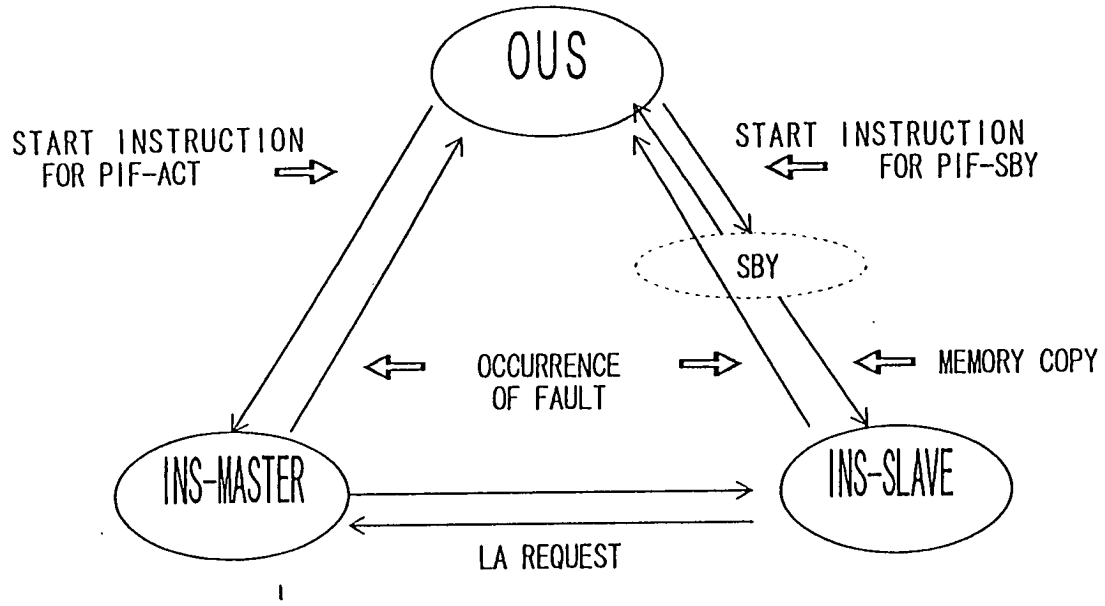
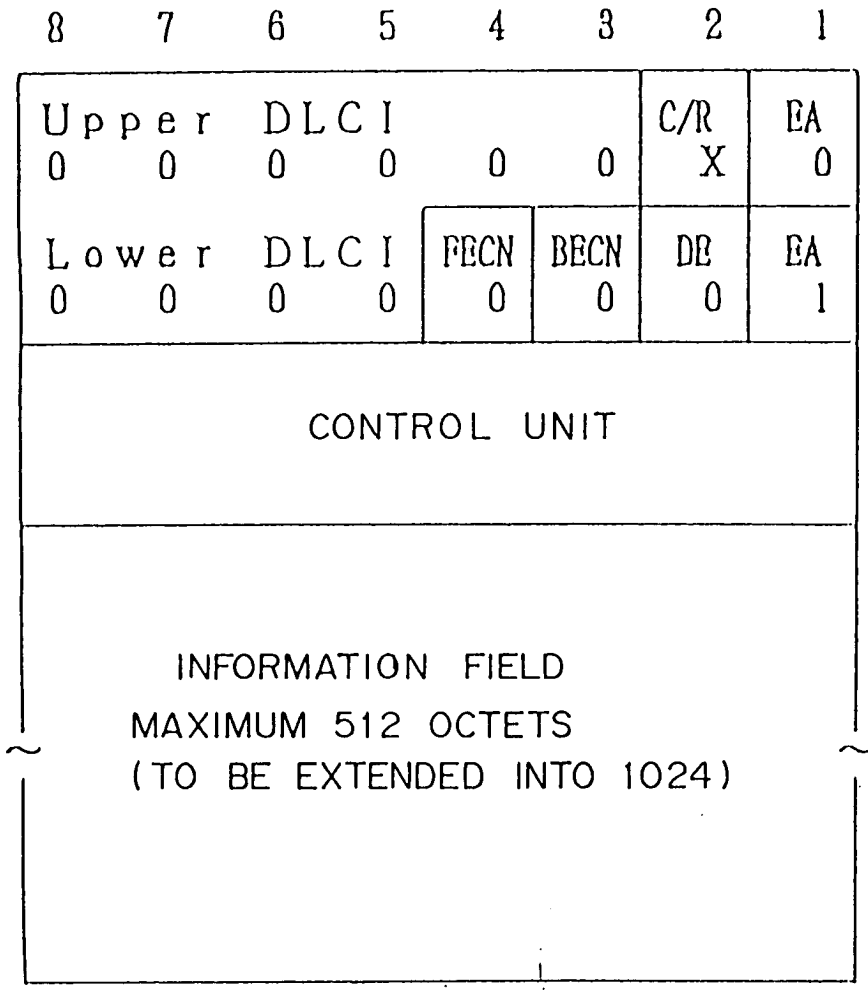
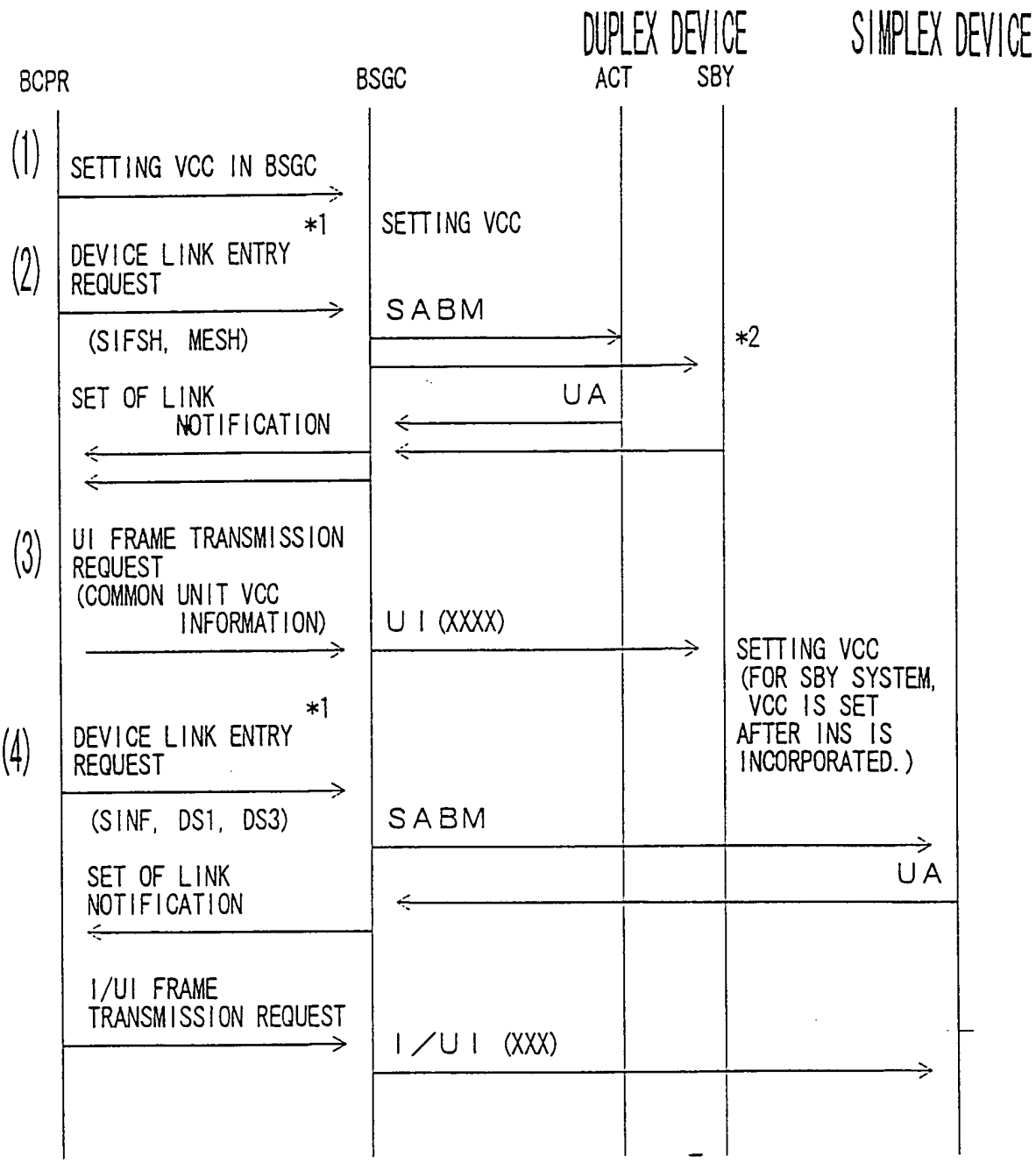

OUS
START INSTRUCTION FOR PIF-ACT
START INSTRUCTION FOR PIF-SBY
SBY
OCCURRENCE OF FAULT
MEMORY COPY
INS-MASTER
INS-SLAVE
LA REQUEST

FIG. 712



EA :Address Field Extension bit
C/R :Command Response bit
FECN:Forward Explicit Congestion Notification
BECN:Backward Explicit Congestion Notification
DE :Discard Eligibility bit

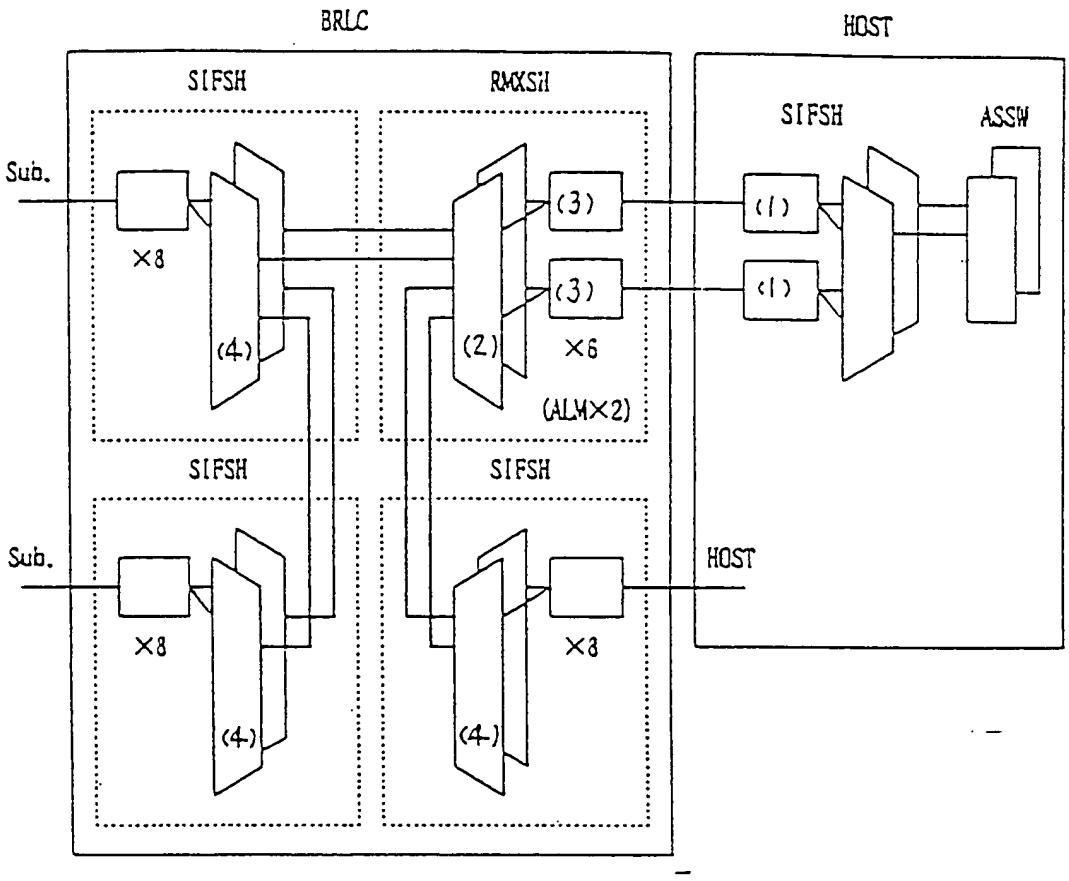
FIG. 713



*1 : ENTIRE LINKS ARE ESTABLISHED BASED ON BCPR DATA.

*2 : RETURNING TAG INFORMATION IS ASSIGNED TO SABM TO COMMON UNIT.

FIG. 714



(1) – (4) : INDICATES LAP LINK SETTING NUMBER
(1) AND (3) : SIMPLEX COMMUNICATIONS PORT
(2) AND (4) : 2 LINKS OF ACT/SBY ARE ESTABLISHED FOR DUPLEX COMMUNICATIONS PORT.
LINK ESTABLISHING PROCEDURE IS SAME AS THAT FOR SIFCOM COMMON UNIT

FIG. 715

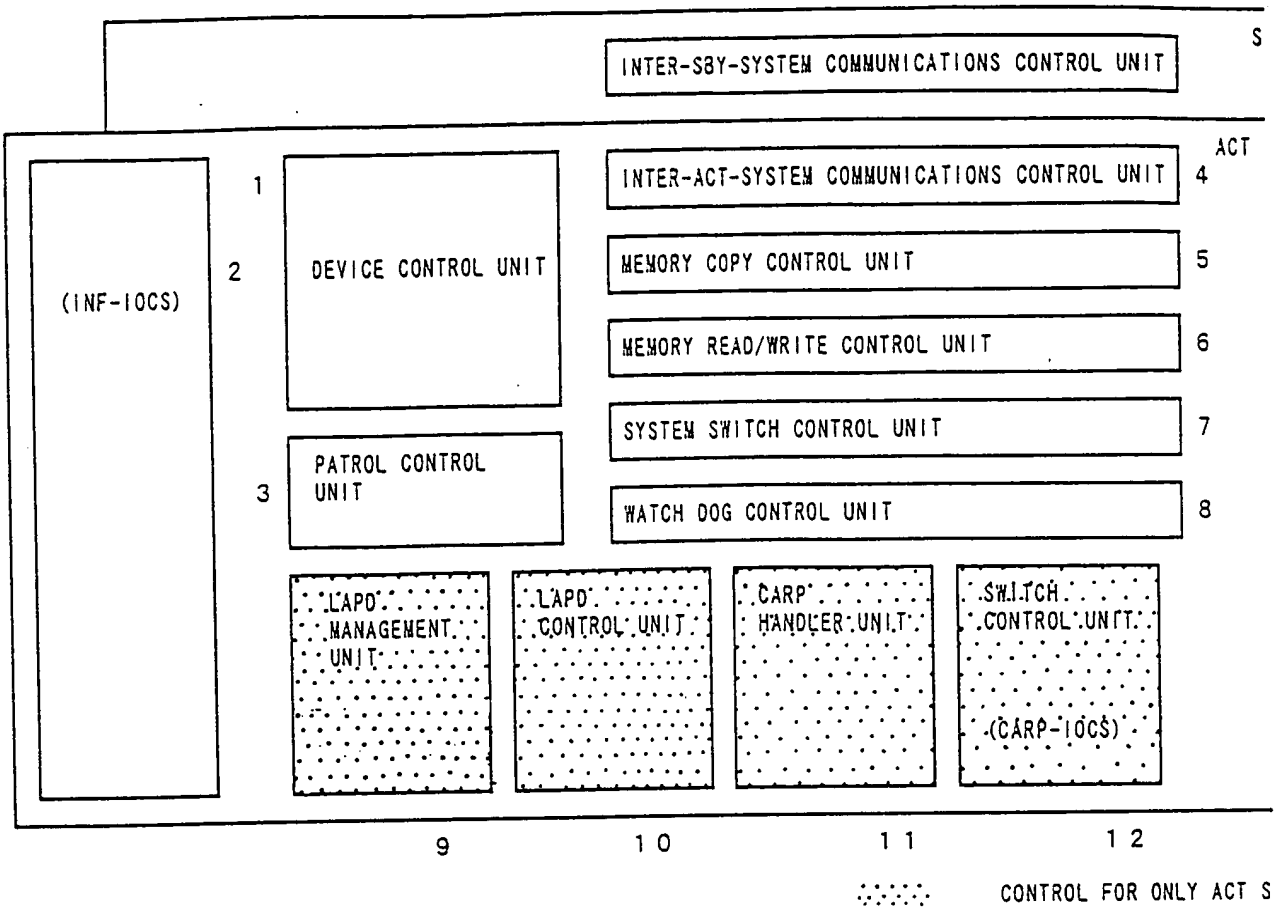
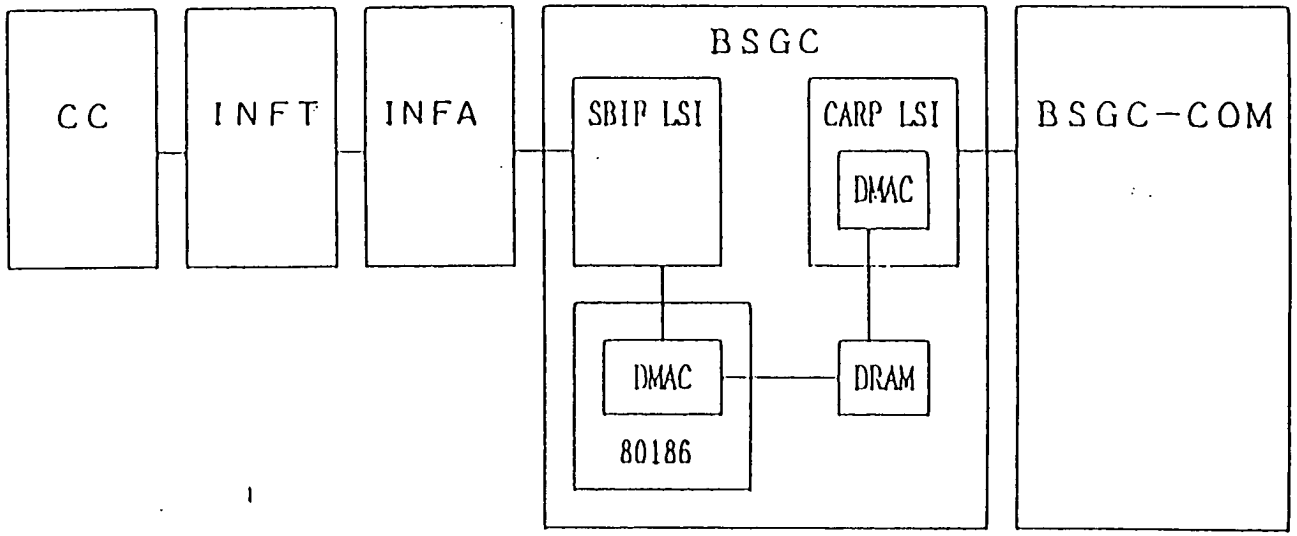

S
INTER-SBY-SYSTEM COMMUNICATIONS CONTROL UNIT
ACT
(INF-IOCS)
1
2
DEVICE CONTROL UNIT
3
PATROL CONTROL UNIT
INTER-ACT-SYSTEM COMMUNICATIONS CONTROL UNIT
4
MEMORY COPY CONTROL UNIT
5
MEMORY READ/WRITE CONTROL UNIT
6
SYSTEM SWITCH CONTROL UNIT
7
WATCH DOG CONTROL UNIT
8
LAPD MANAGEMENT UNIT
LAPD CONTROL UNIT
CARP HANDLER UNIT
SWITCH CONTROL UNIT
(CARP-IOCS)
9
10
11
12
CONTROL FOR ONLY ACT S

FIG. 716



NOTE 1 : DMA OF INF IS REALIZED BY DMA FUNCTIONS OF 80186 AND SBIF.
NOTE 2 : DMA OF CARP IS REALIZED BY DMA FUNCTIONS IN CARP 2
NOTE 3 : SBIF AND CARP ARE CONTROLLED BY 80186 EXTERNAL INTERRUPTION (INT 3).

FIG. 717

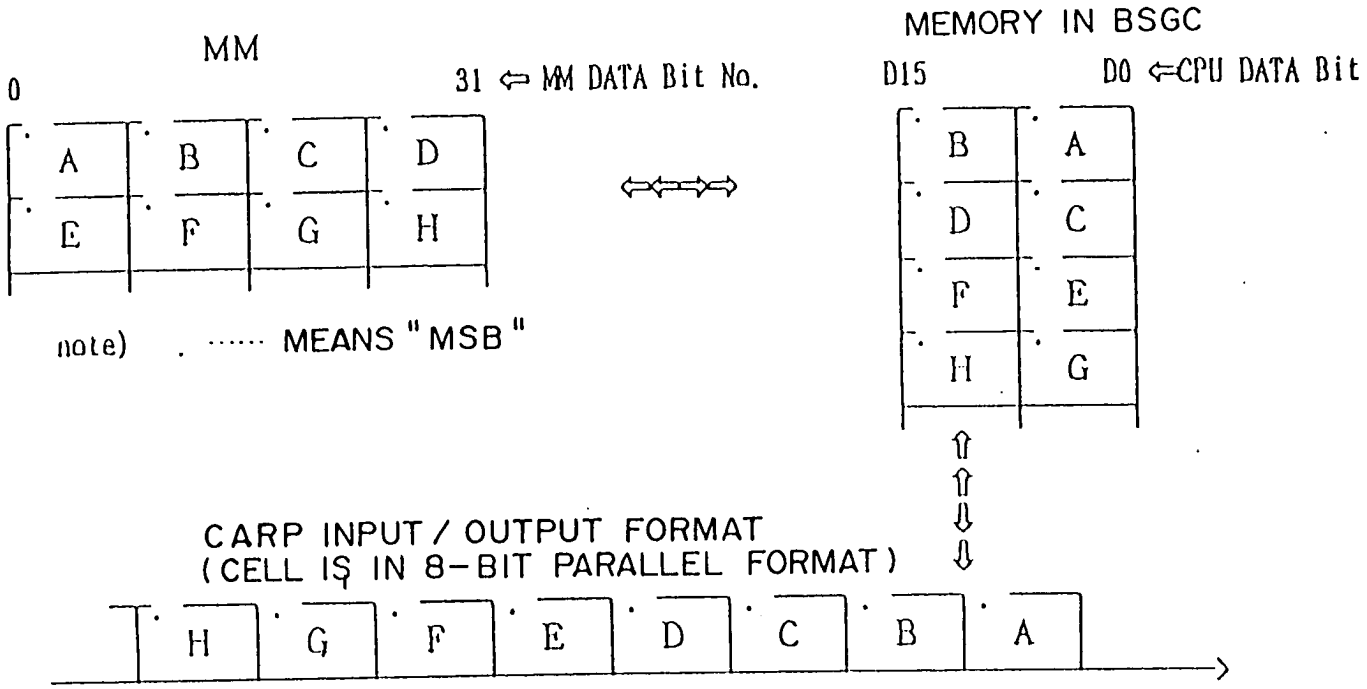

MM
0
31 ⇦ MM DATA Bit No.
A
B
C
D
E
F
G
H
note) . ····· MEANS "MSB"
MEMORY IN BSGC
D15
D0 ⇦CPU DATA Bit
B
A
D
C
F
E
H
G
CARP INPUT / OUTPUT FORMAT
(CELL IS IN 8-BIT PARALLEL FORMAT)
H
G
F
E
D
C
B
A

FIG. 718

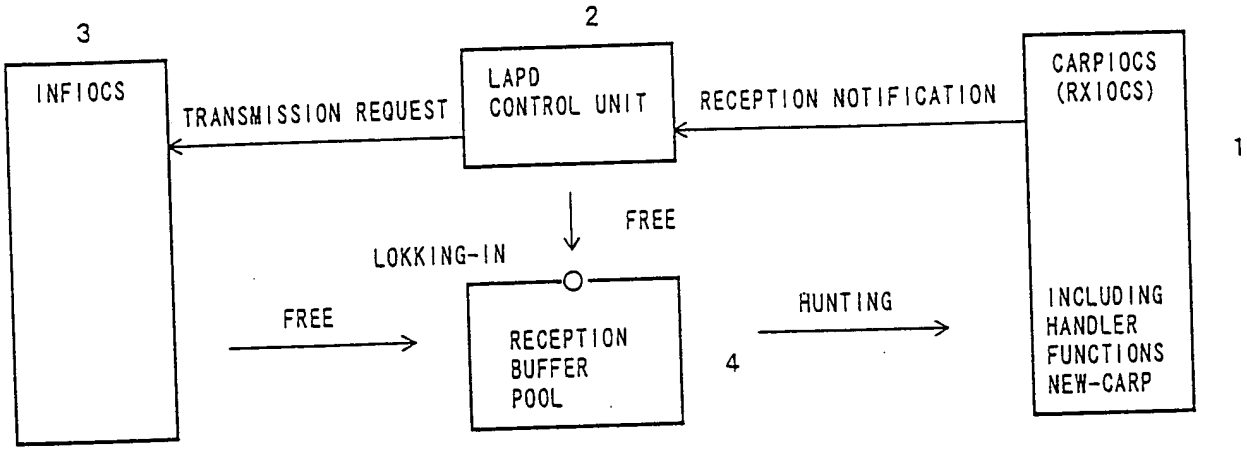

3
INFIOCS
TRANSMISSION REQUEST
2
LAPD
CONTROL UNIT
RECEPTION NOTIFICATION
CARPIOCS
(RXIOCS)
1
FREE
LOKKING-IN
FREE
RECEPTION
BUFFER
POOL
4
HUNTING
INCLUDING
HANDLER
FUNCTIONS
NEW-CARP

FIG. 719

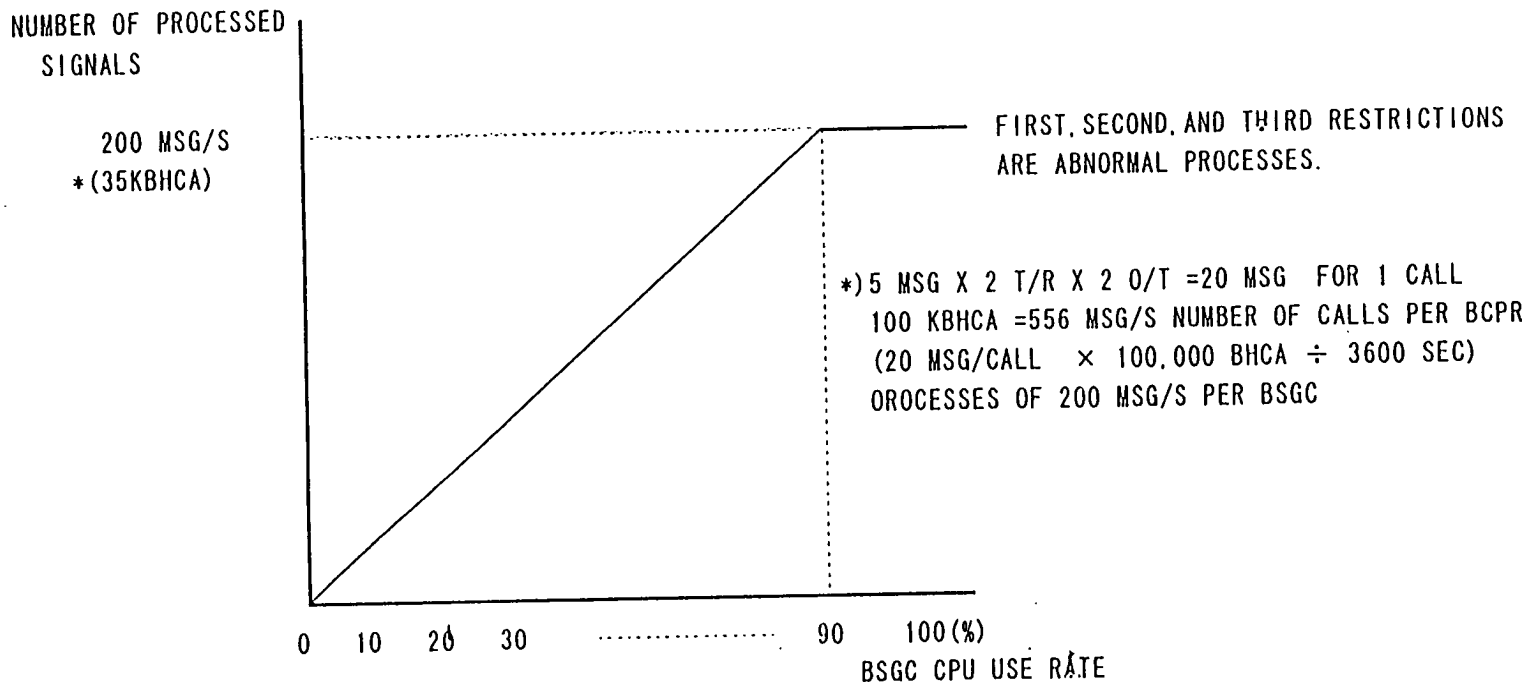

NUMBER OF PROCESSED SIGNALS
200 MSG/S
*(35KBHCA)
FIRST, SECOND, AND THIRD RESTRICTIONS ARE ABNORMAL PROCESSES.
*)5 MSG X 2 T/R X 2 O/T =20 MSG FOR 1 CALL
100 KBHCA =556 MSG/S NUMBER OF CALLS PER BCPR
(20 MSG/CALL × 100,000 BHCA ÷ 3600 SEC)
OROCESSES OF 200 MSG/S PER BSGC
0 10 20 30 90 100(%)
BSGC CPU USE RATE

FIG. 720

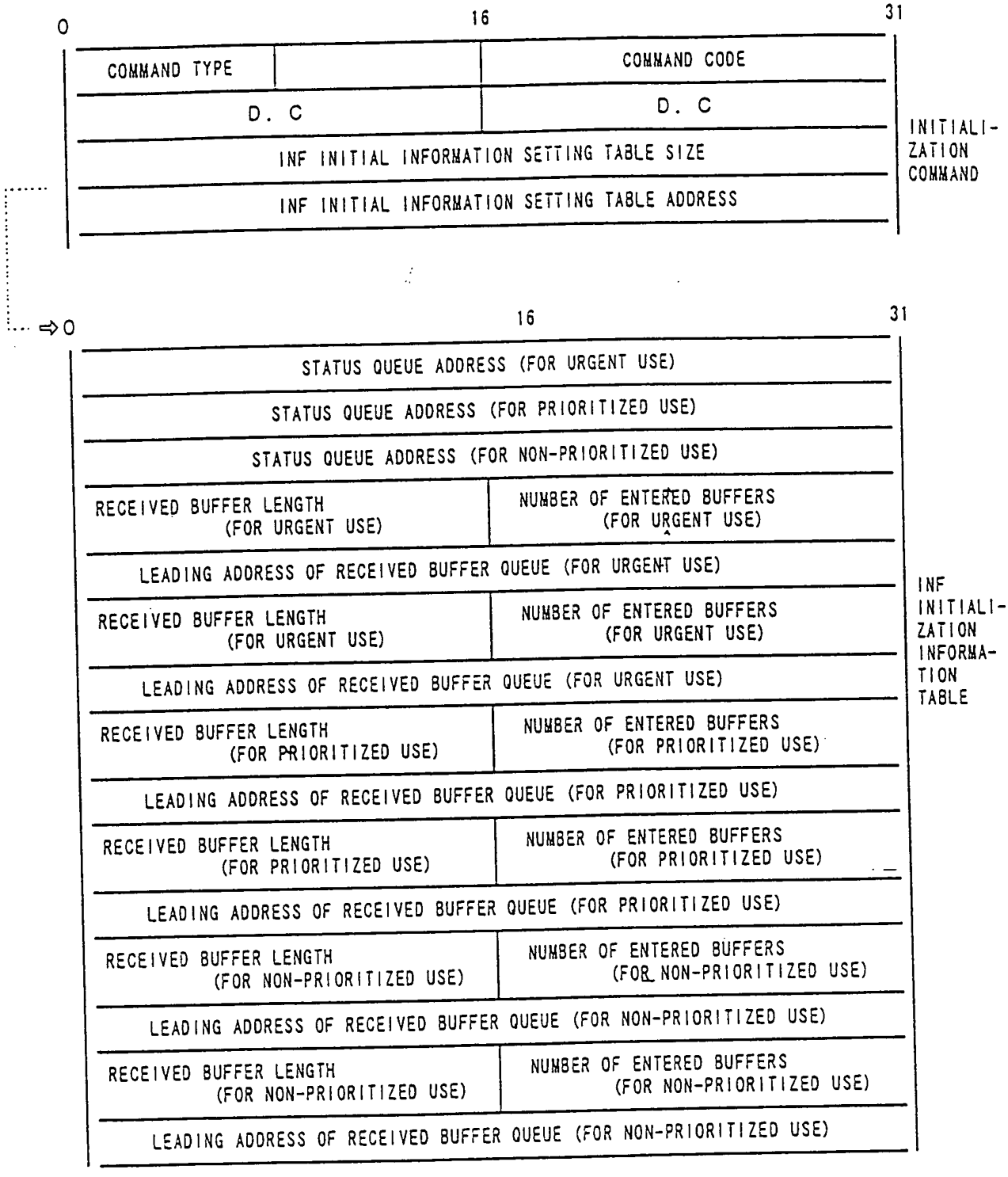

0
16
31
COMMAND TYPE
COMMAND CODE
D. C
D. C
INF INITIAL INFORMATION SETTING TABLE SIZE
INF INITIAL INFORMATION SETTING TABLE ADDRESS
INITIALI-ZATION COMMAND
STATUS QUEUE ADDRESS (FOR URGENT USE)
STATUS QUEUE ADDRESS (FOR PRIORITIZED USE)
STATUS QUEUE ADDRESS (FOR NON-PRIORITIZED USE)
RECEIVED BUFFER LENGTH (FOR URGENT USE)
NUMBER OF ENTERED BUFFERS (FOR URGENT USE)
LEADING ADDRESS OF RECEIVED BUFFER QUEUE (FOR URGENT USE)
RECEIVED BUFFER LENGTH (FOR URGENT USE)
NUMBER OF ENTERED BUFFERS (FOR URGENT USE)
LEADING ADDRESS OF RECEIVED BUFFER QUEUE (FOR URGENT USE)
RECEIVED BUFFER LENGTH (FOR PRIORITIZED USE)
NUMBER OF ENTERED BUFFERS (FOR PRIORITIZED USE)
LEADING ADDRESS OF RECEIVED BUFFER QUEUE (FOR PRIORITIZED USE)
RECEIVED BUFFER LENGTH (FOR PRIORITIZED USE)
NUMBER OF ENTERED BUFFERS (FOR PRIORITIZED USE)
LEADING ADDRESS OF RECEIVED BUFFER QUEUE (FOR PRIORITIZED USE)
RECEIVED BUFFER LENGTH (FOR NON-PRIORITIZED USE)
NUMBER OF ENTERED BUFFERS (FOR NON-PRIORITIZED USE)
LEADING ADDRESS OF RECEIVED BUFFER QUEUE (FOR NON-PRIORITIZED USE)
RECEIVED BUFFER LENGTH (FOR NON-PRIORITIZED USE)
NUMBER OF ENTERED BUFFERS (FOR NON-PRIORITIZED USE)
LEADING ADDRESS OF RECEIVED BUFFER QUEUE (FOR NON-PRIORITIZED USE)
INF INITIALI-ZATION INFORMA-TION TABLE

FIG. 721

SIG	UL	TAGC	COM	PATH
0/1	0	000	0	SIFSH#0 LINE0/SIGNALING
0/1	0	001	0	SIFSH#0 LINE1/SIGNALING
		⟆		⟆
0/1	0	111	0	SIFSH#0 LINE7/SIGNALING
0/1	1	000	0	SIFSH#1 LINE0/SIGNALING
0/1	1	001	0	SIFSH#1 LINE1/SIGNALING
		⟆		⟆
0/1	1	111	0	SIFSH#1 LINE7/SIGNALING
1	0	000	1	SIFSH#0 COM SIGNALING
1	1	000	1	SIFSH#1 COM SIGNALING

FIG. 722

SIG	UL	TAGB	TAGC	COM	PATH
0/1	0	0	000	0	RMUXSH#0 LINE0 / SIGNALING
0/1	0	0	001	0	RMUXSH#0 LINE1 / SIGNALING
			⟆		⟆
0/1	0	0	111	0	RMUXSH#0 LINE7 / SIGNALING
0/1	1	0	000	0	RMUXSH#1 LINE0 / SIGNALING
0/1	1	0	001	0	RMUXSH#1 LINE1 / SIGNALING
			⟆		⟆
0/1	1	0	111	0	RMUXSH#1 LINE7 / SIGNALING
0/1	1	1	000	0	RMUXSH#2 LINE0 / SIGNALING
0/1	1	1	001	0	RMUXSH#2 LINE1 / SIGNALING
			⟆		⟆
0/1	1	1	111	0	RMUXSH#2 LINE7 / SIGNALING
1	0	0	000	1	RMUXSH#0 COM SIGNALING
1	1	0	000	1	RMUXSH#1 COM SIGNALING
1	1	1	000	1	RMUXSH#2 COM SIGNALING

FIG. 723

SIG	ADS1 BLK	ADS1 SEL	
0	0 0 0 ~	0 0 ~ 1 1	USER CELL TO DTC 0/LINE 0 ~ USER CELL TO DTC 0/LINE 3
0	~ 1 1 1	0 0 ~ 1 1	USER CELL TO DTC 7/LINE 0 ~ USER CELL TO DTC 7/LINE 3
1	0 0 0 ~	0 0 ~ 1 1	LAP CELL TO DTC 0/LINE 0 ~ LAP CELL TO DTC 0/LINE 3
1	~ 1 1 1	0 0 ~ 1 1	LAP CELL TO DTC 7/LINE 0 ~ LAP CELL TO DTC 7/LINE 3

FIG. 724

5,638,360

SIG	UL	TAGC	PATH
0	0	000	BSGCSH#0/LINE0
			→ BSGC CARD NO.
			→ DAISY-CHAINED SHELF NO.
		⌇	⌇
0	0	111	BSGCSH#0/LINE5
0	1	000	BSGCSH#1/LINE0
0	1	001	BSGCSH#1/LINE1
		⌇	⌇
0	1	111	BSGCSH#1/LINE5

FIG. 725

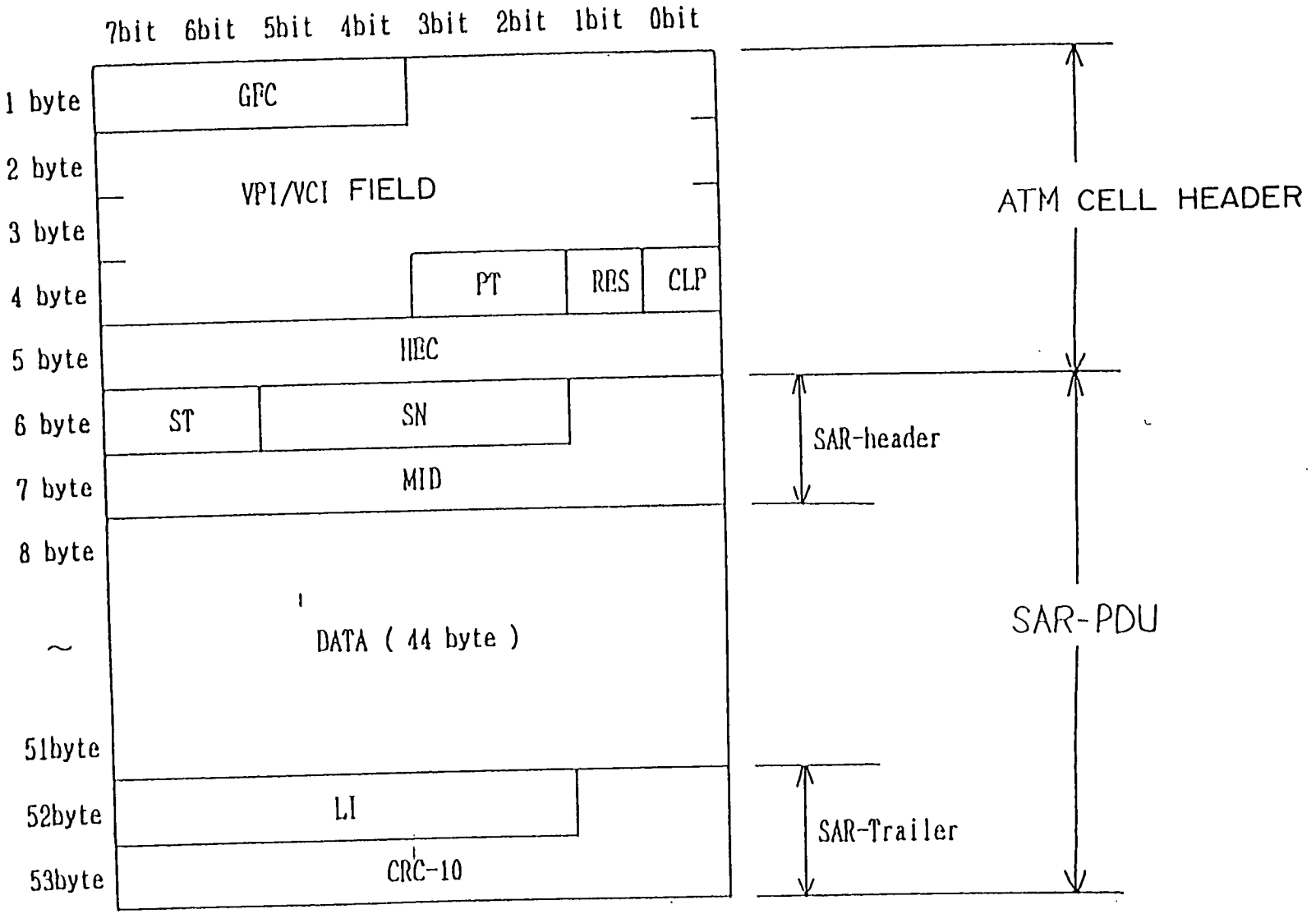

7bit 6bit 5bit 4bit 3bit 2bit 1bit 0bit
1 byte
2 byte
3 byte
4 byte
5 byte
6 byte
7 byte
8 byte
~
51byte
52byte
53byte
GFC
VPI/VCI FIELD
PT
RES
CLP
HEC
ST
SN
MID
DATA (44 byte)
LI
CRC-10
ATM CELL HEADER
SAR-header
SAR-PDU
SAR-Trailer

FIG. 726

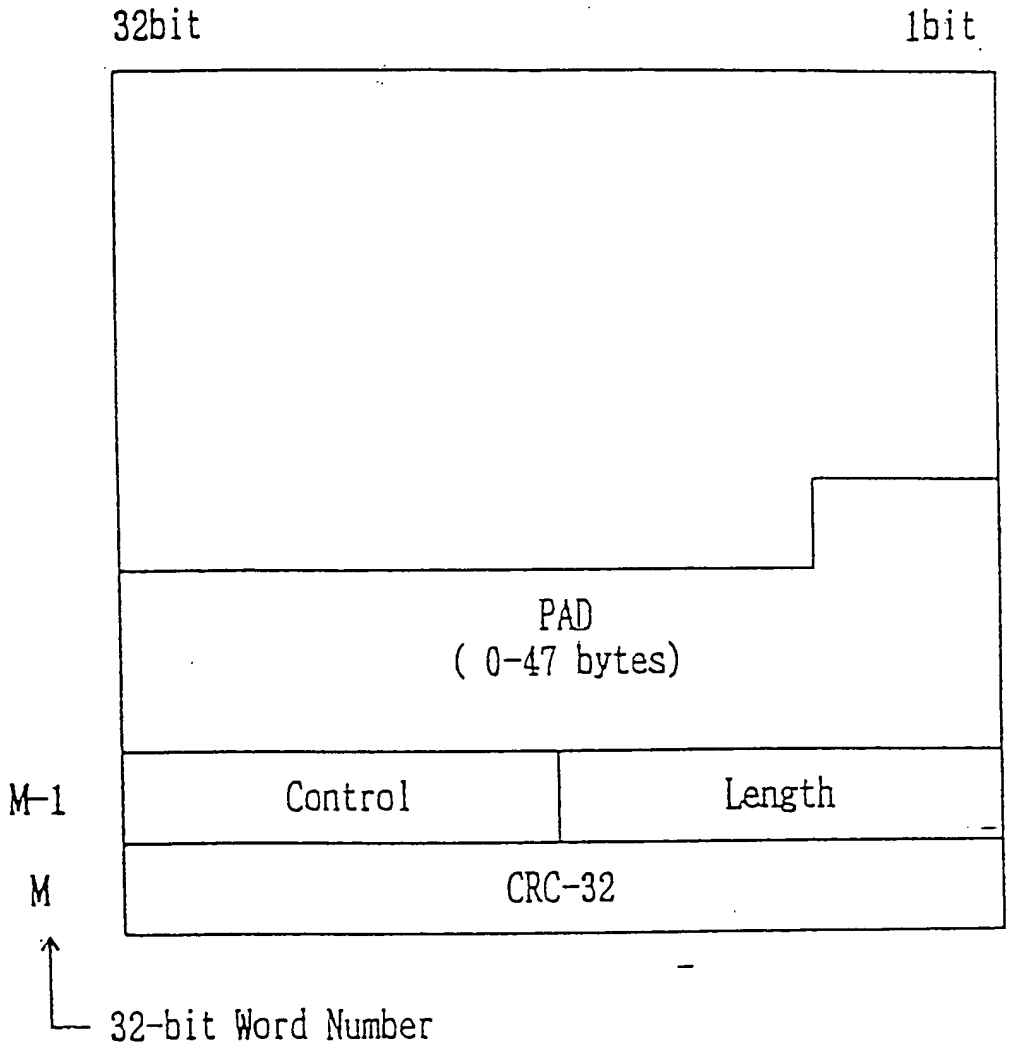

32bit
1bit
PAD
(0-47 bytes)
M-1
Control
Length
M
CRC-32
32-bit Word Number

FIG. 727

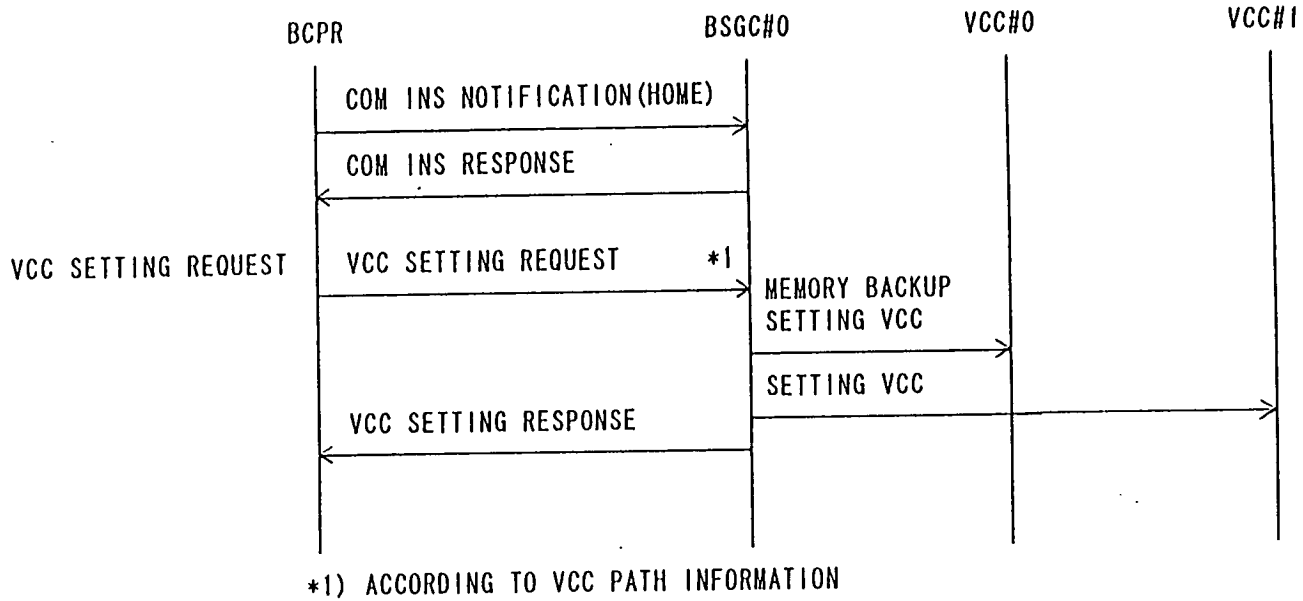
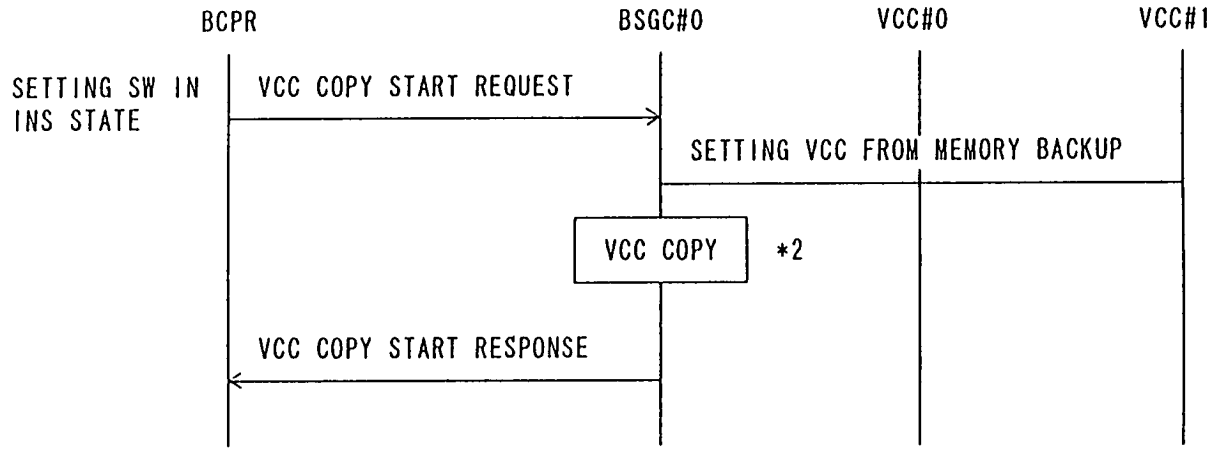
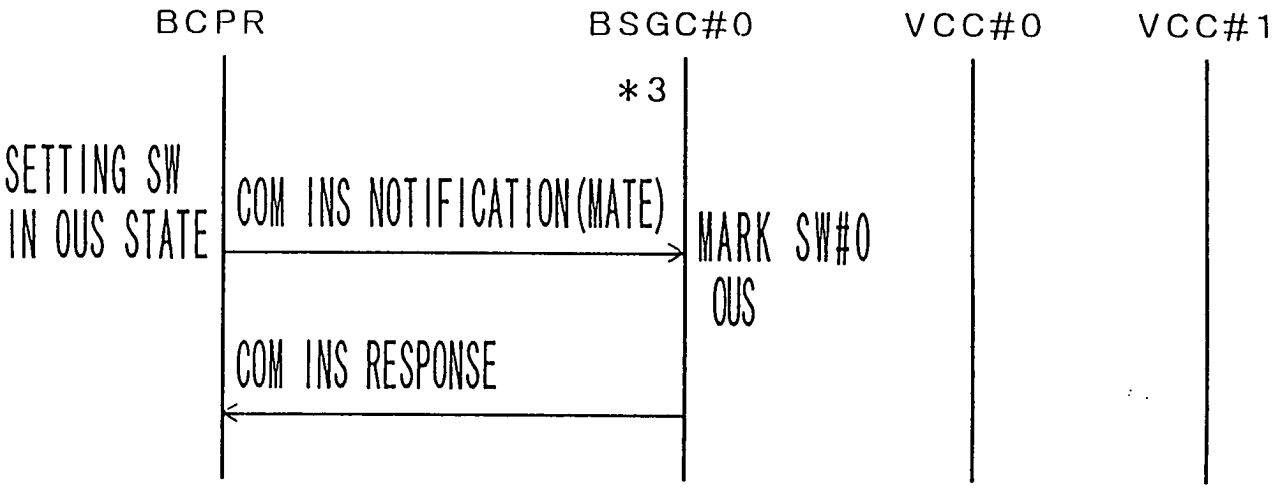

BCPR
BSGC#0
VCC#0
VCC#1
COM INS NOTIFICATION(HOME)
COM INS RESPONSE
VCC SETTING REQUEST
VCC SETTING REQUEST
*1
MEMORY BACKUP SETTING VCC
SETTING VCC
VCC SETTING RESPONSE
*1) ACCORDING TO VCC PATH INFORMATION

FIG. 728



*2) VCC CAN BE SET DURING VCC COPY PROCESS AFTERWARDS, VCC IS WRITTEN IN BOTH SYSTEMS.

FIG. 729



*3) AFTERWARDS, VCC IS WRITTEN IN ONLY INS SYSTEM(#1)

FIG. 730

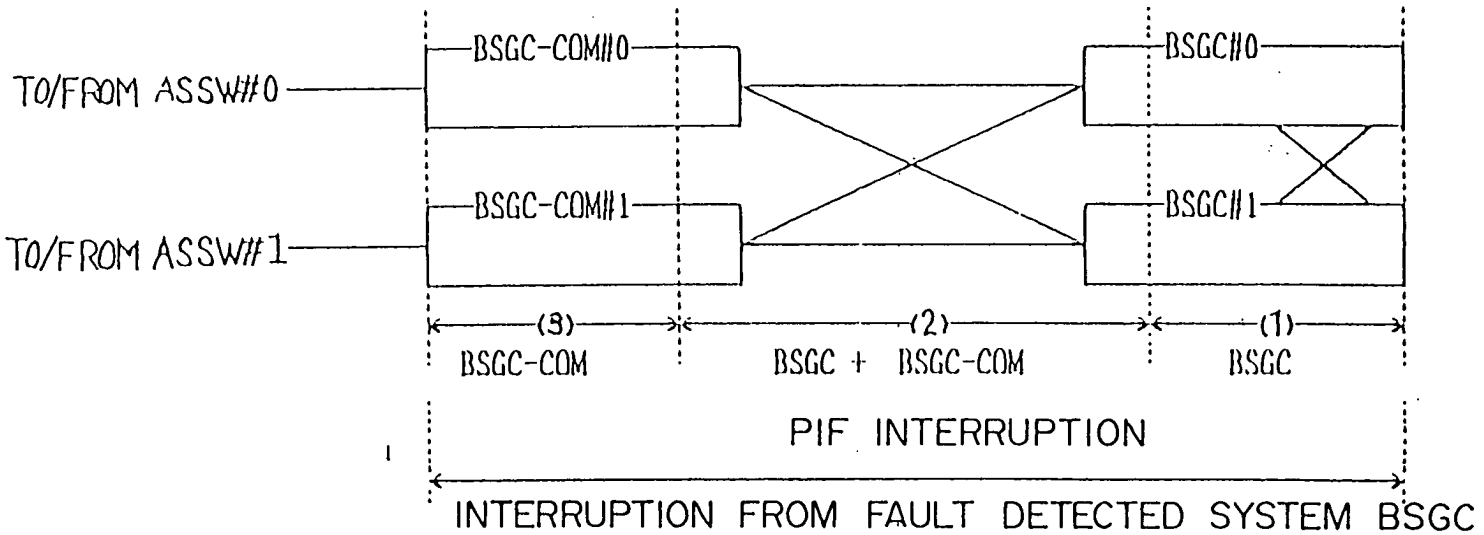
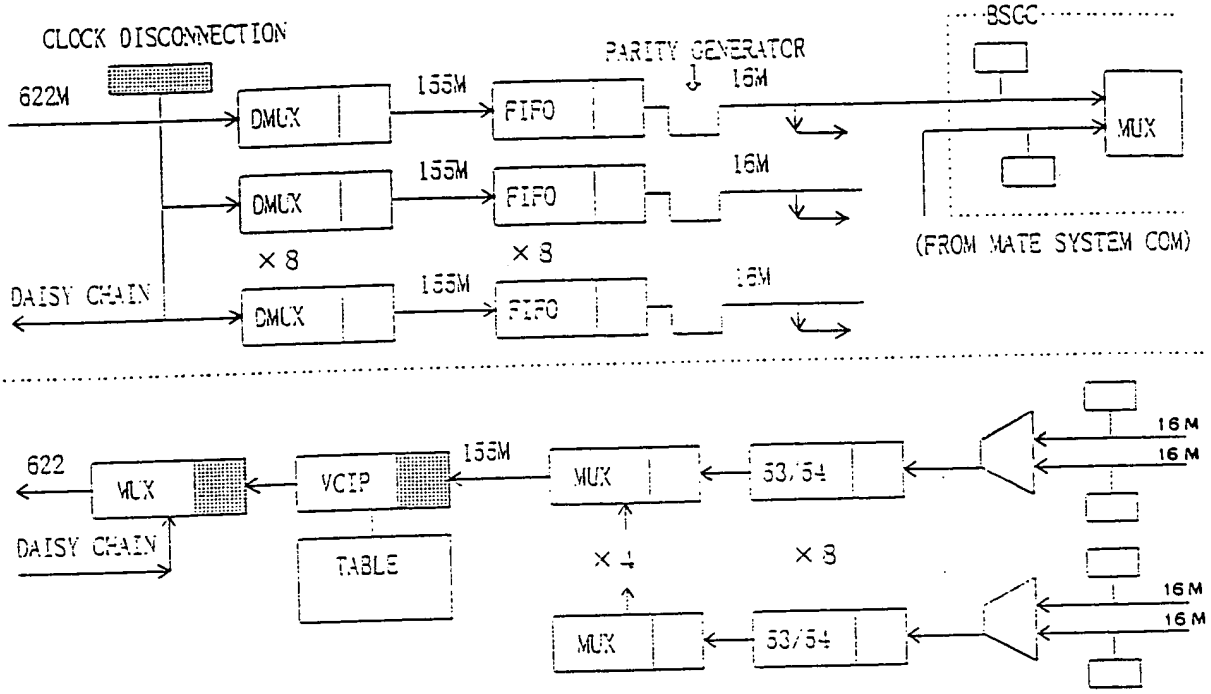

TO/FROM ASSW#0
TO/FROM ASSW#1
BSGC-COM#0
BSGC-COM#1
BSGC#0
BSGC#1
(3)
BSGC-COM
(2)
BSGC + BSGC-COM
(1)
BSGC
PIF INTERRUPTION
INTERRUPTION FROM FAULT DETECTED SYSTEM BSGC

FIG. 731



BSGC-PKG UNIT FAULT NOTIFICATION POINT

NOTIFICATION POINT FOR STARTING NUMBER BSGC-PKG
(FAULT POINT OF ONE PORTION OF COM UNIT)

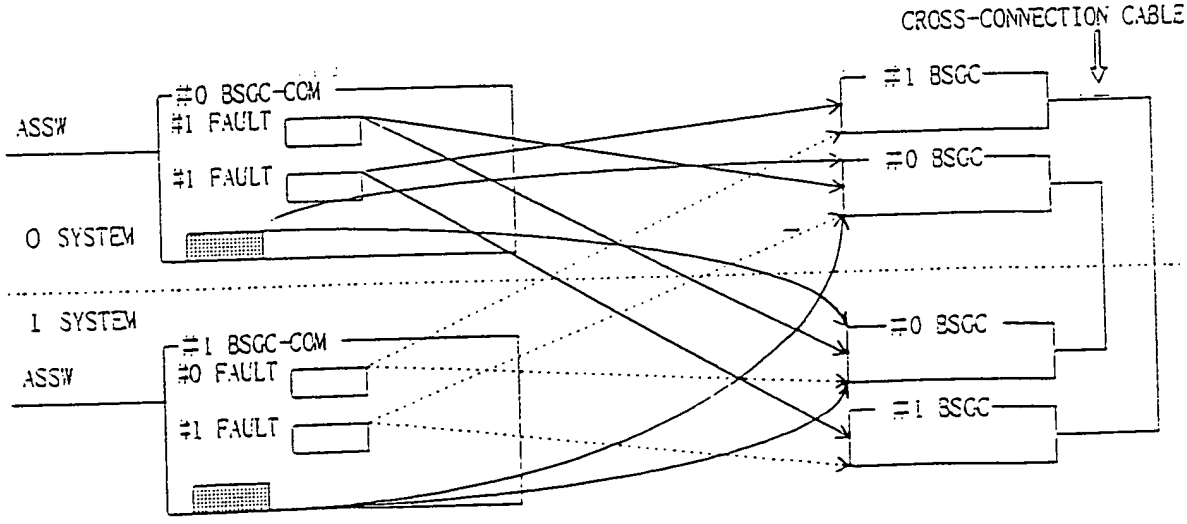


FIG. 732

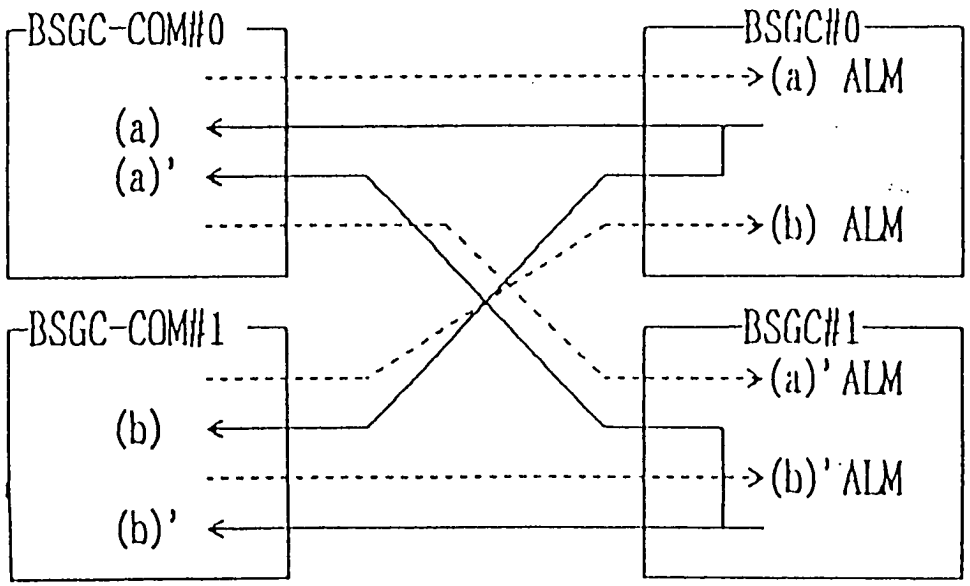


FIG. 733

FAULT POINT				AFTER-FAULT STATE OF BSGC SYSTEM		AFTER-FAULT STATE OF BSGC-COM SYSTEM		INTER-RUPTED BSGC SYSTEM	REMARKS
BSGC#0SCN		BSGC#1SCN							
(a)	(b)	(a)'	(b)'	#0	#1	#0	#1		
1	0	0	0	OUS	ACT	ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#1 → COM#0, COM#1 AVAILABLE
0	1	0	0	ACT	OUS	ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#0 → COM#0, COM#1 AVAILABLE
0	0	1	0	OUS	ACT	ACT/SBY	NO AMENDMENT	BSGC#1	BSGC#1 → COM#0, COM#1 AVAILABLE
0	0	0	1	ACT	OUS	ACT/SBY	NO AMENDMENT	BSGC#1	BSGC#0 → COM#0, COM#1 AVAILABLE

FIG. 734

FAULT POINT				AFTER-FAULT STATE OF BSGC SYSTEM		AFTER-FAULT STATE OF BSGC-COM SYSTEM		INTERRUPTED BSGC SYSTEM	REMARKS
BSGC#0SCN		BSGC#1SCN							
(a)	(b)	(a)'	(b)'	#0	#1	#0	#1		
1	1	0	0	OUS	ACT	(NOTE 1) ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#1 → COM#0, COM#1 AVAILABLE
0	0	1	1	ACT	OUS	(NOTE 2) ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#0 → COM#0, COM#1 AVAILABLE
1	0	1	0	(NOTE 3) ACT/SBY NO AMENDMENT		OUS	ACT	BSGC#0 BSGC#1	BSGC#0 → COM#1, AVAILABLE BSGC#1 → COM#1, AVAILABLE
0	1	0	1	(NOTE 4) ACT/SBY NO AMENDMENT		ACT	OUS	BSGC#0 BSGC#1	BSGC#0 → COM#0, AVAILABLE BSGC#1 → COM#0, AVAILABLE

FIG. 735

CASE-1

(a) — FAULT IN BSGC-COM#0, (b) — FAULT IN BSGC#0

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.
#0	#1	#0	#1	
OUS	ACT	OUS	ACT	

BSGC-COM-PKG=XXXXXX

CASE-2

(a) — FAULT IN BSGC#0 (b) — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.
#0	#1	#0	#1	
OUS	ACT	ACT	OUS	

BSGC-COM-PKG=XXXXXX

CASE-3

(a) — FAULT IN BSGC-COM#0, (b) — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇨ AFTER SWITCHING BSGC-COM xxxxx-PKG AND CONFIRMING NORMALITY ;
#0	#1	#0	#1	
OUS	ACT	OUS	ACT	

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇨ AFTER SWITCHING BSGC-COM xxxxx-PKG AND CONFIRMING NORMALITY ;
#0	#1	#0	#1	
OUS	ACT	ACT	OUS	

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

FIG. 736

CASE−1

(a)' — FAULT IN BSGC-COM#0, (b)' — FAULT IN BSGC#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
ACT	OUS	OUS	ACT

⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE−2

(a)' — FAULT IN BSGC#1 (b)' — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
ACT	OUS	ACT	OUS

⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHI BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE−3

(a) — FAULT IN BSGC-COM#0, (b) — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#i1
ACT	OUS	OUS	ACT

⇨ AFTER SWITCHING BSGC-COM xxxxx-PKG AND CONFIRMING NORMALITY ;

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
ACT	OUS	ACT	OUS

⇨ AFTER SWITCHING BSGC-COM xzxxx-PKG AND CONFIRMING NORMALITY ;

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

FIG. 737

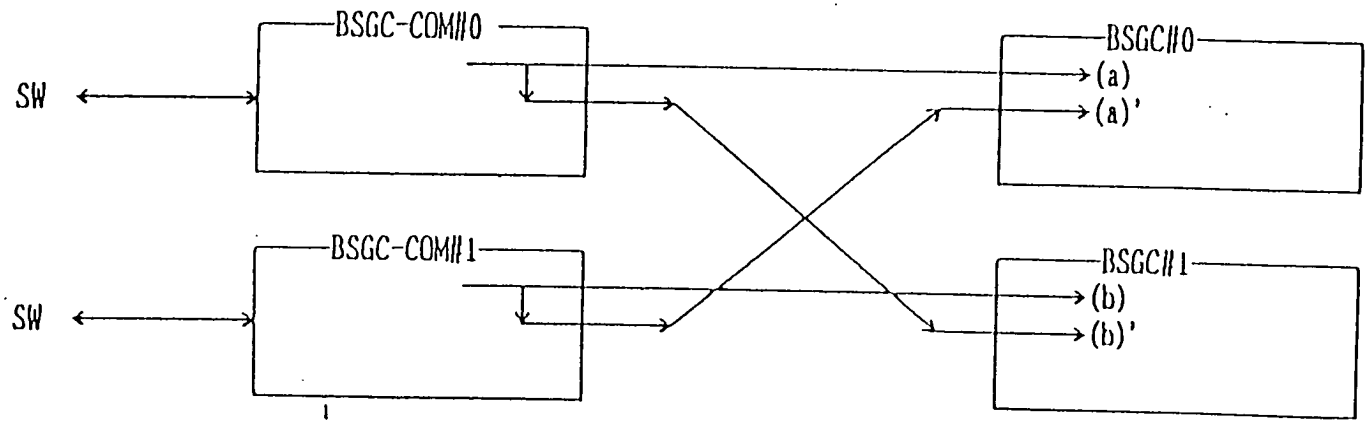


FIG. 738

FAULT POINT				AFTER-FAULT STATE OF BSGC SYSTEM		AFTER-FAULT STATE OF BSGC-COM SYSTEM		INTER-RUPTED BSGC SYSTEM	REMARKS
BSGC#0SCN		BSGC#1SCN							
(a)	(b)	(a)'	(b)'	#0	#1	#0	#1		
1	0	0	0	OUS	ACT	ACT/SBY	NO AMENDMENT	BSGC#0	
				DIAGNOSTICS EXECUTED : FORLLOWING STATE IS ENTERED WHEN N.G. IS SPECIFIED FOR BSGC-COM #0 WHEN N.G. IS SPECIFIED FOR BSGC#0, BSGC#0 IS MAINTAINED ONLY.					
				SBY	ACT	OUS	ACT	—	BSGC-COM#0 MAINTENANCE
0	1	0	0	ACT	OUS	ACT/SBY	NO AMENDMENT	BSGC#1	
				DIAGNOSTICS EXECUTED : FORLLOWING STATE IS ENTERED WHEN N.G. IS SPECIFIED FOR BSGC-COM #0 WHEN N.G. IS SPECIFIED FOR BSGC#1, BSGC#1 IS MAINTAINED ONLY.					
				ACT	SBY	OUS	ACT	—	BSGC-COM#0 MAINTENANCE
0	0	1	0	OUS	ACT	ACT/SBY	NO AMENDMENT	BSGC#0	
				DIAGNOSTICS EXECUTED : FORLLOWING STATE IS ENTERED WHEN N.G. IS SPECIFIED FOR BSGC-COM #1 WHEN N.G. IS SPECIFIED FOR BSGC#0, BSGC#0 IS MAINTAINED ONLY.					
				SBY	ACT	ACT	OUS	—	BSGC-COM#1 MAINTENANCE
0	0	0	1	ACT	OUS	ACT/SBY	NO AMENDMENT	BSGC#1	
				DIAGNOSTICS EXECUTED : FORLLOWING STATE IS ENTERED WHEN N.G. IS SPECIFIED FOR BSGC-COM #1 WHEN N.G. IS SPECIFIED FOR BSGC#1, BSGC#1 IS MAINTAINED ONLY.					
				ACT	SBY	ACT	OUS	—	BSGC-COM#1 MAINTENANCE

FIG. 739

FAULT POINT				AFTER-FAULT STATE OF BSGC SYSTEM				INTERRUPTED BSGC SYSTEM	REMARKS
BSGC#0SCN		BSGC#1SCN							
(a)	(b)	(a)	(b)	#0	#1	#0	#1		
1	1	0	0	(NOTE1) ACT/SBY	NO AMENDMENT	OUS	ACT	BSGC#0 BSGC#1	BSGC#0 → COM#1 AVAILABLE BSGC#1 → COM#1 AVAILABLE
0	0	1	1	(NOTE2) ACT/SBY	NO AMENDMENT	ACT	OUS	BSGC#0 BSGC#1	BSGC#0 → COM#0 AVAILABLE BSGC#1 → COM#0 AVAILABLE
1	0	1	0	OUS	ACT	(NOTE3) ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#1 → COM#0, COM#1 AVAILABLE
0	1	0	1	ACT	OUS	(NOTE4) ACT/SBY	NO AMENDMENT	BSGC#1	BSGC#0 → COM#0, COM#1 AVAILABLE

FIG. 740

CASE−1

(a) — FAULT IN BSGC-COM#0, (a)' — FAULT IN BSGC#0

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	OUS	ACT

⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE−2

(a) — FAULT IN BSGC#0 (a)' — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	ACT	OUS

⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE−3

(a) — FAULT IN BSGC-COM#0, (a)' — FAULT IN BSG-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	OUS	ACT

⇨ AFTER SWITCHING COM#0 xxxxx-PKG AND CONFIRMING NORMALITY ;

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	ACT	OUS

⇨ AFTER SWITCHING COM#1 xxxxx-PKG AND CONFIRMING NORMALITY ;

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

FIG. 741

CASE−1

(b) — FAULT IN BSGC-COM#1, (b)' — FAULT IN BSGC#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
ACT	OUS	OUS	ACT

⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE−2

(b) — FAULT IN BSGC#1 (b)' — FAULT IN BSGC-COM#0

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
ACT	OUS	ACT	OUS

⇨ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE−3

(b) — FAULT IN BSGC-COM#0, (b) — FAULT IN BSG-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
ACT	OUS	OUS	ACT

⇨ AFTER SWITCHING COM#0 xxxxx-PKG AND CONFIRMING NORMALITY ;

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
ACT	OUS	ACT	OUS

⇨ AFTER SWITCHING COM#1 xxxxx-PKG AND CONFIRMING NORMALITY ;

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

FIG. 742

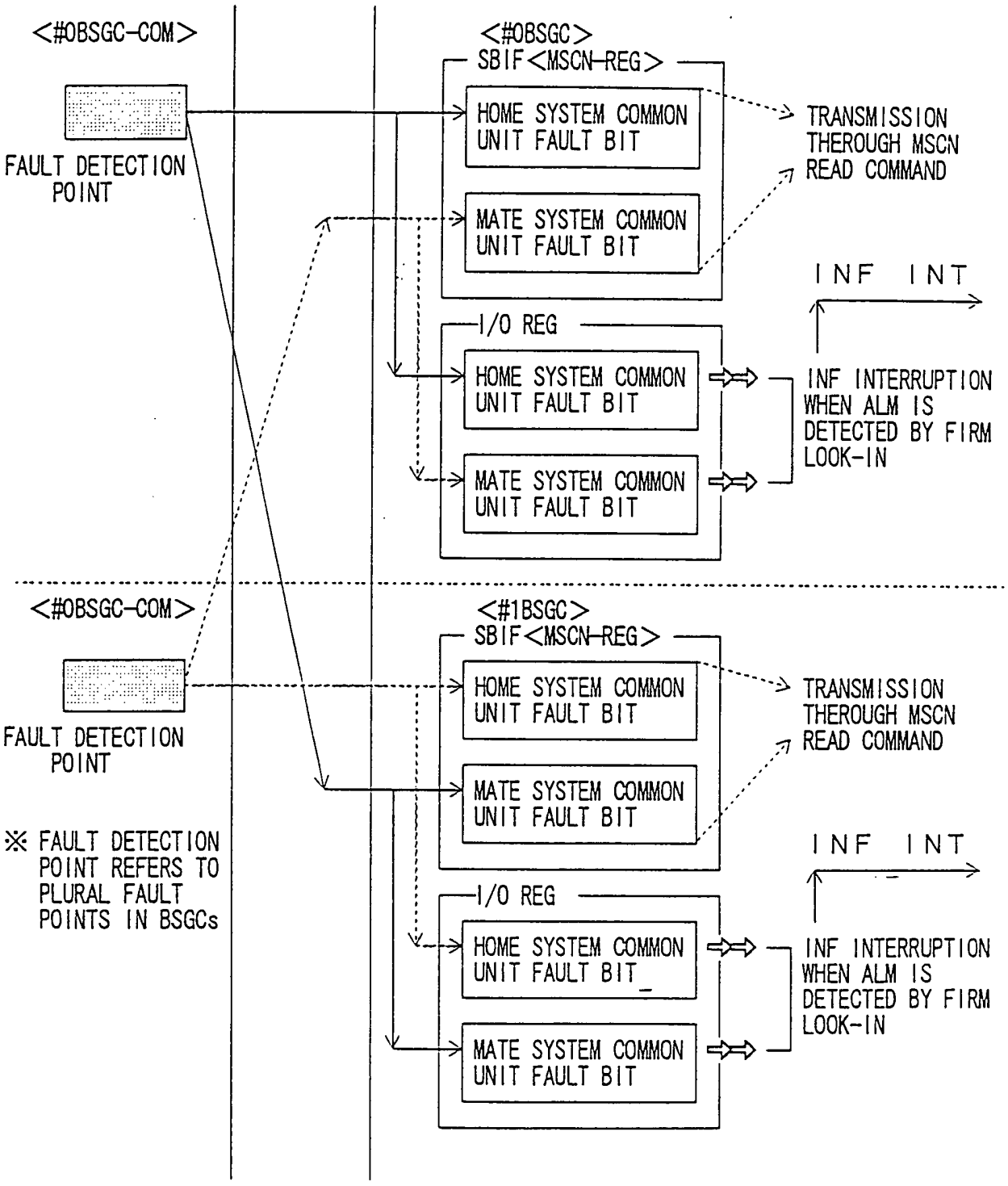

<#OBSGC-COM>
FAULT DETECTION POINT
<#OBSGC>
SBIF<MSCN-REG>
HOME SYSTEM COMMON UNIT FAULT BIT
MATE SYSTEM COMMON UNIT FAULT BIT
TRANSMISSION THEROUGH MSCN READ COMMAND
I/O REG
HOME SYSTEM COMMON UNIT FAULT BIT
MATE SYSTEM COMMON UNIT FAULT BIT
INF INT
INF INTERRUPTION WHEN ALM IS DETECTED BY FIRM LOOK-IN
<#OBSGC-COM>
FAULT DETECTION POINT
※ FAULT DETECTION POINT REFERS TO PLURAL FAULT POINTS IN BSGCs
<#1BSGC>
SBIF<MSCN-REG>
HOME SYSTEM COMMON UNIT FAULT BIT
MATE SYSTEM COMMON UNIT FAULT BIT
TRANSMISSION THEROUGH MSCN READ COMMAND
I/O REG
HOME SYSTEM COMMON UNIT FAULT BIT
MATE SYSTEM COMMON UNIT FAULT BIT
INF INT
INF INTERRUPTION WHEN ALM IS DETECTED BY FIRM LOOK-IN

FIG. 743

No	CONTENTS	CC INTERRUPTION	F I RM INTERRUPTION	MSCN-BIT	FAULT CORRECTING PROCESS	REMARKS
1	INF DMA ACCESS ERROR 1	EXISTING	EXISTING	28	RETRIAL PROCESS FAULT IF NG	ANSWER SBER1- BIT=1. AT DMA-TRANSFER, INFT PARITY CHECKER GENERATES N. G. IN BSGC⟶ PFT DIRECTION.
2	INF DMA ACCESS ERROR 2	EXISTING	EXISTING	27	RETRIAL PROCESS FAULT IF NG	ANSWER SBER2-BIT=1. AT DMA-TRANSFER, INFT BECOMES BERR THROUGH ACCESS TO TOXBUS AND DMA ADDRES GUARD ERROR OCCURS.
3	INF DMA PARITY ERROR	EXISTING	EXISTING	26	RETRIAL PROCESS FAULT IF NG	ERROR OCCURS IN PARITY CHECK OF ANSWER RECEPTION DATA.
4	INF DMA TIMEOVER	EXISTING	EXISTING	25	RETRIAL PROCESS FAULT IF NG	TIME NOMITOR TIMER INDICATES "OVER" DURING PERIOD FROM DMA ACCESS TERMINATION TO ANSWER (NO ANSWER)
5	BSGC FAULT	EXISTING	EXISTING	23	SETTING AS OUS STATE SYSTEM SWITCH FOR ACT SYSTEM	BSGC FAULT ① WATCH DOG TIMER OVER ② DRAM PARITY N. G ③ WRITE PROTECT ERROR

FIG. 744

BIT	C O N T E N T S	
31	RESET COMPLETION INDICATOR	
30	(DON'T CARE)	
29	BSGC FAULT	(1)
28	DMA ACCESS ERROR 1 (OCCURRENCE OF ANSWER ER1)	(1)
27	DMA ACCESS ERROR 2 (OCCURRENCE OF ANSWER ER2)	(1)
26	DMA PARITY ERROR	(1)
25	DMA TIME OVER	(1)
24	HPAL : HOME BSGC-COM OBP FAULT	(3)
23	MPAL : MATE BSGC-COM OBP FAULT	(3)
22	MFAL : MATE FUSE ALRAM (MATE SYSTEM HPT01A LOADED FUSE DISCONNECTION STATE)	(3)
21	HOME SYSTEM BSGC-COM FAULT-1 ☆VALID BIT FOR ONLY STARTING NUMBER BSGC	(3)
20	MATE SYSTEM BSGC-COM FAULT-1 ☆VALID BIT FOR ONLY STARTING NUMBER BSGC	(3)
19	HOME SYSTEM BSGC-COM FAULT-2	(3)
18	MATE SYSTEM BSGC-COM FAULT-2	(3)
17	(DON'T CARE)	
16	(DON'T CARE)	
15	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN HOME SYSTEM DATA PARITY N.G	(2)
14	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN HOME SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
13	(DON'T CARE)	
12	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM DATA PARITY N.G	(2)
11	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
10	(DON'T CARE)	
09	BSGC—BSGC-COM DETECTION FAULT AT BSGC IN HOME SYSTEM DATA PARITY N.G	(2)
08	BSGC—BSGC-COM DETECTION FAULT AT BSGC IN HOME SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
07	(DON'T CARE)	
06	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM DATA PARITY N.G	(2)
05	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
04	(DON'T CARE)	
03	(DON'T CARE)	
02	(DON'T CARE)	
01	(DON'T CARE)	
00	(DON'T CARE)	

☆···BITS 21-16 RECEIVES REPORT FROM STARTING NUMBER BSGC ONLY. OTHER BSGCFs ARE "DON'T CARE".

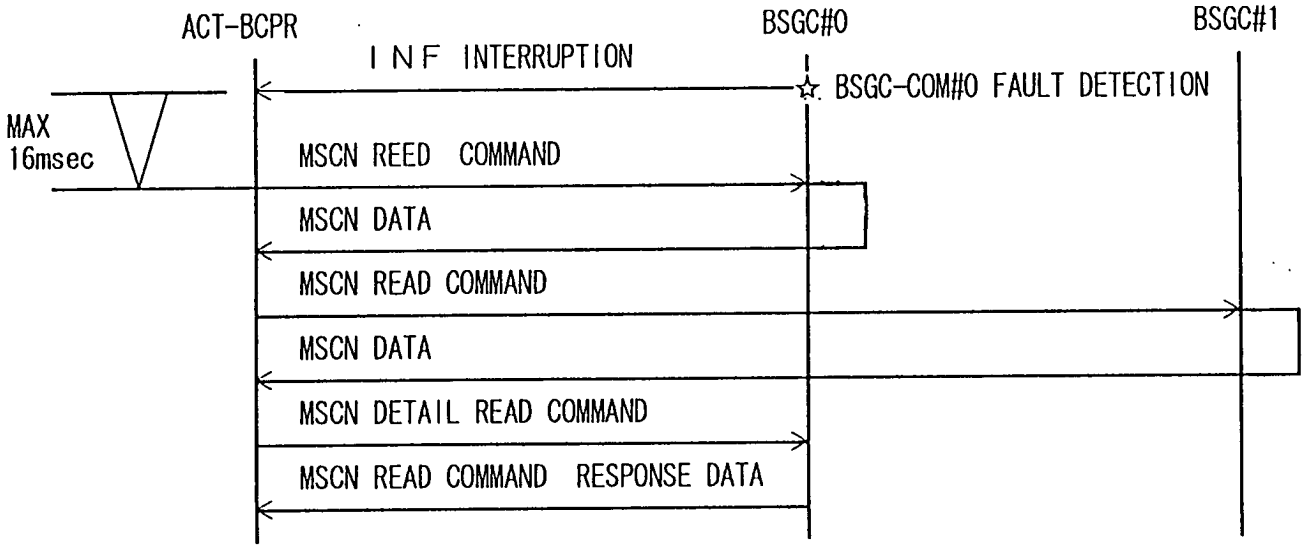
FIG. 745

	BSGC FAULT	29	WATCH DOG TIME OVER, DRAM PARITY N.G, DRAM WRITE PROTECT ERR MUX LSI ALM FOR ACT/SBY-LINK MULTIPLEX, 54/53 CNV ALM, PIF RETRY OUT

FIG. 746

NO	MSCN CONTENTS	BIT NO	DETAILED FACTOR LISTING
2	HOME-SYSTEM BSGC-COM FAULT-1	21	BIT INDICATING ONLY STARTING NUMBER BSGC ALL SUBSEQUENT BITS ARE FAULT BITS IN HOME SYSTEM BSGC-COM. 1)MUX UNIT IN HOME SYSTEM IS FAULTY.
3	MATE-SYSTEM BSGC-COM FAULT-1	20	BIT INDICATING ONLY STARTING NUMBER BSGC ALL SUBSEQUENT BITS ARE FAULT BITS IN MATE SYSTEM BSGC-COM. 1)MUX UNIT IN MATE SYSTEM IS FAULTY.
4	HOME-SYSTEM BSGC-COM FAULT-2	19	FAULT NOTIFICATION FROM EACH BSGC. ALL FAULT ARE FROM BSGC-COM IN HOME SYSTEM. EACH BSGC-PKG CORRESPONDING UNIT 1)MUX UNIT IN HOME SYSTEM IS FAULTY. 2)DMUX-VCC UNIT IN HOME SYSTEM IS FAULTY. 3)BSGC-CORRESPOMDING MUX UNIT IN HOME SYSTEM IS FAULTY.
5	MATE-SYSTEM BSGC-COM FAULT-2	18	FAULT NOTIFICATION FROM EACH BSGC. ALL FAULTS ARE FROM BSGC-COM IN MATE SYSTEM. EACH BSGC-PKG CORRESPONDING UNIT 1)MUX UNIT IN MATE SYSTEM IS FAULTY. 2)DMUX-VCC UNIT IN MATE SYSTEM IS FAULTY. 3)BSGC-CORRESPONDING MUX UNIT IN MATE SYSTEM IS FAULTY.

FIG. 747


ACT-BCPR
BSGC#0
BSGC#1
I N F INTERRUPTION
BSGC-COM#0 FAULT DETECTION
MAX
16msec
MSCN REED COMMAND
MSCN DATA
MSCN READ COMMAND
MSCN DATA
MSCN DETAIL READ COMMAND
MSCN READ COMMAND RESPONSE DATA

F I G. 7 4 8

6692E0 EP2772860

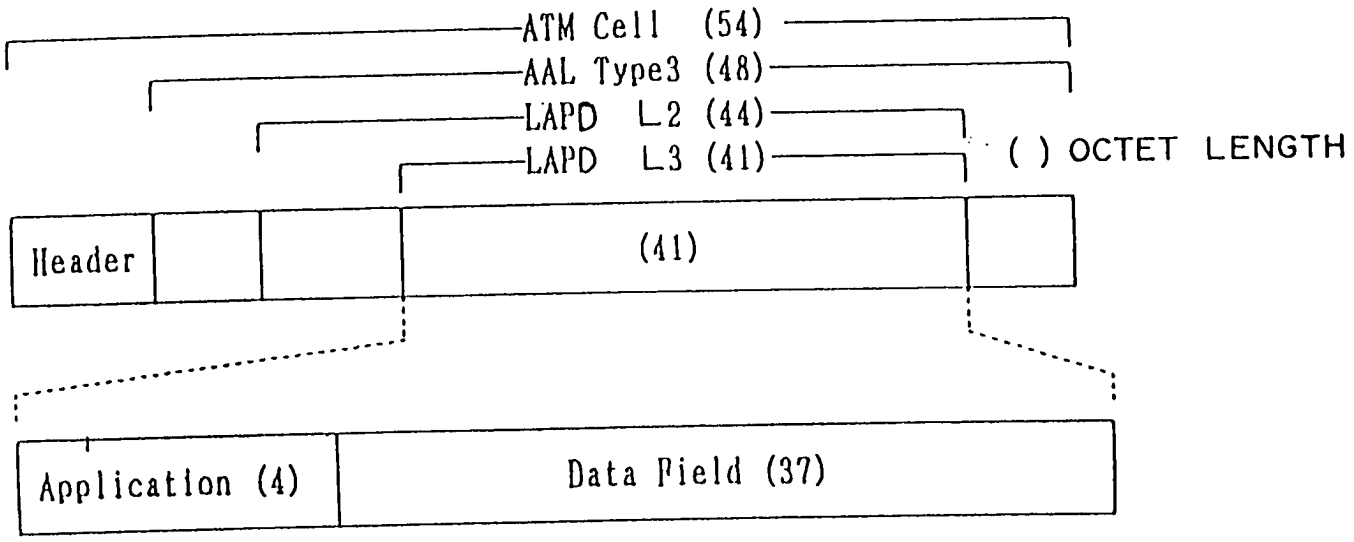


FIG. 749

69260 ET27260

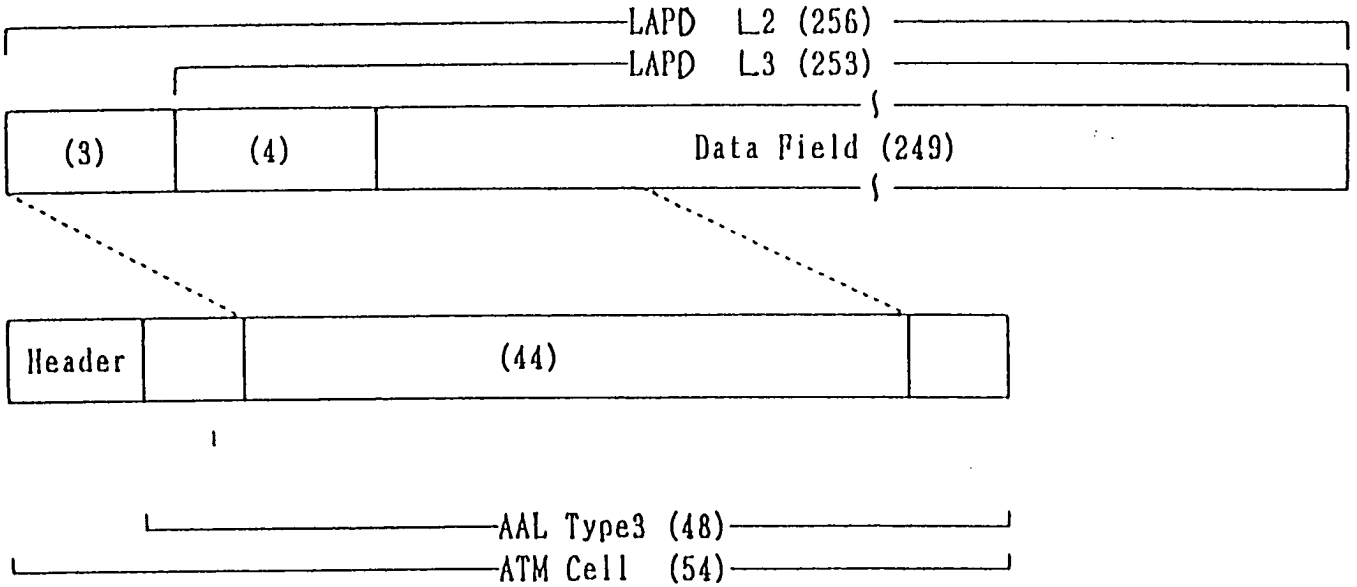


FIG. 750

6692E0 ET22260

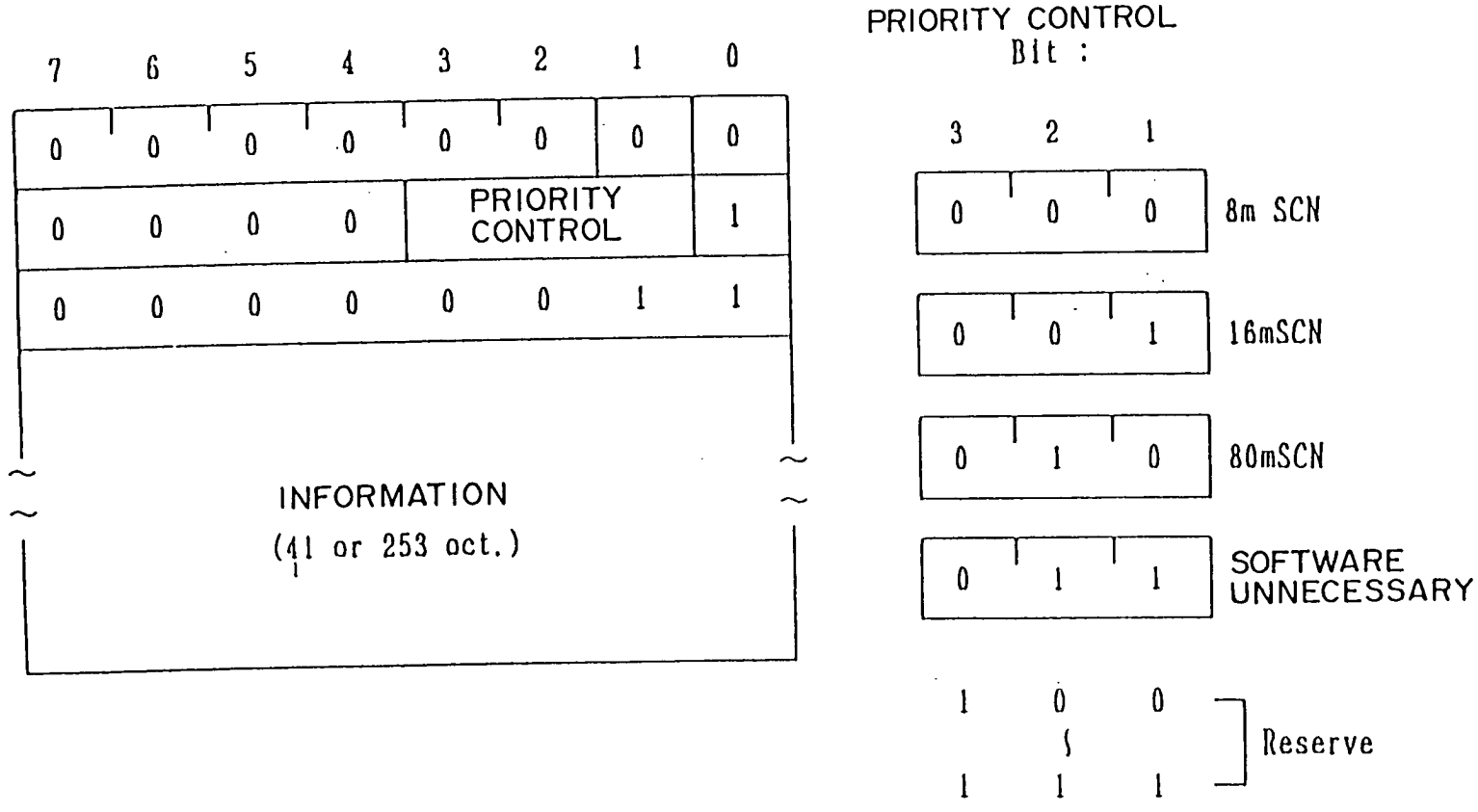


FIG. 751

Fig 6.1.3 UI FORMAT (SIFSH⇒BSGC)

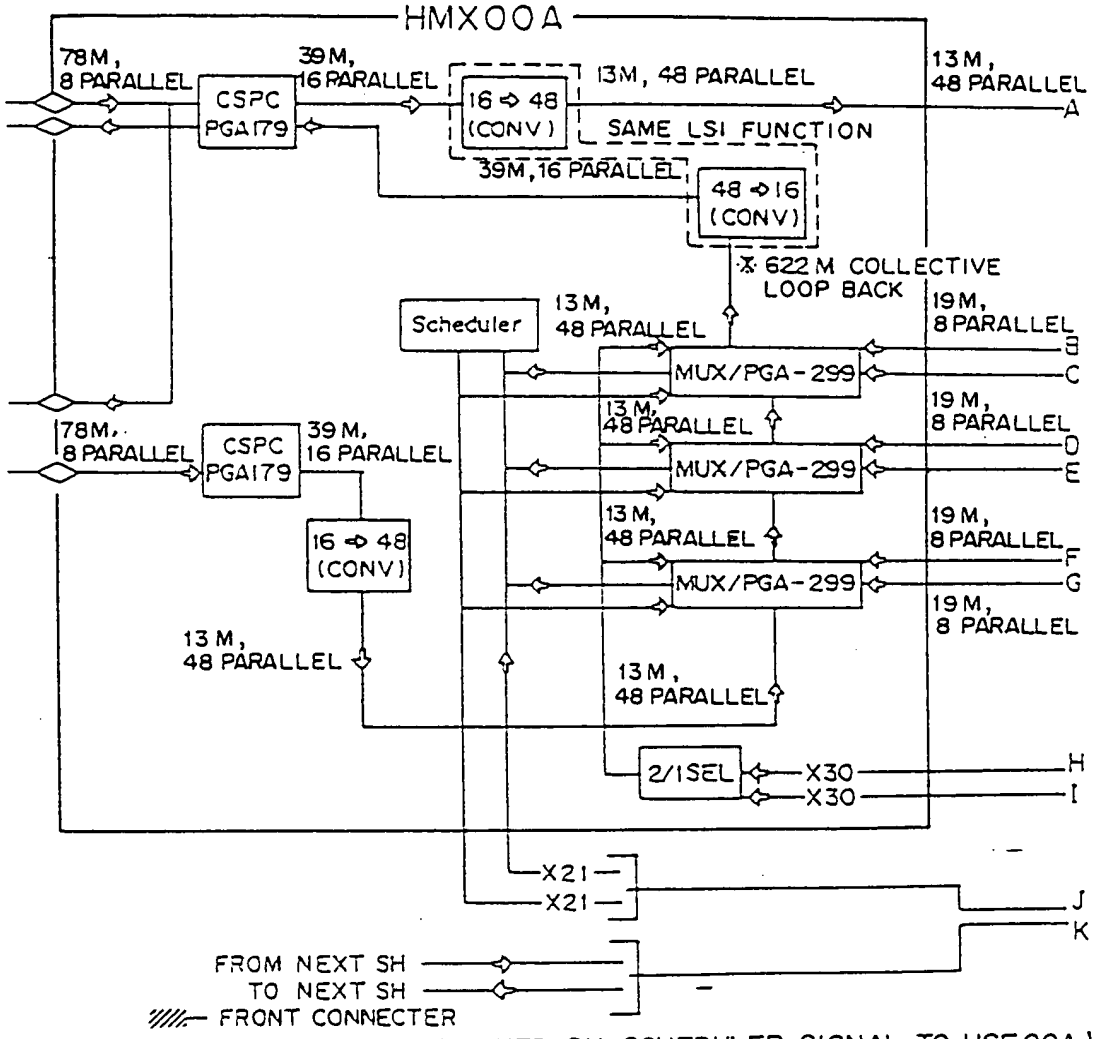
LENGTH	APDI	
MESG	NS	0
COMMAND ID	00	
USER INFORMATION		

MAXIMUM LENGTH 512 BYTE

THIS FORMAT IS DIFFERENT IN SIMPLE LAP AND FULL LAPD IN THE FOLLOWING POINTS.
1. MAXIMUM MESSAGE LENGTH IS 509 BYTES FOR SIMPLE LAP.
2. NS FIELD IS FIXED AT 0 FOR FULL LAPD.

APID/MESG VALUE IS CENTRALLY MANAGED BY SOFTWARE FOR ALL DEVICES.

FIG. 752



(CONNECTOR FOR DAISY-CHAINED SH SCHEDULER SIGNAL TO HSF00A)

FIG. 753

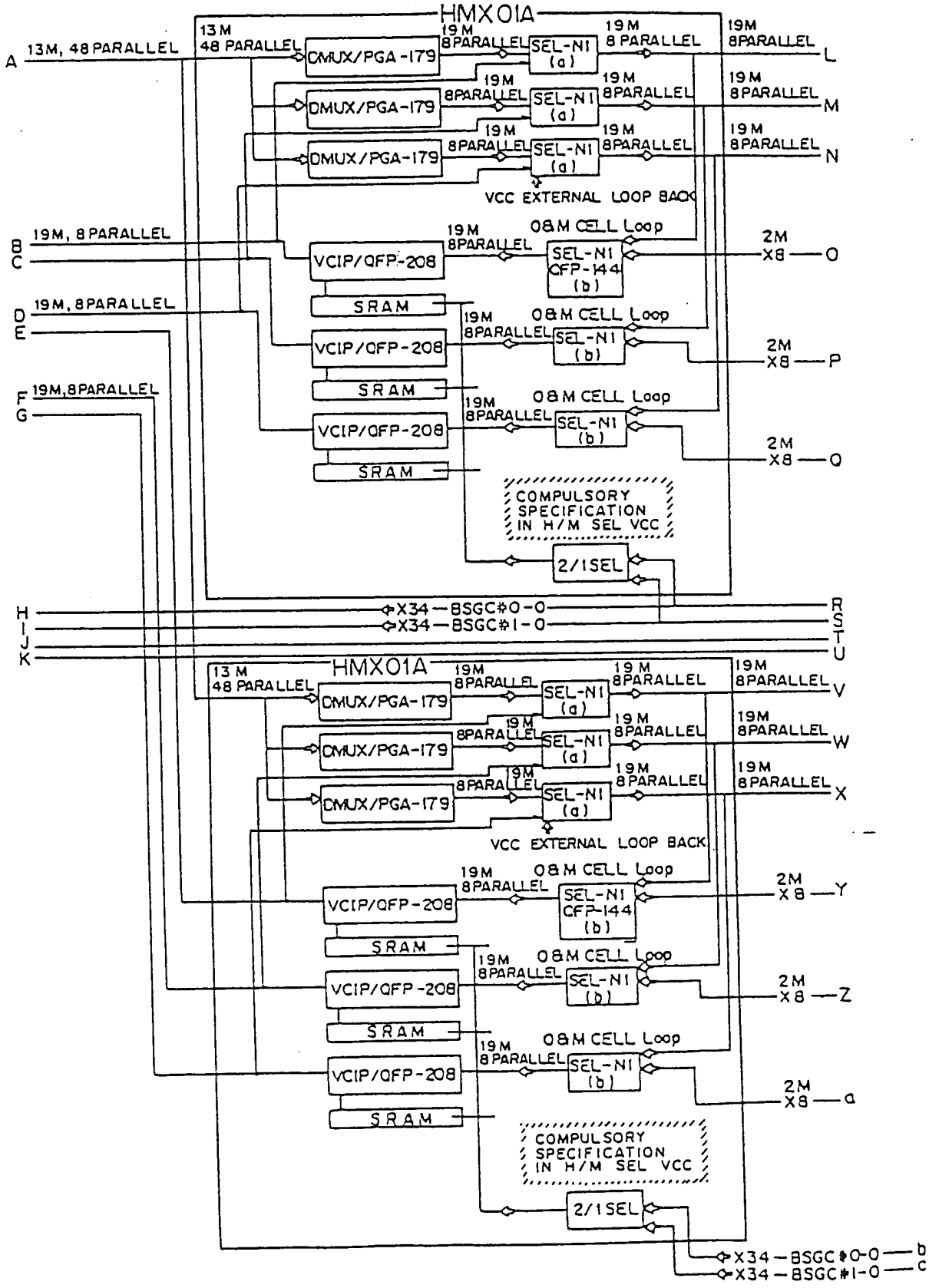

HMX01A
13M, 48 PARALLEL
13M 48 PARALLEL
DMUX/PGA-179
19M 8PARALLEL
SEL-N1 (a)
19M 8 PARALLEL
19M 8PARALLEL
L
M
N
VCC EXTERNAL LOOP BACK
19M, 8 PARALLEL
VCIP/QFP-208
08M CELL Loop
SEL-N1 QFP-144 (b)
2M X8
O
P
Q
SRAM
COMPULSORY SPECIFICATION IN H/M SEL VCC
2/1SEL
X34 — BSGC#0-0
X34 — BSGC#1-0
R
S
T
U
V
W
X
Y
Z
a
b
c

FIG. 754

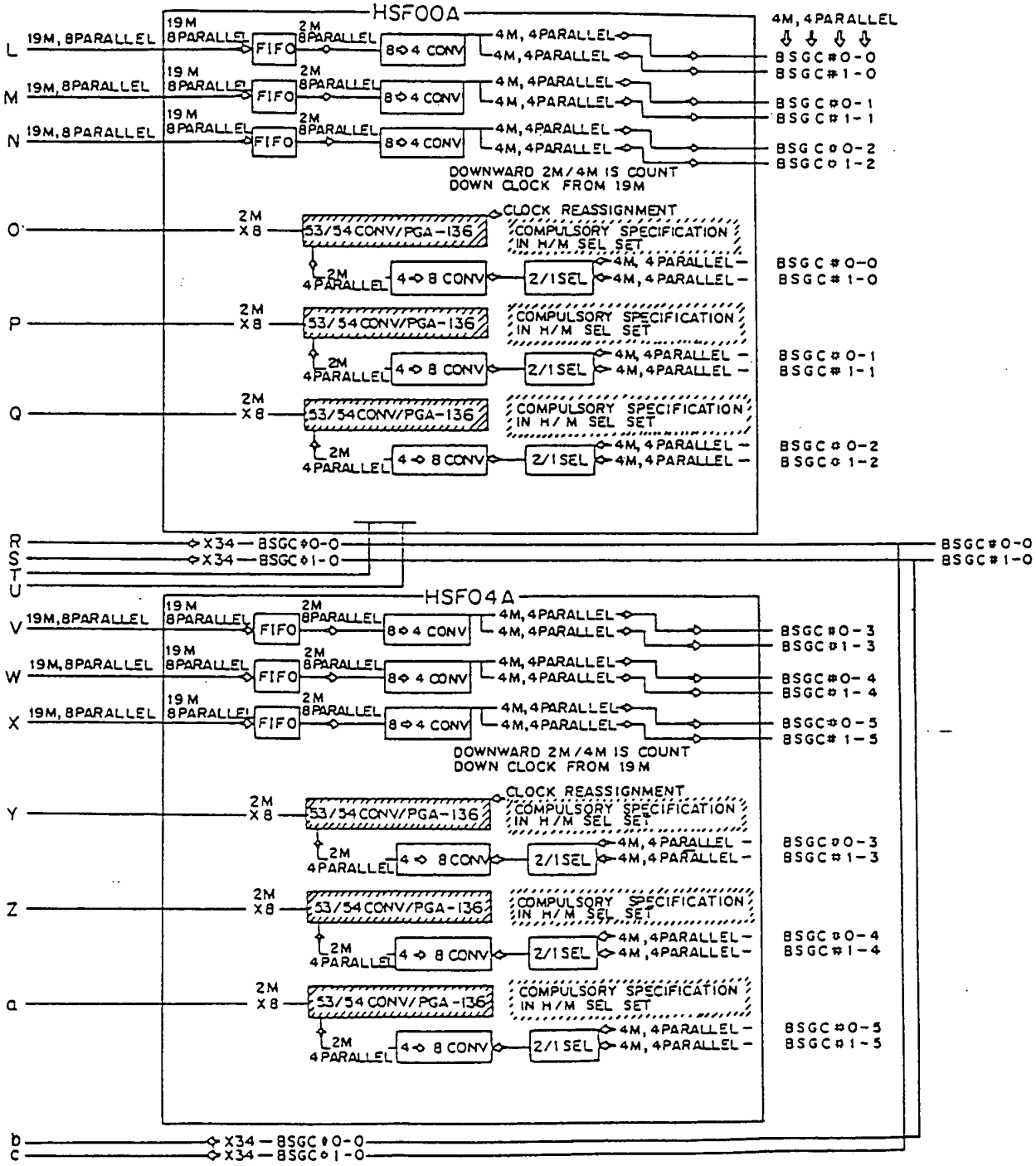

HSF00A
HSF04A
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z
a
b
c
19M, 8PARALLEL
19M 8PARALLEL
2M 8PARALLEL
FIFO
8⇔4 CONV
4M, 4PARALLEL
BSGC#0-0
BSGC#1-0
BSGC#0-1
BSGC#1-1
BSGC#0-2
BSGC#1-2
DOWNWARD 2M/4M IS COUNT DOWN CLOCK FROM 19M
2M X8
53/54 CONV/PGA-136
CLOCK REASSIGNMENT
COMPULSORY SPECIFICATION IN H/M SEL SET
2M 4PARALLEL
4⇔8 CONV
2/1 SEL
X34 — BSGC#0-0
X34 — BSGC#1-0
BSGC#0-3
BSGC#1-3
BSGC#0-4
BSGC#1-4
BSGC#0-5
BSGC#1-5

FIG. 755

HMX00A

NO	FUNCTION BLOCK NAME	OUTLINE OF FUNCTIONS	MAIN LSI
1	CSPC	LEVEL IS CONVERTED BETWEEN ECL AND TTL OF 622M UP/DOWN DATA BY INTERFACING WITH ASSWSH. CONVERSION BETWEEN ECL LEVEL 8 BITS, 78M AND LEVEL 16 BITS, 39M.	MB222M607-CR-G
2	16 ⇨ 48 16 ⇦ 48 CONV (CSPCAD)	AMENDMENT IS MADE FROM 39M, 16 BITS TO 13M, 48 BITS OR FROM 13M, 48 BITS TO 39M, 16 BITS.	MBCG10572-607CR-G
3	SCHEDULER	MAIN FUNCTION OF SCHEDULER CAPABLE OF CELL MULTIPLEXING CONTROL FOR HOME SH 6BSGC AND LOWER SH 6BSGC IS REALIZED BY LCA.	64K EPROM LCA E76C-0024-0740 #6470G132
4	MUX	156M CELL 2 SYSTEM AND 622M HIGH SPEED CELL 1 SYSTEM CAN BE MULTIPLEXED. MULTIPLEXER.	MBCG31204-639CR-G
5	2/1 SEL	DATA, ADD, SELECTOR OF CONTROL LINE, AND ACT-BSGC ARE SELECTED FROM HOME/MATE SYSTEM STARTING NUMBER BSGC.	————

FIG. 756

HMX01A

NO	FUNCTION BLOCK NAME	OUTLINE OF FUNCTIONS	MAIN LSI
1	DMUX	TAG IS DETECTED FROM CELL OF 622M, MATCHED WITH PREDETERMINED TAG INFORMATION, AND OUTPUT AS 156M CELL IF THEY MATCH. INPUT 13M, 48 PARALLEL ⇨ OUTPUT 19M, 8 PARALLEL	MBCG31204-638CR-G
2	SEL-N1 (a)	FOR CELL BY CELL LOOPBACK TO BSGC SPECIFYING LOOPBACK CELL FROM O-BIT IN TAG.	MBCG21104-616ZFV
3	SEL-N1 (b)	FOR CELL BY CELL LOOPBACK TO ASSWSH SPECIFYING LOOPBACK CELL FROM O-BIT IN TAG. VCI OF TEST CELL IS SPECIFIED BY SPECIFIC VRLUE. VCI=03FE, 03FF	MBCG21104-616ZFV
4	VCIP	REALIZING VCC FUNCTION. EXTERNALLY PROVIDING MEMORY AND CONVERTING CELL1-6 OCT DATA TO A VALUE WRITTEN TO MEMORY. AS SRAM, 64K × 16BIT CMOS SRAM (TC551664J-20 : FROM TOSHIBA)	MBCG21503-609ZFV E76L-0025-0269## 5164-20
5	2/1 SEL	DATA, ADD, SELECTOR OF CONTROL LINE, AND ACT-BSGC ARE SELECTED FROM HOME/MATE SYSTEM STARTING NUMBER BSGC.	————

FIG. 757

HSF00A/HSF04A

NO	FUNCTION BLOCK NAME	OUTLINE OF FUNCTIONS	MAIN LSI
1	FIFO	MEMORY FOR USE IN CONVERTING FROM 19M, 8 PARALLEL TO 1M, 8 PARALLEL	IDT 7206-20
2	8 ⇨ 4 CONV	CONVERTING PARALLEL WIDTH FROM 8 TO 4 TO INTERFACE WITH BSGC 2M, 8BIT ⇨ 4M, 4BIT	————
3	2/1 SEL (a)	BSGC-DIRECTION LOOPBACK SELECTOR	————
4	2/1 SEL (b)	HOME/MATE SYSTEM SELECTOR IN BSGC DIRECTION SELECTING ACT-BSGC	————
5	4 ⇨ 8 CONV	CONVERTING PARALLEL WIDTH FROM 4 TO 8 TO INTERFACE WITH BSGC 4M, 4BIT ⇨ 2M, 8BIT	
6	53/54 CONV	CONVERTING CELL VALID OCT LENGTH 530CT (CARP LSI SPECIFICATION) CONVERSION FOR 540CT IN SW	MB632607-G (CELL FIFO)

FIG. 758

SENDING	RECEIV-ING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	CONNECTING METHOD	REMARKS
IMX00A (A)	SWMDX (IMX03A)	OSICKX, Y	77.76MHz CLOCK	1	ECL BALANCED	12.86ns H L 1 0	50-CORE COAXIAL CABLE	
		OSICFX, Y	CELL FRAME SIGNAL	1		54 CLOCK H L 0 1		1 CELL SLOT LEADING BIT "H"
		OSICEX, Y	CELL ENABLE SIGNAL	1		54 CLOCK H L 0 1		L: INVALID CELL SLOT H: VALID CELL SLOT
		OSI00 ~7X, Y	CELL DATA OSID7: MSB OSID0: LSB	8		H L 1 0		
		JSOU	IMPLEMEN-TATION SIGNAL	1	TTL UNBALANCED	H L 1 0		L: IMPLEMENTED H: NON-IM-PLEMENTED
		OSIPTX, Y	CELL DATA PARITY	1	ECL BALANCED			

FIG. 759

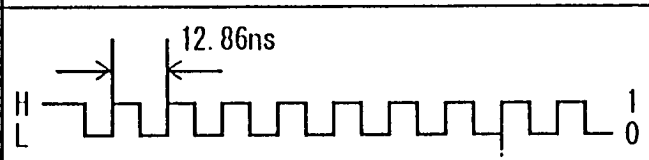
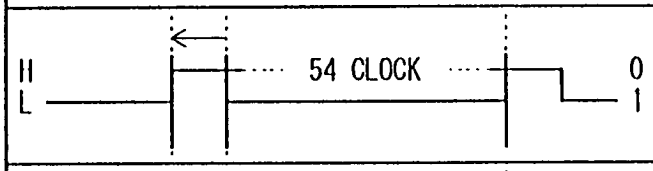
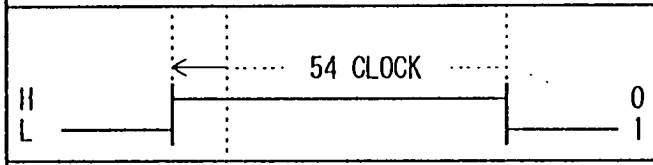
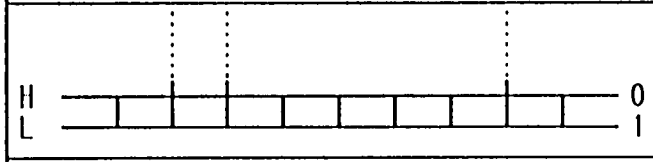
SENDING	RECEIVING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMI-SSION FORMAT	SIGNAL FORMAT	CONNECT-ING METHOD	REMARKS
SWMDX (HMX03A)	HMX00A(A)	ISICKX, Y	77.76MHz CLOCK	1	ECL BALANCED		50-CORE COAXIAL CABLE	
		ISICFX, Y	CELL FRAME SIGNAL	1				CELL SLOT LEADING BIT 'H'
		ISICEX, Y	CELL ENABLE SIGNAL	1				L: INVALID CELL SLOT H: VALID CELL SLOT
		ISI00-7X, Y	SELF DATA IMDX7 : MSB IMDX0 : LSB	8				
		ISIPTX, Y	CELL DATA PARITY	1				

FIG. 760

SENDING	RECEIVING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	CONNECTING METHOD	REMARKS
HSF04A	SWTIF (HNC00A)		LOWER ORDER μP FAULT SIGNAL	2	PSEUDO ECL BALANCED	H L 1 0	12-PAIR AC BUS CABLE	L : VALID H : INVALID
			LOWER ORDER DEVICE IMPLEMENTATION SIGNAL	2		H L 1 0		L : IMPLEMENTED H : NON-IMPLEMENTED

(a)

SENDING	RECEIVING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	CONNECTING METHOD	REMARKS
SWTIF (HNC00A)	HSF04A		SENDING/ RECEIVING CLOCK	2	PSEUDO ECL BALANCED	400ns H L 1 0	12-PAIR AC BUS CABLE	
			LU SYSTEM SELECTION SIGNAL	2		H L 1 0		L:0 SYSTEM SELECT INSTRUCTION H:1 SYSTEM SELECT INSTRUCTION
			LU SYSTEM SELECTION STROBE SIGNAL	2		H L 1 0		L: VALID H: INVALID

(b)

FIG. 761

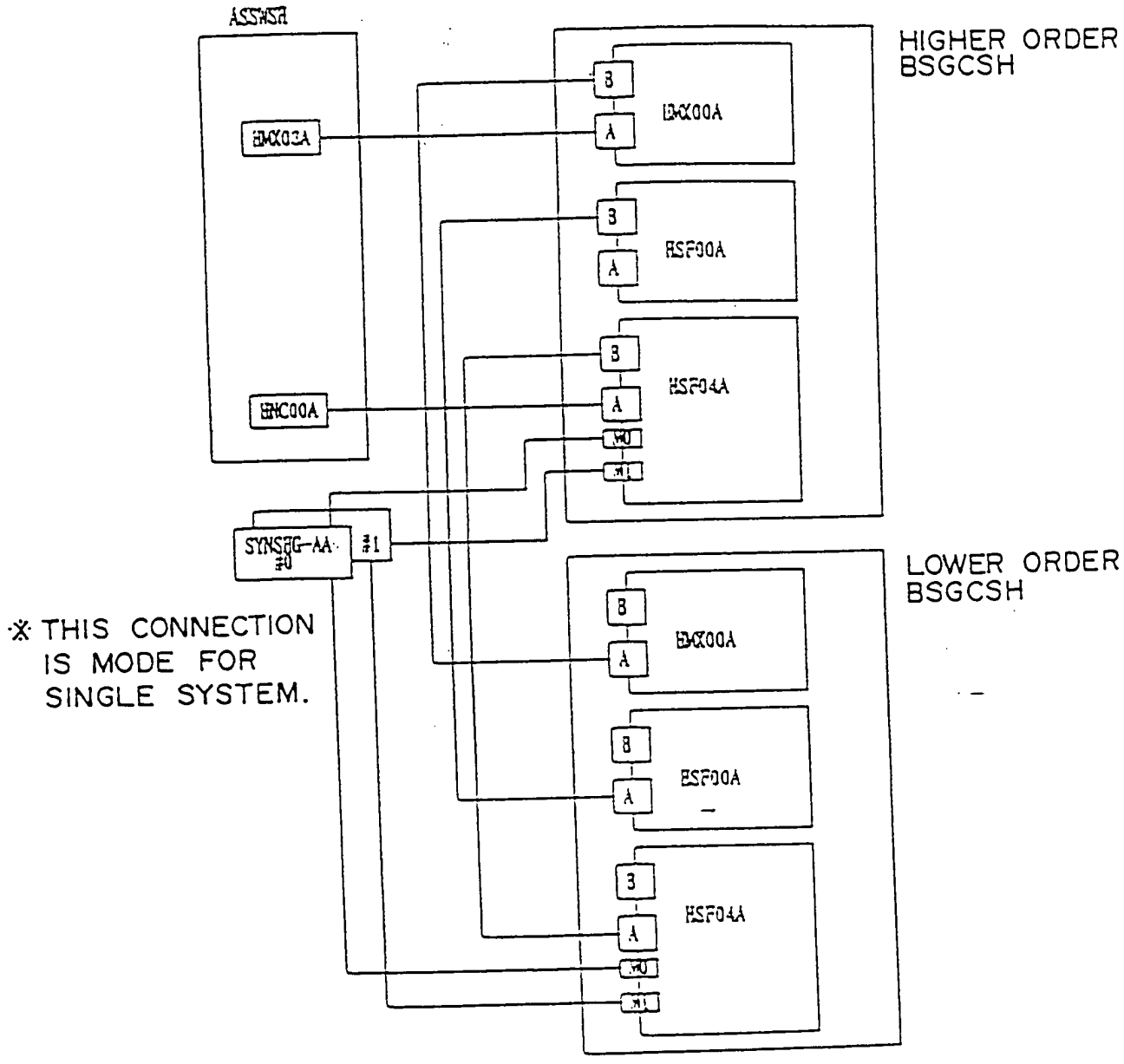

HIGHER ORDER BSGCSH
LOWER ORDER BSGCSH
B
A
#0
#1
※ THIS CONNECTION IS MODE FOR SINGLE SYSTEM.

FIG. 762

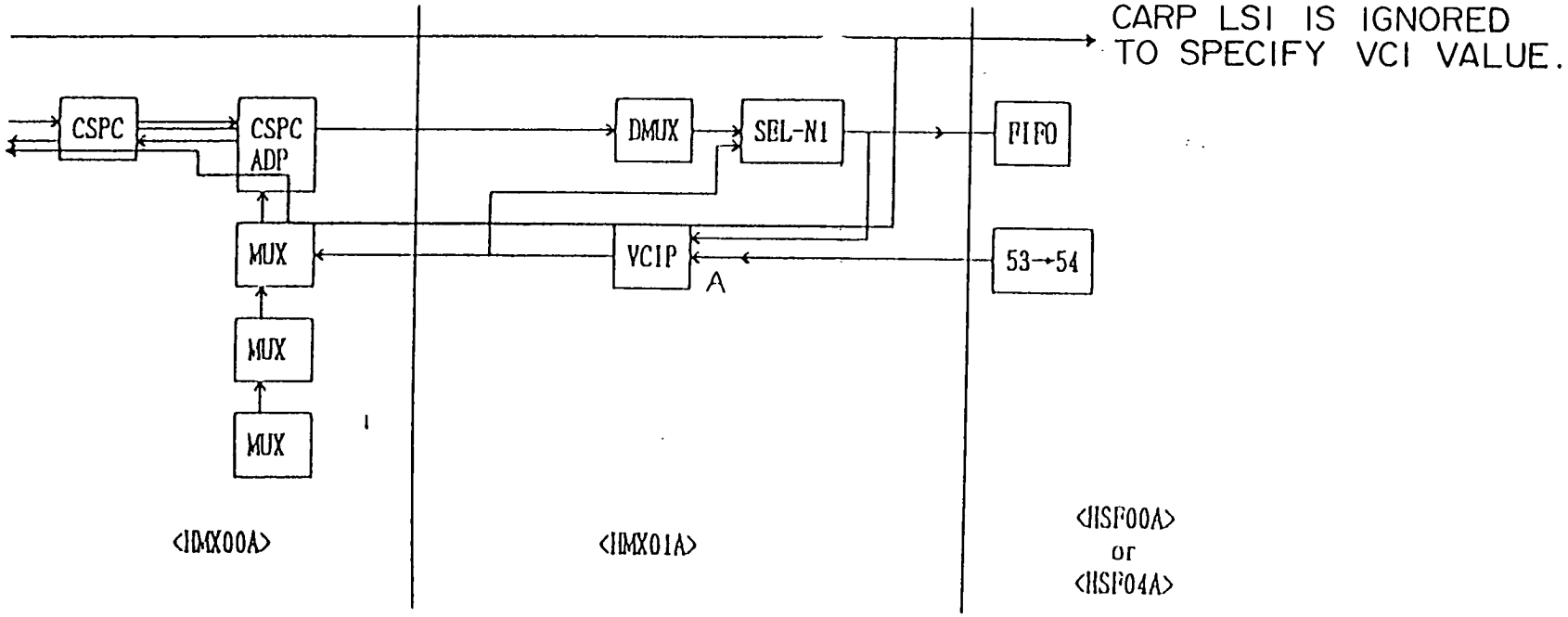

CARP LSI IS IGNORED
TO SPECIFY VCI VALUE.
CSPC
CSPC
ADP
DMUX
SEL-N1
FIFO
MUX
VCIP
A
53→54
MUX
MUX
<IDMX00A>
<IDMX01A>
<IISP00A>
or
<IISP04A>

FIG. 763

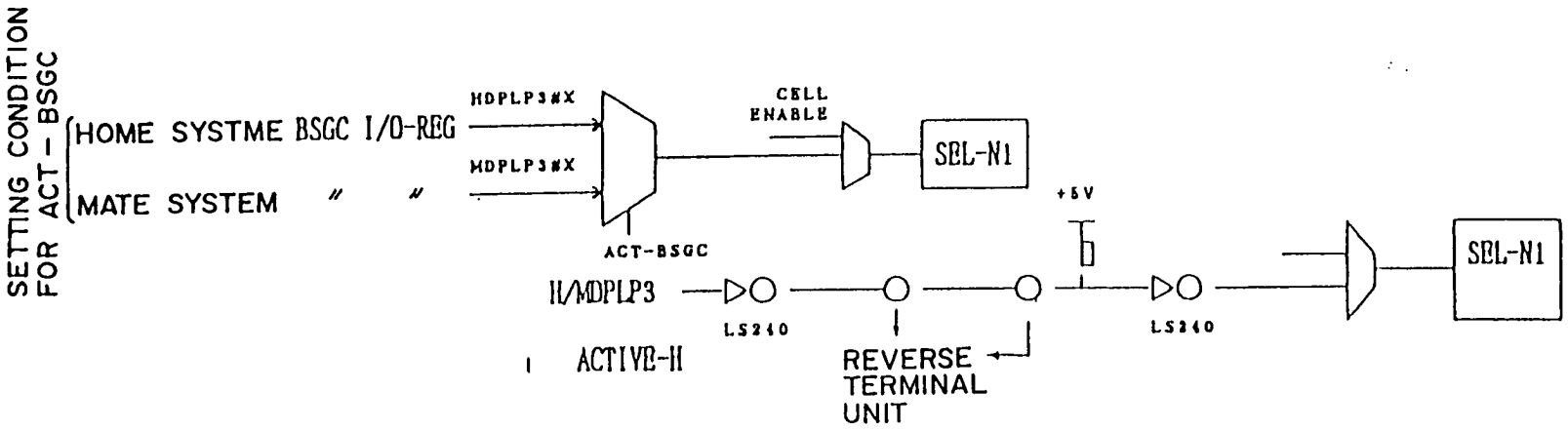

SETTING CONDITION FOR ACT-BSGC
HOME SYSTME BSGC I/O-REG
MATE SYSTEM " "
MDPLP3#X
MDPLP3#X
ACT-BSGC
CELL ENABLE
SEL-N1
+5V
H/MDPLP3
LS240
ACTIVE-H
REVERSE TERMINAL UNIT
LS240
SEL-N1

FIG. 764

0693260 "ETZ7260

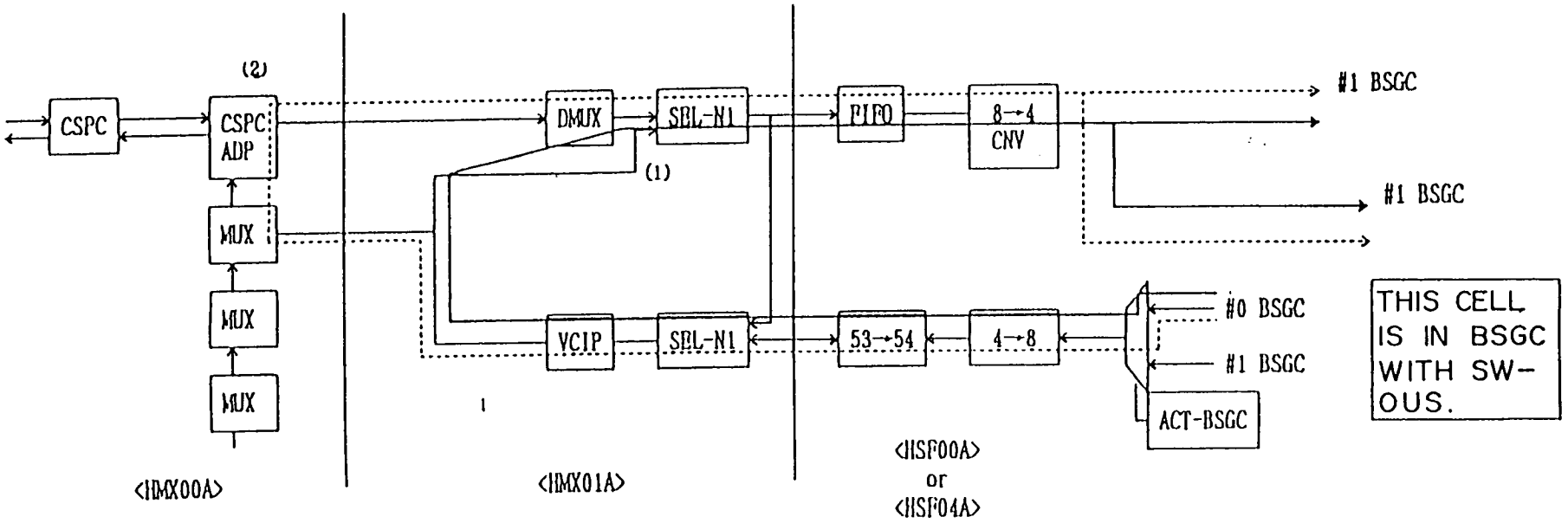


FIG. 765

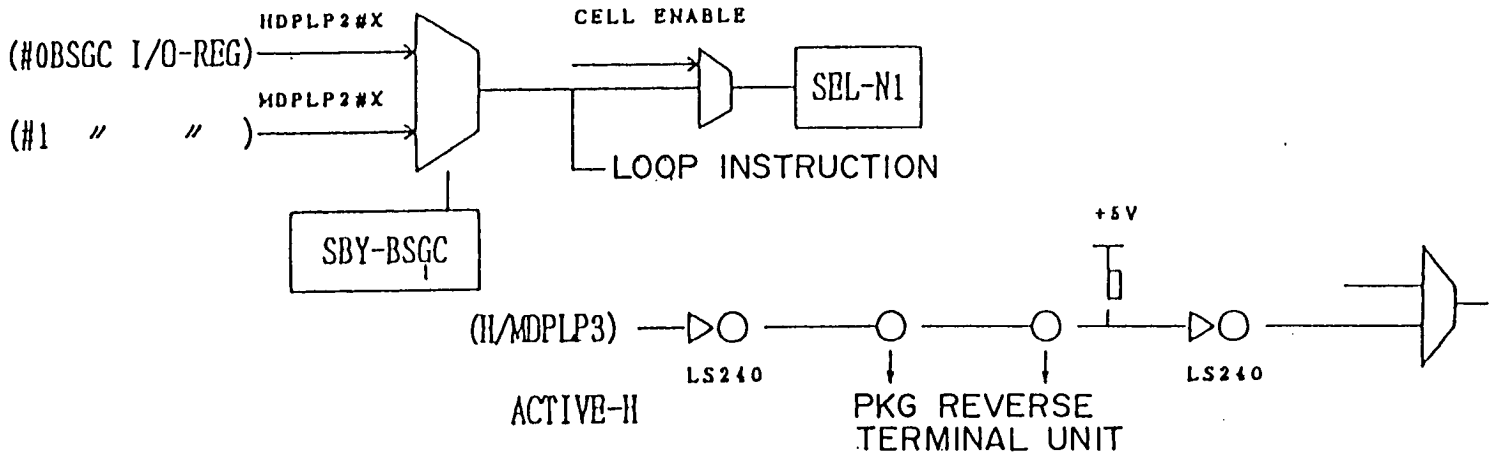

HDPLP2#X
(#0BSGC I/O-REG)
MDPLP2#X
(#1 〃 〃)
CELL ENABLE
SEL-N1
LOOP INSTRUCTION
SBY-BSGC
+5V
(H/MDPLP3)
LS240
LS240
ACTIVE-H
PKG REVERSE
TERMINAL UNIT

FIG. 766

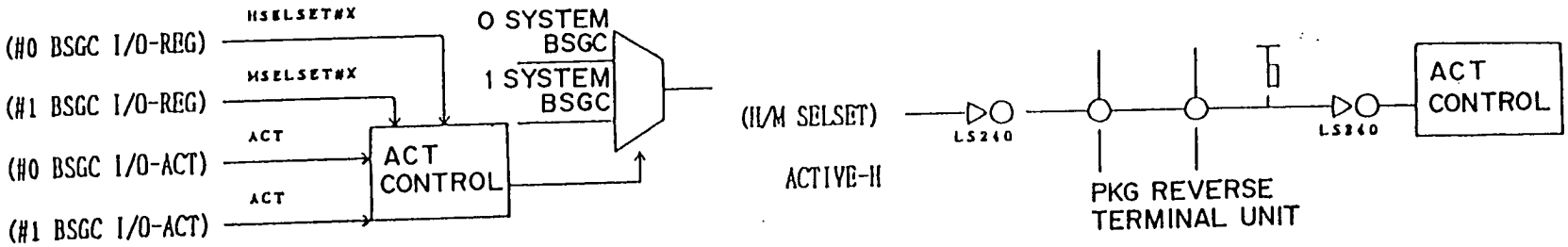

(#0 BSGC I/O-REG)
(#1 BSGC I/O-REG)
(#0 BSGC I/O-ACT)
(#1 BSGC I/O-ACT)
HSELSET#X
HSELSET#X
ACT
ACT
ACT CONTROL
0 SYSTEM BSGC
1 SYSTEM BSGC
(H/M SELSET)
ACTIVE-H
LS240
LS240
PKG REVERSE TERMINAL UNIT
ACT CONTROL

FIG. 767

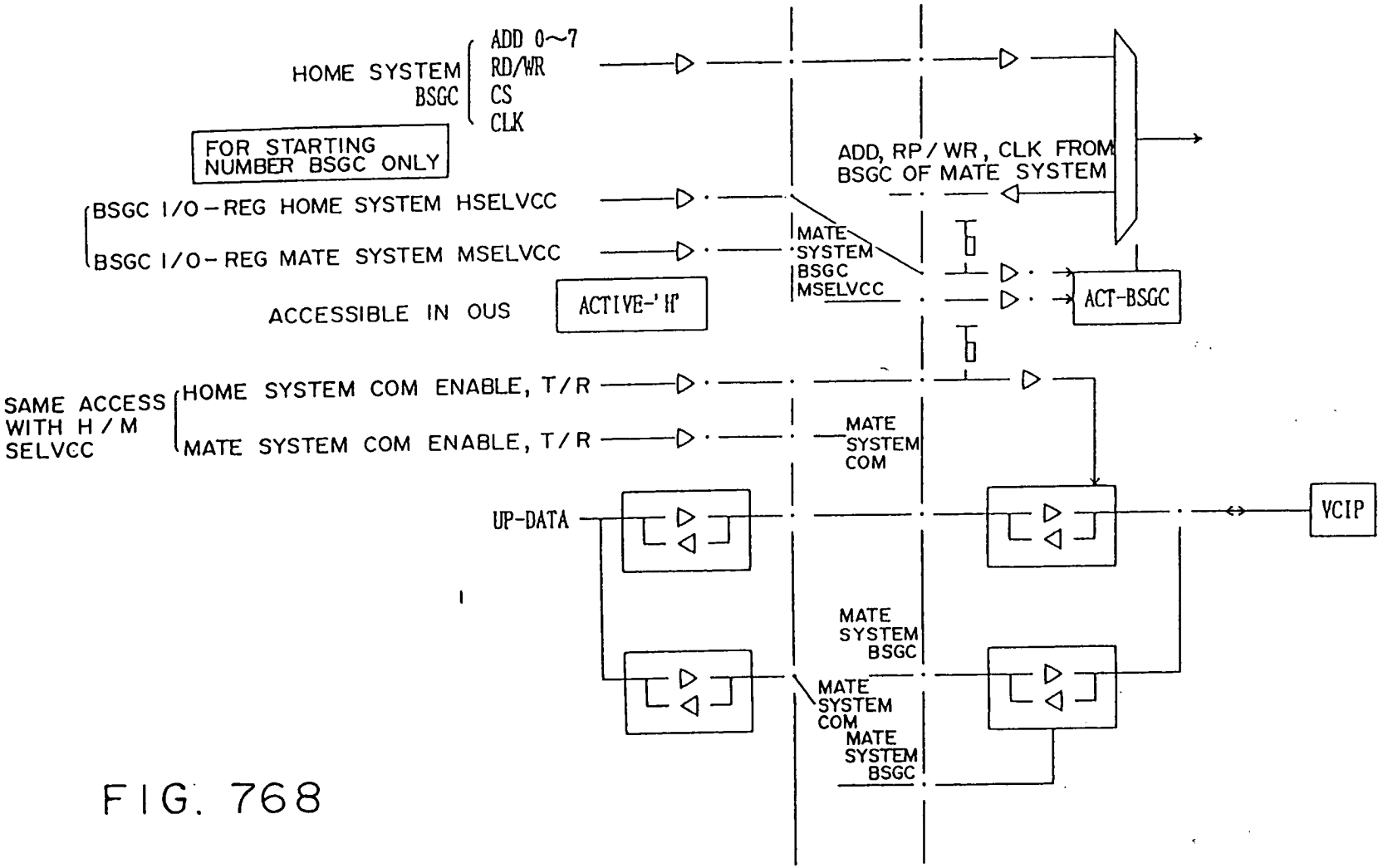

HOME SYSTEM BSGC
ADD 0~7
RD/WR
CS
CLK
FOR STARTING NUMBER BSGC ONLY
ADD, RP/WR, CLK FROM BSGC OF MATE SYSTEM
BSGC I/O-REG HOME SYSTEM HSELVCC
BSGC I/O-REG MATE SYSTEM MSELVCC
MATE SYSTEM BSGC MSELVCC
ACCESSIBLE IN OUS
ACTIVE-'H'
ACT-BSGC
SAME ACCESS WITH H/M SELVCC
HOME SYSTEM COM ENABLE, T/R
MATE SYSTEM COM ENABLE, T/R
MATE SYSTEM COM
UP-DATA
VCIP
MATE SYSTEM BSGC
MATE SYSTEM COM
MATE SYSTEM BSGC

FIG. 768

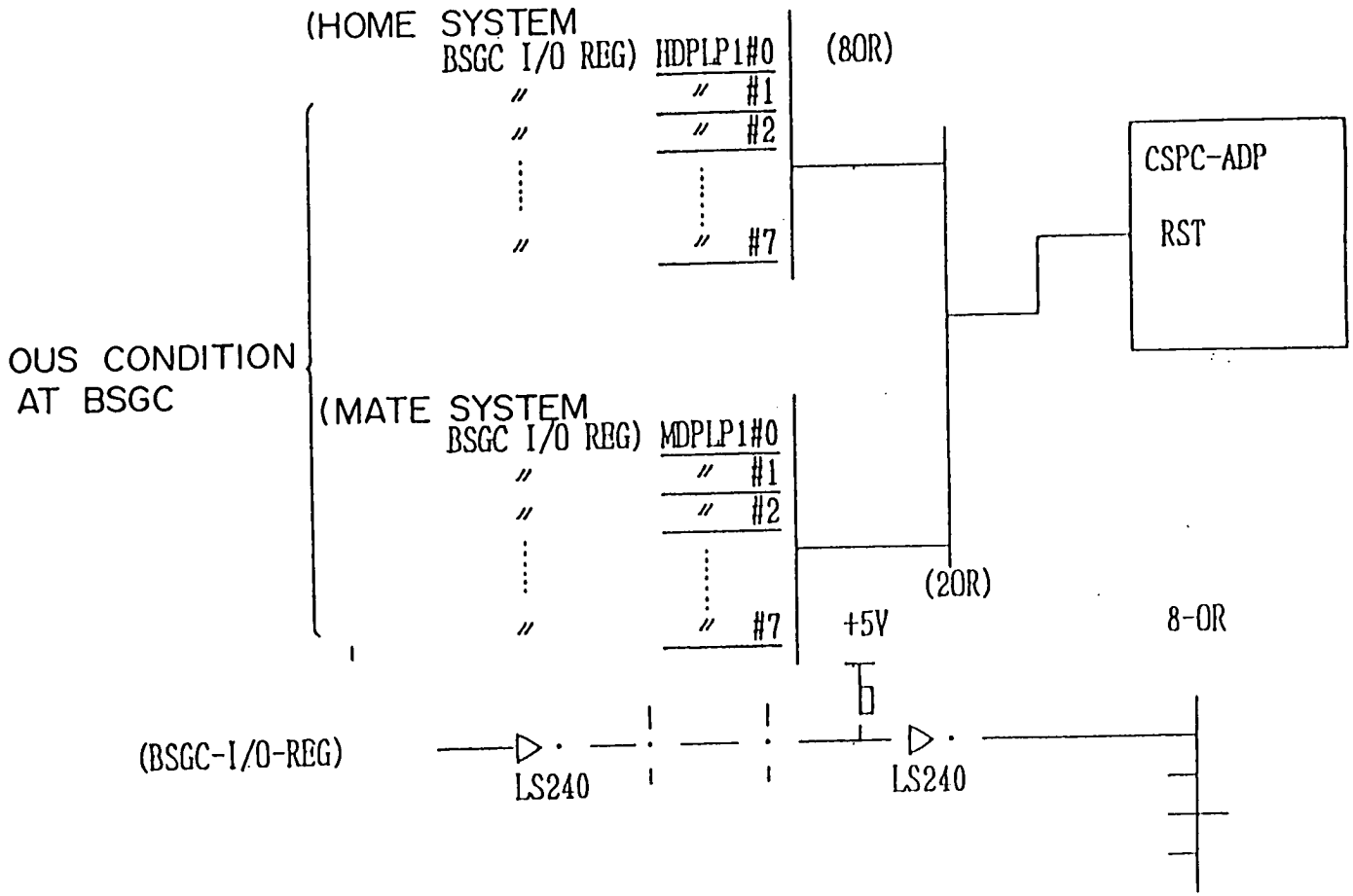

(HOME SYSTEM
BSGC I/O REG)
HDPLP1#0
〃 #1
〃 #2
〃 #7
(8OR)
CSPC-ADP
RST
OUS CONDITION
AT BSGC
(MATE SYSTEM
BSGC I/O REG)
MDPLP1#0
〃 #1
〃 #2
〃 #7
(2OR)
+5V
8-OR
(BSGC-I/O-REG)
LS240
LS240

FIG. 769

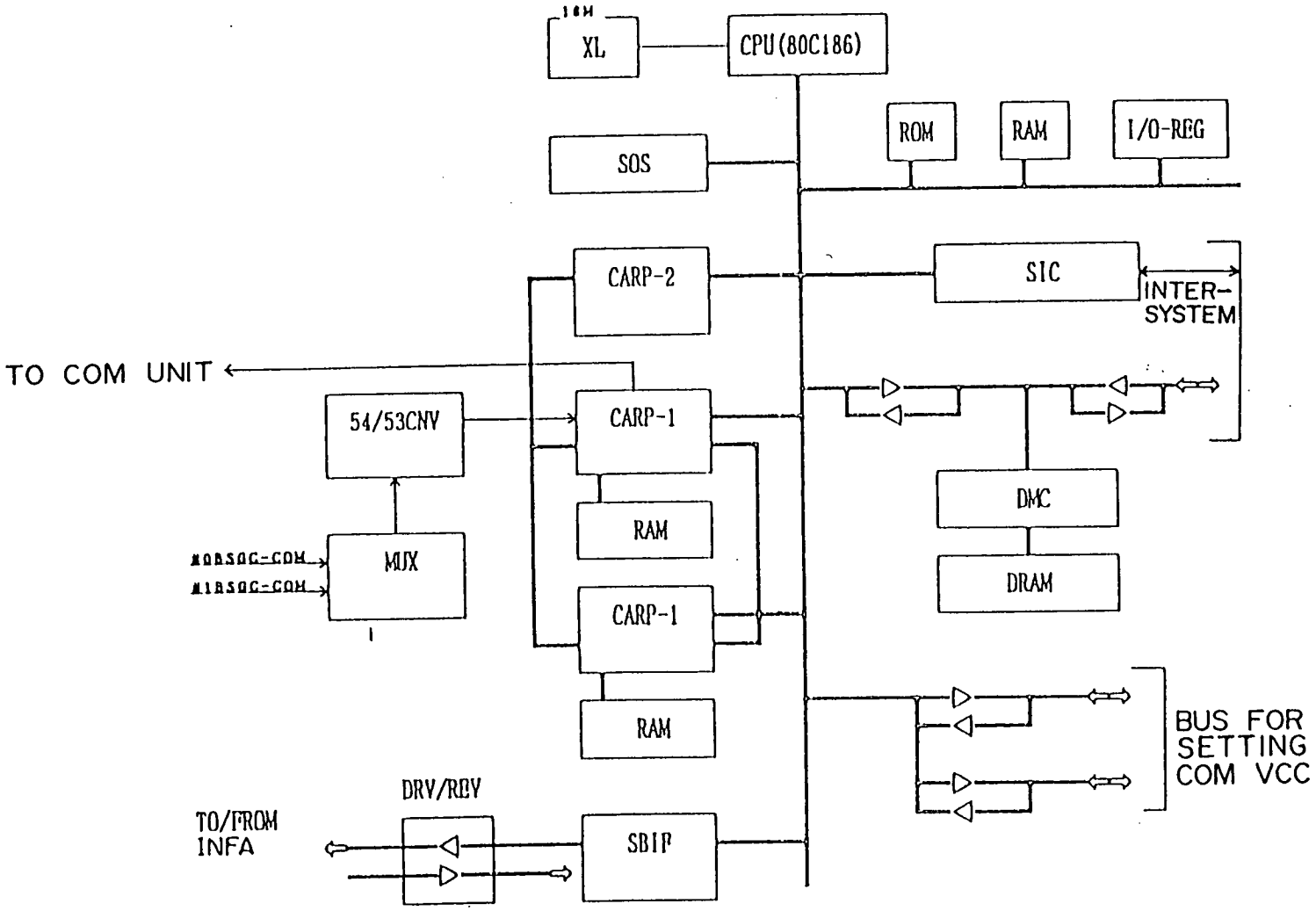

16M
XL
CPU(80C186)
ROM
RAM
I/O-REG
SOS
CARP-2
SIC
INTER-SYSTEM
TO COM UNIT
54/53CNV
CARP-1
RAM
DMC
DRAM
MUX
CARP-1
RAM
BUS FOR SETTING COM VCC
DRV/RCV
TO/FROM INFA
SBIP

FIG. 770

FUNCTION BLOCK NAME	OUTLINE OF FUNCTION	MAIN LSI
MPU	MAIN CONTROL PROCESSOR 8MHz OPERATION. INF INTERFACE/SUBCRIBER, INTER-DEVICE LAP CONTROL	INTEL80C186
ROM	64 KBYTE X 4 PHASE BAND CONFIGURATION	HN27C4096G-10
RAM	SRAM - 32 KBYTE	MB84256A
	DRAM - 896 KBYTE	MB81256 X 4 81C4256 X 8
DMC	DETECTING DRAM CONTROL, MEMORY WRITE PROTECT, AND MATE SYSTEM CLOCK DISCONNECTION. DETECTING MATE SYSTEM POWER SOURCE DISCONNECTION	MB670639
CARP-1	MULTIPLEXING LSI CAPABLE OF SIMULTANEOUSLY OPERATING UP TO 16 CH CELL DISASSEMBLY AND ASSEMBLY BY SUPPORTING TYPSE-3 OF ATM LAYER OF B-ISDN PROTOCOL AND CELL DISASSEMBLY/ASSEMBLY SUBLAYER (SAR)	MBCG31134-602
CARP-2	CARP-2 IS CONNECTED TO CARP-1 AND TRANSFERS TRANSMISSION DATA IN MEMORY TO SW IN DMA OPERATION AS TRANSMISSION PROCESS	MB630615
SIC	FOR SYSTEM CROSS-CONNECTION, PARALLEL DATA FROM CPU IS CONVERTED INTO SERIAL DATA FOR COMMUNICATIONS	MB674602
SOS	LSI FOR PERFORMING 80186 CPU REALTIME COMPASS III PROCESS AT HIGH SPEED	MB602773
SBIF	DATA TRANSFER PROCESS BETWEEN INF INTERFACE AND CPU BUS. COMMAND ACTIVATION IS REALIZED AND REPORTED THROUGH INTERRUPTION TO CPU. DATA TRANSMISSION DMA IS SPECIFIED FOR REG IN SBIF	MB651623
DRV/REV	ELECTRICAL CHANGE IS MADE IN INF INTERFACE (V.11)	MB412/MB413

FIG. 771

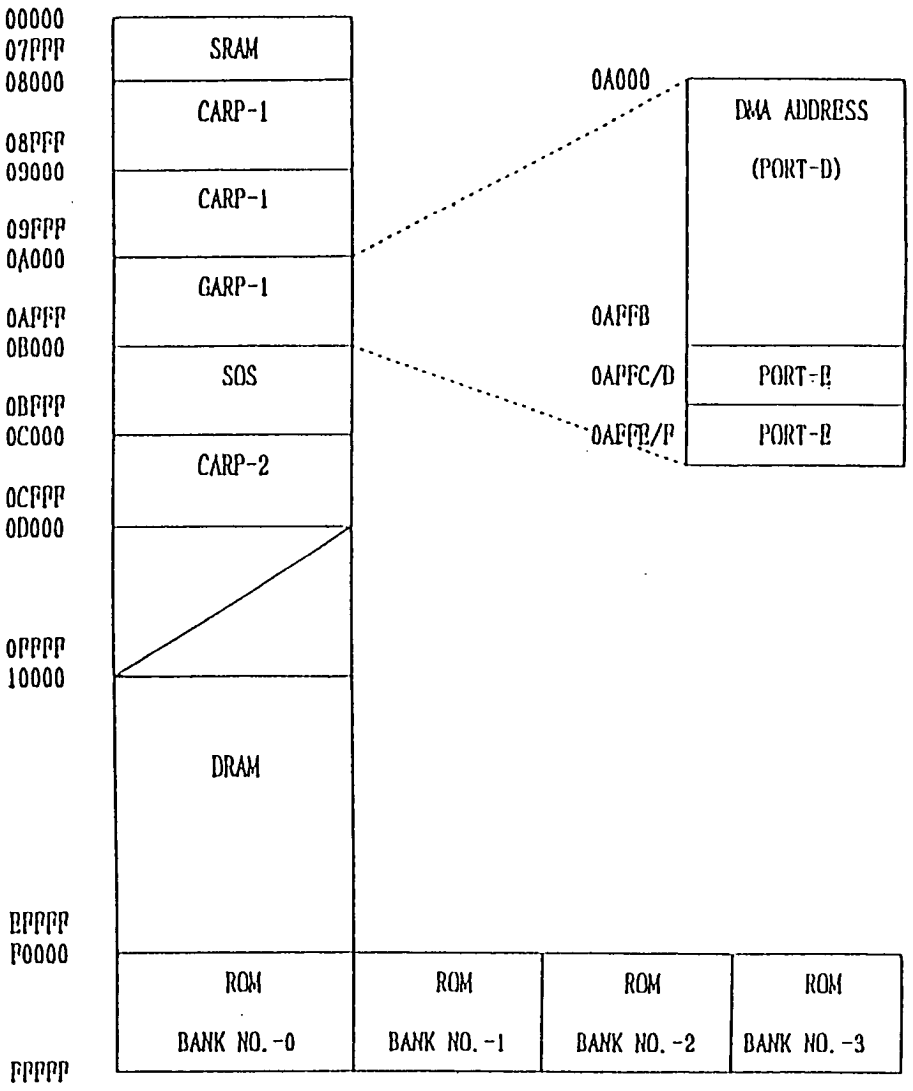

00000
07FFF
08000
08FFF
09000
09FFF
0A000
0AFFF
0B000
0BFFF
0C000
0CFFF
0D000
0FFFF
10000
FFFFF
F0000
FFFFF
SRAM
CARP-1
CARP-1
GARP-1
SOS
CARP-2
DRAM
ROM
BANK NO.-0
ROM
BANK NO.-1
ROM
BANK NO.-2
ROM
BANK NO.-3
0A000
0AFFB
0AFFC/D
0AFFE/F
DMA ADDRESS
(PORT-D)
PORT-C
PORT-E

FIG. 772

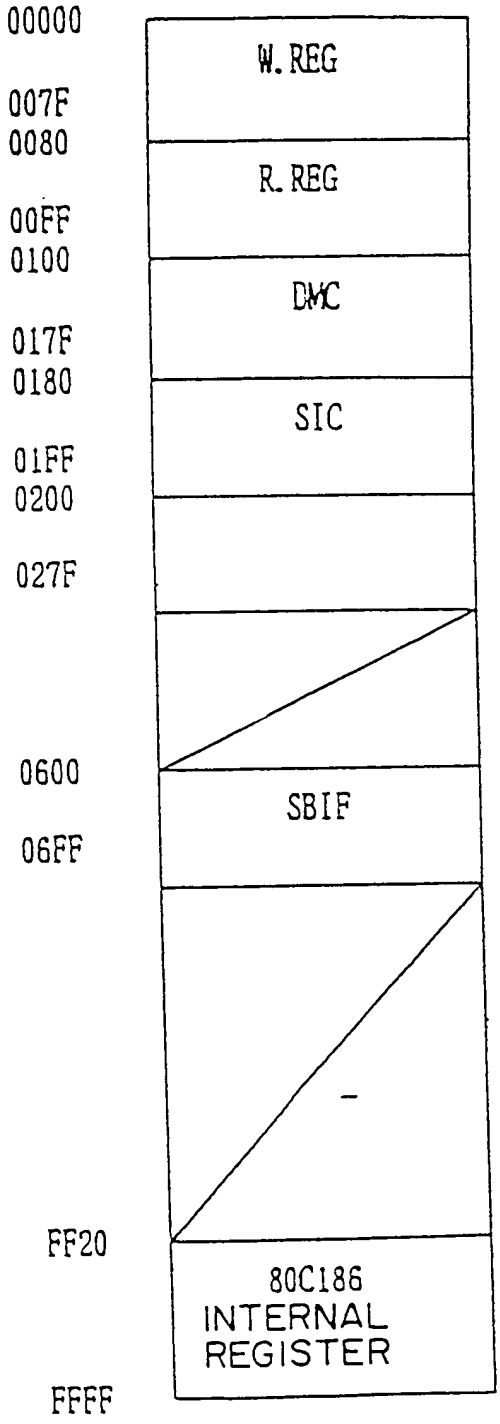
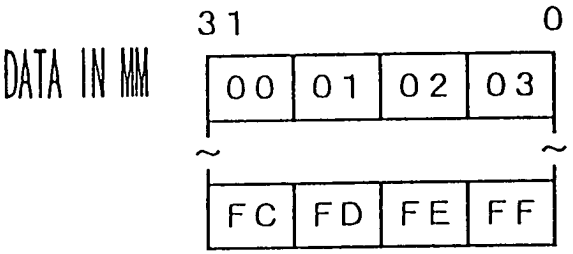

00000
W. REG
007F
0080
R. REG
00FF
0100
DMC
017F
0180
SIC
01FF
0200
027F
0600
SBIF
06FF
FF20
80C186
INTERNAL
REGISTER
FFFF

FIG. 773

No.	INSTRUCTION TYPE	IN/OUT	READ/WRITE	REMARKS
1	COMMAND ACTIVATION	OUT	WRITE	
2	RETRY INSTRUCTION	OUT	WRITE	
3	MSCN READ	IN	READ	
4	TEST LOOPBACK DATA WRITE	OUT	WRITE	
5	TEST LOOPBACK DATA READ	IN	READ	

FIG. 774

PATTERN1 CONSECUTIVE DATA PATTERN WITHOUT USING CD



PATTERN2 CONSECUTIVE DATA PATTERN USING CD

FIG. 775

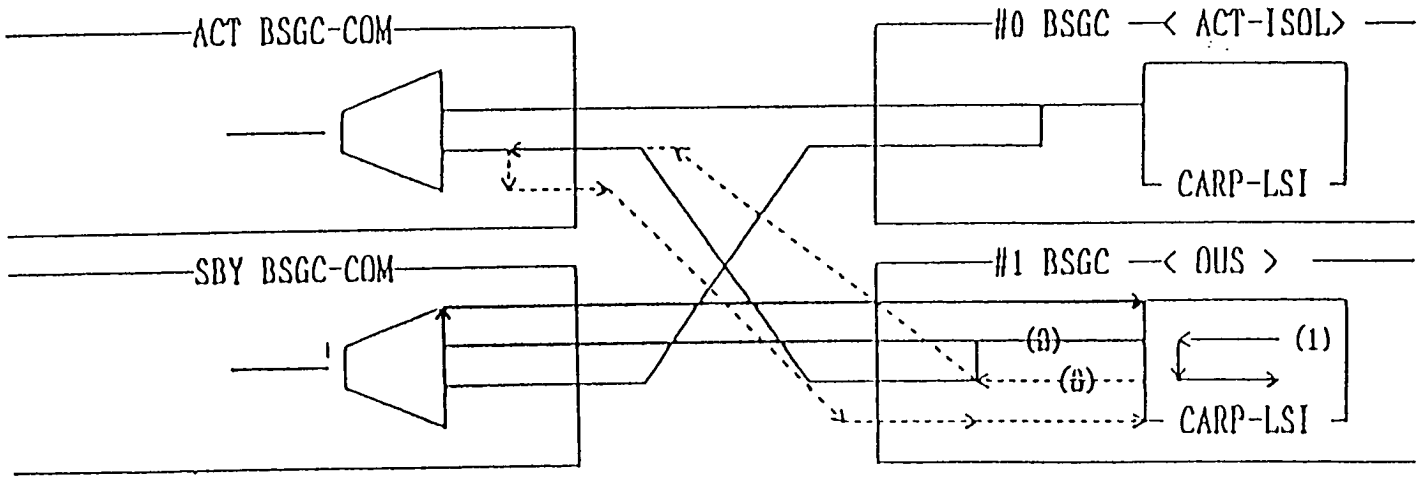
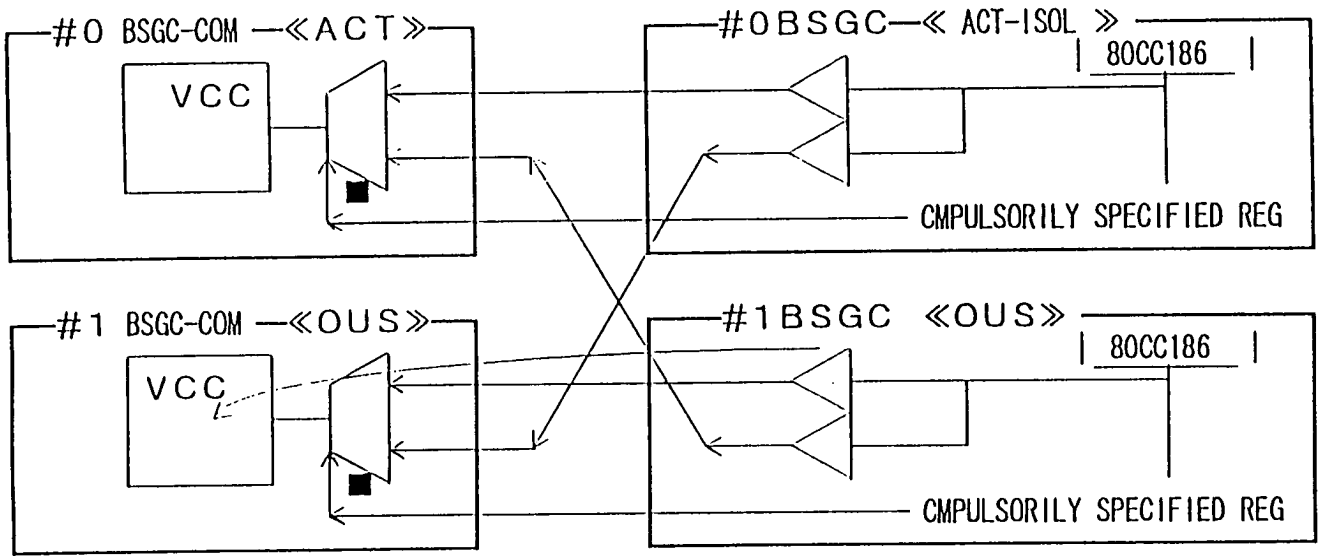

ACT BSGC-COM
SBY BSGC-COM
#0 BSGC —< ACT-ISOL>
CARP-LSI
#1 BSGC —< OUS >
(0)
(0)
(1)
CARP-LSI

FIG. 776



■ ····· INDICATES 2-1 SEL SELECT LOGIC CIRCUIT. NORMALLY ACT-BSGE IS SELECTED.

FIG. 777

ACT SYSTEM TEST	SBY SYSTEM TEST	OUS STATE
SINCE COMMUNICATIONS IS ESTABLISHED BY SIMPLE LAP PROTOCOL, NO TEST IS MADE	SINCE SIMPLE LAP PROTOCOL COMMUNICATIONS ARE MADE FROM BSGC OF ACT SYSTEM TO SW OF SBY SYSTEM, NO TEST IS MADE AS IN ACT SYSTEM	CONTINUITY TEST IS MADE CELL-BY-CELL LOOPBACK IS MADE BY BSGC-COM CELL-BY-CELL LOOP TRIGGER IS 0-BIT IN ATM HEADER

FIG. 778

EP 0 762 696 A2

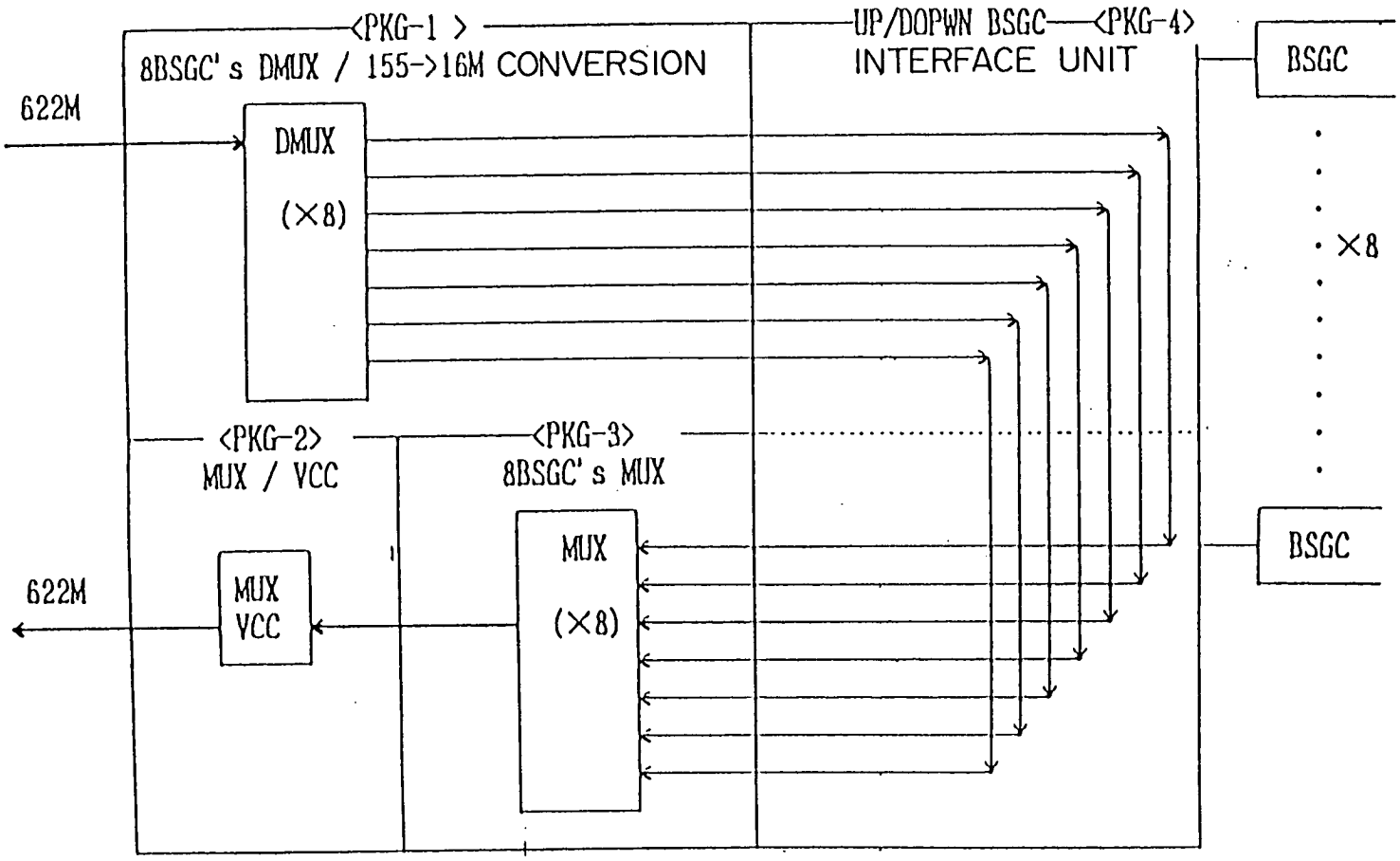

<PKG-1 >
8BSGC's DMUX / 155->16M CONVERSION
UP/DOPWN BSGC
<PKG-4>
INTERFACE UNIT
BSGC
622M
DMUX
(×8)
×8
<PKG-2>
MUX / VCC
<PKG-3>
8BSGC's MUX
MUX
(×8)
BSGC
622M
MUX
VCC

FIG. 779

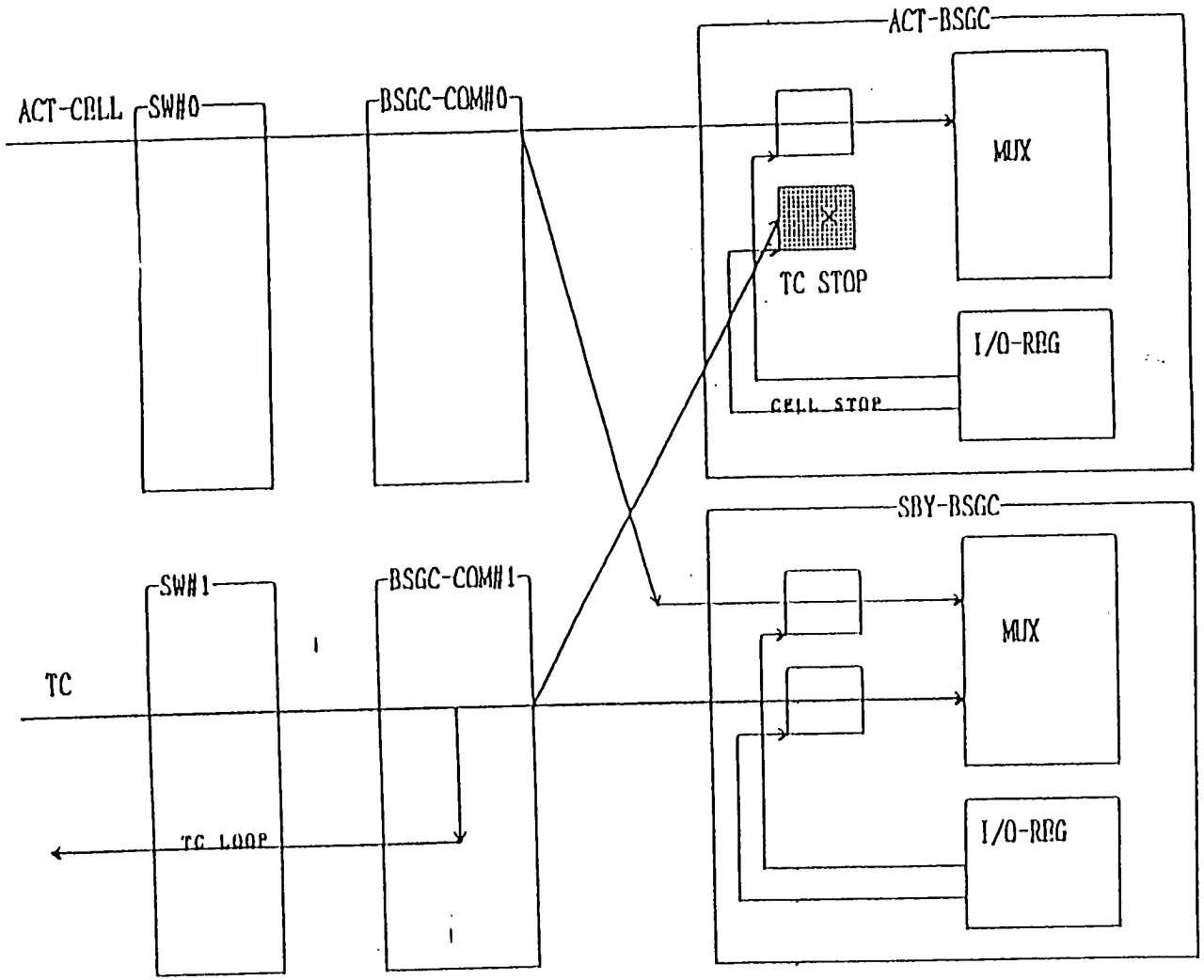

ACT-BSGC
ACT-CELL
SW#0
BSGC-COM#0
MUX
TC STOP
I/O-REG
CELL STOP
SBY-BSGC
SW#1
BSGC-COM#1
MUX
TC
I/O-REG
TC LOOP

FIG. 780

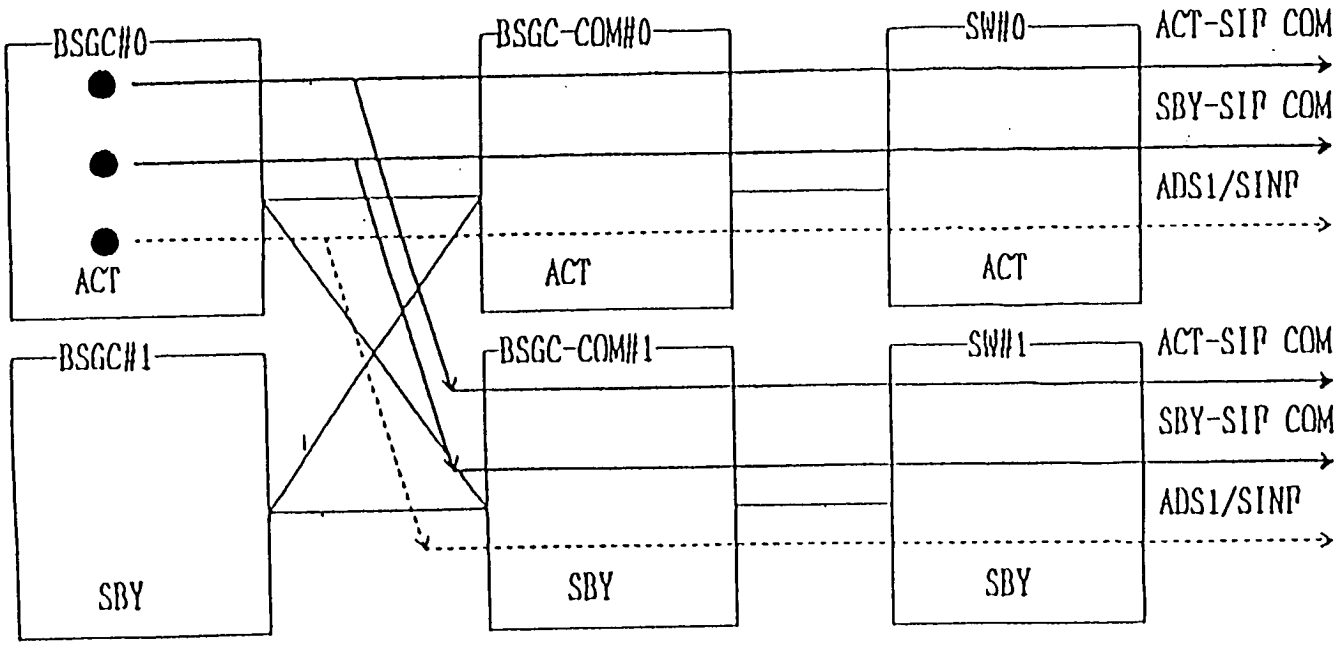

BSGC#0
ACT
BSGC#1
SBY
BSGC-COM#0
ACT
BSGC-COM#1
SBY
SW#0
ACT
SW#1
SBY
ACT-SIP COM
SBY-SIP COM
ADS1/SINP
ACT-SIP COM
SBY-SIP COM
ADS1/SINP

FIG. 781

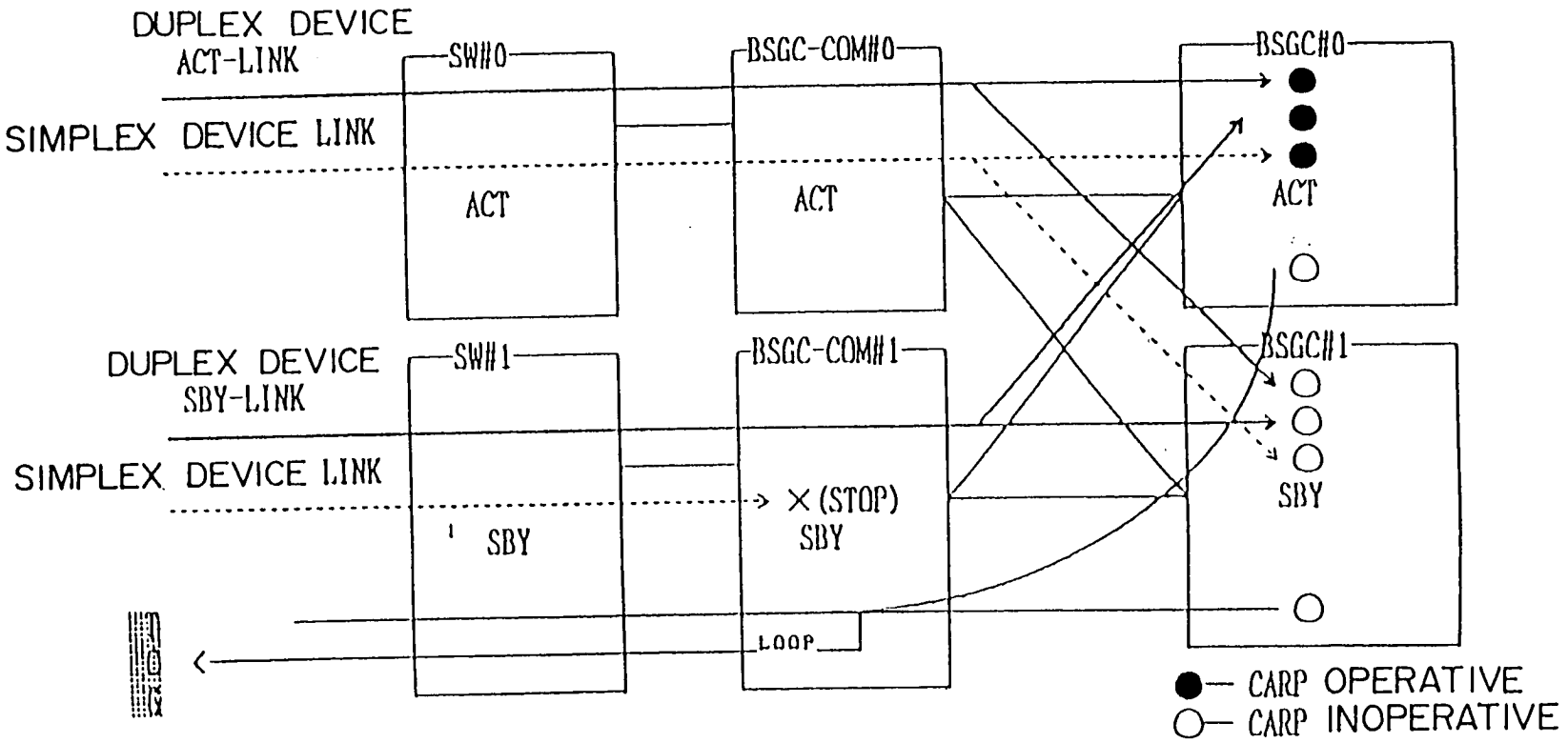

DUPLEX DEVICE
ACT-LINK
SIMPLEX DEVICE LINK
SW#0
ACT
BSGC-COM#0
ACT
BSGC#0
ACT
DUPLEX DEVICE
SBY-LINK
SIMPLEX DEVICE LINK
SW#1
SBY
BSGC-COM#1
× (STOP)
SBY
LOOP
BSGC#1
SBY
● CARP OPERATIVE
○ CARP INOPERATIVE

FIG. 782

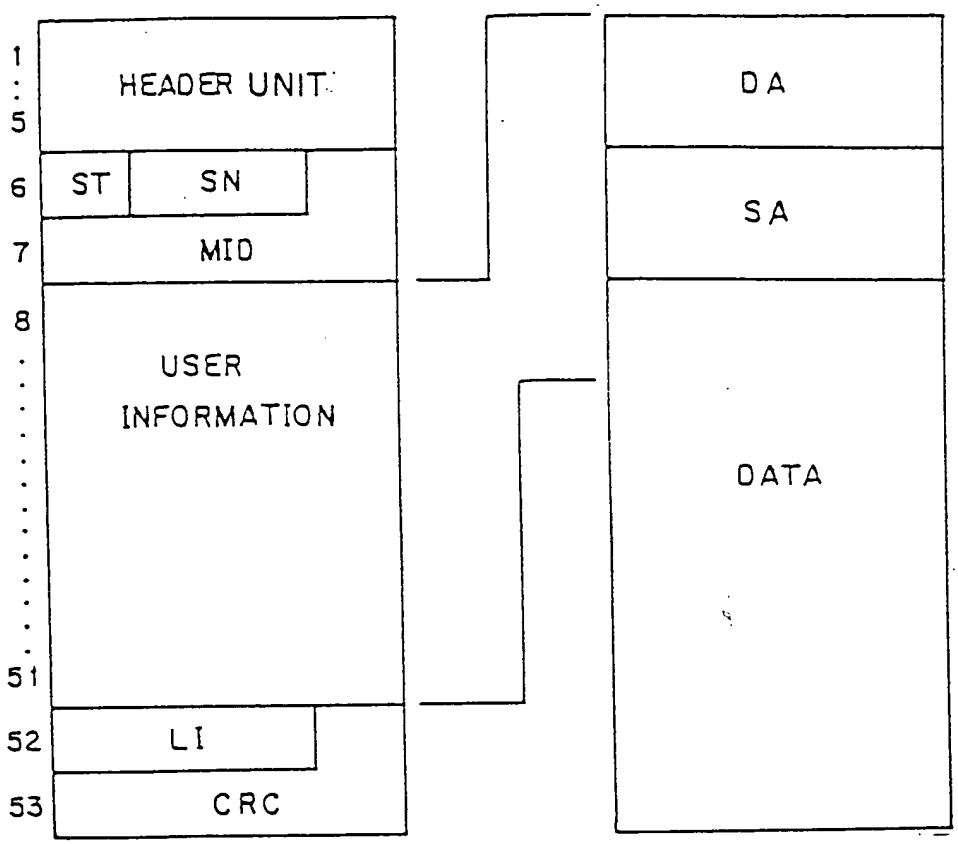

1
:
5
HEADER UNIT
6
ST
SN
7
MID
8
USER
INFORMATION
51
52
LI
53
CRC
DA
SA
DATA
L2 PROTOCOL DATA UNIT
L3 PROTOCOL DATA UNIT
ST : Segment Type (BOM, SSM, COM, EOM)
SN : Sequence Number
MID: Message IDentifier
DA: Destination Address
SA: Source Address

FIG. 783

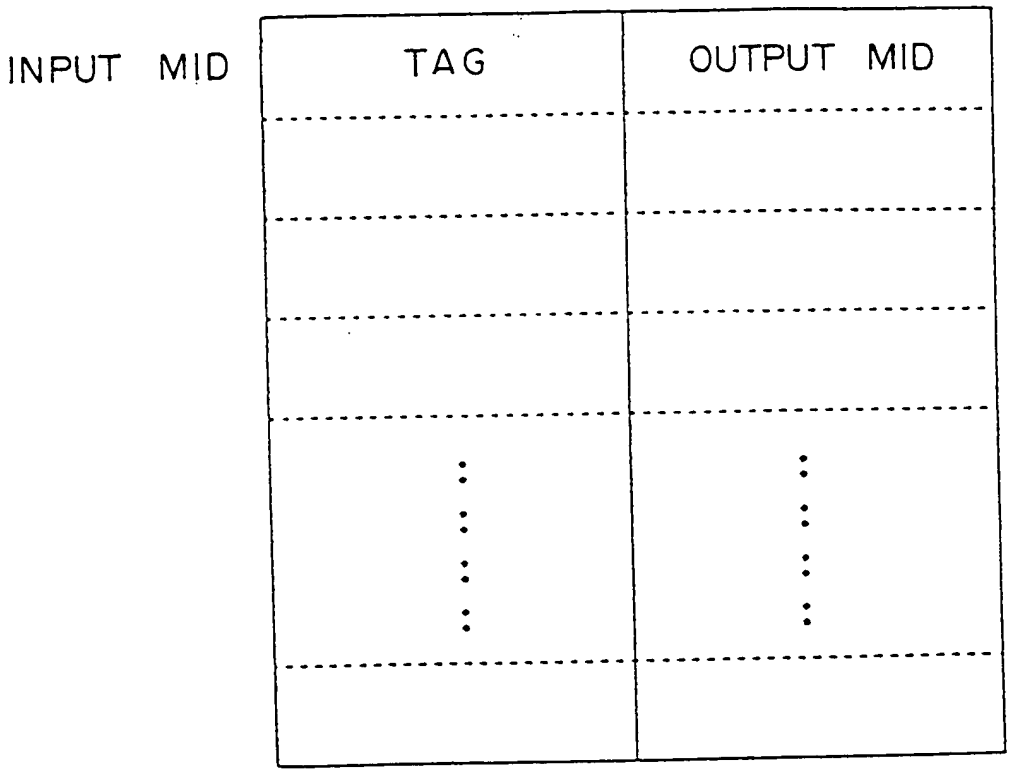


FIG. 784

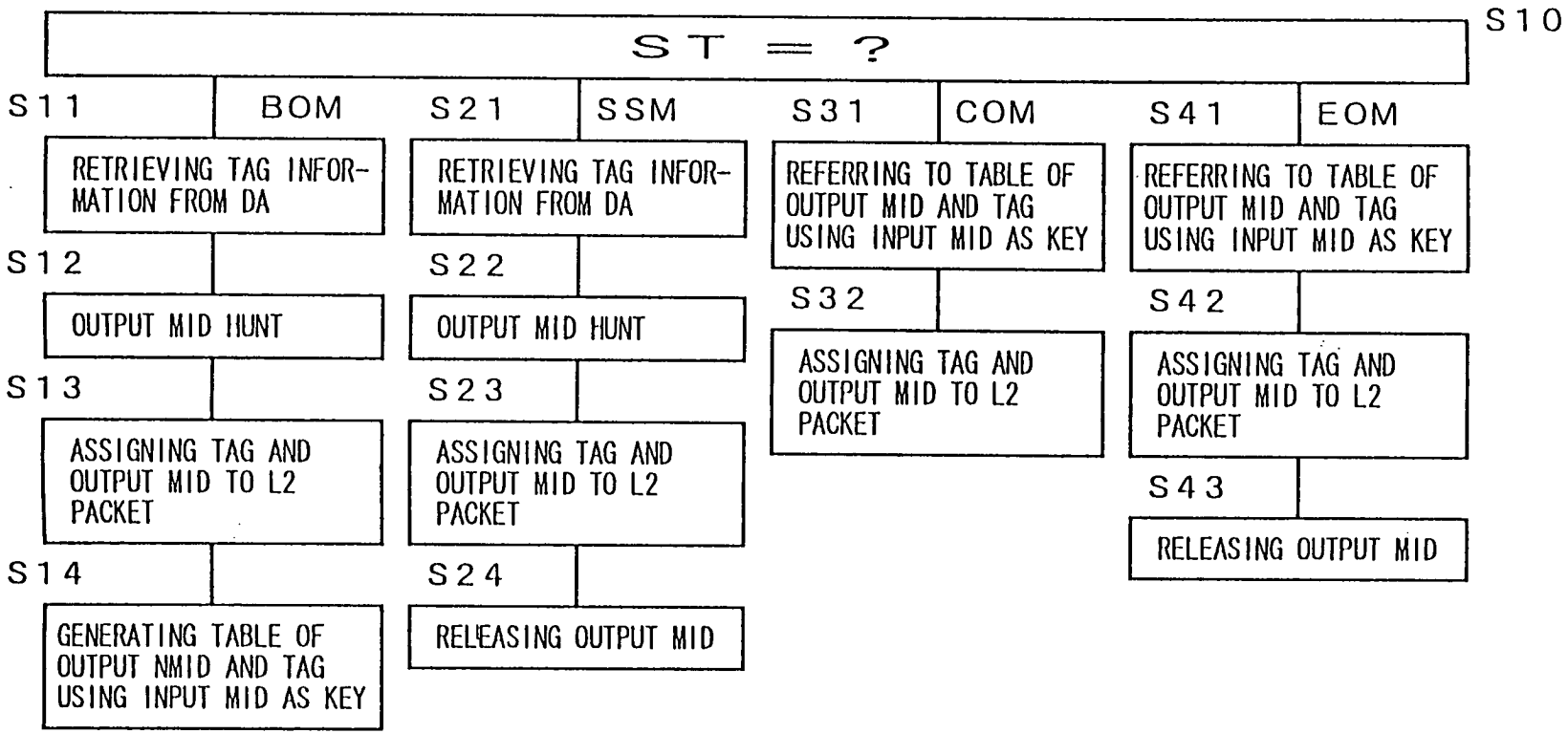

S T = ?
S10
S11
BOM
RETRIEVING TAG INFOR-MATION FROM DA
S12
OUTPUT MID HUNT
S13
ASSIGNING TAG AND OUTPUT MID TO L2 PACKET
S14
GENERATING TABLE OF OUTPUT NMID AND TAG USING INPUT MID AS KEY
S21
SSM
RETRIEVING TAG INFOR-MATION FROM DA
S22
OUTPUT MID HUNT
S23
ASSIGNING TAG AND OUTPUT MID TO L2 PACKET
S24
RELEASING OUTPUT MID
S31
COM
REFERRING TO TABLE OF OUTPUT MID AND TAG USING INPUT MID AS KEY
S32
ASSIGNING TAG AND OUTPUT MID TO L2 PACKET
S41
EOM
REFERRING TO TABLE OF OUTPUT MID AND TAG USING INPUT MID AS KEY
S42
ASSIGNING TAG AND OUTPUT MID TO L2 PACKET
S43
RELEASING OUTPUT MID

FIG. 785

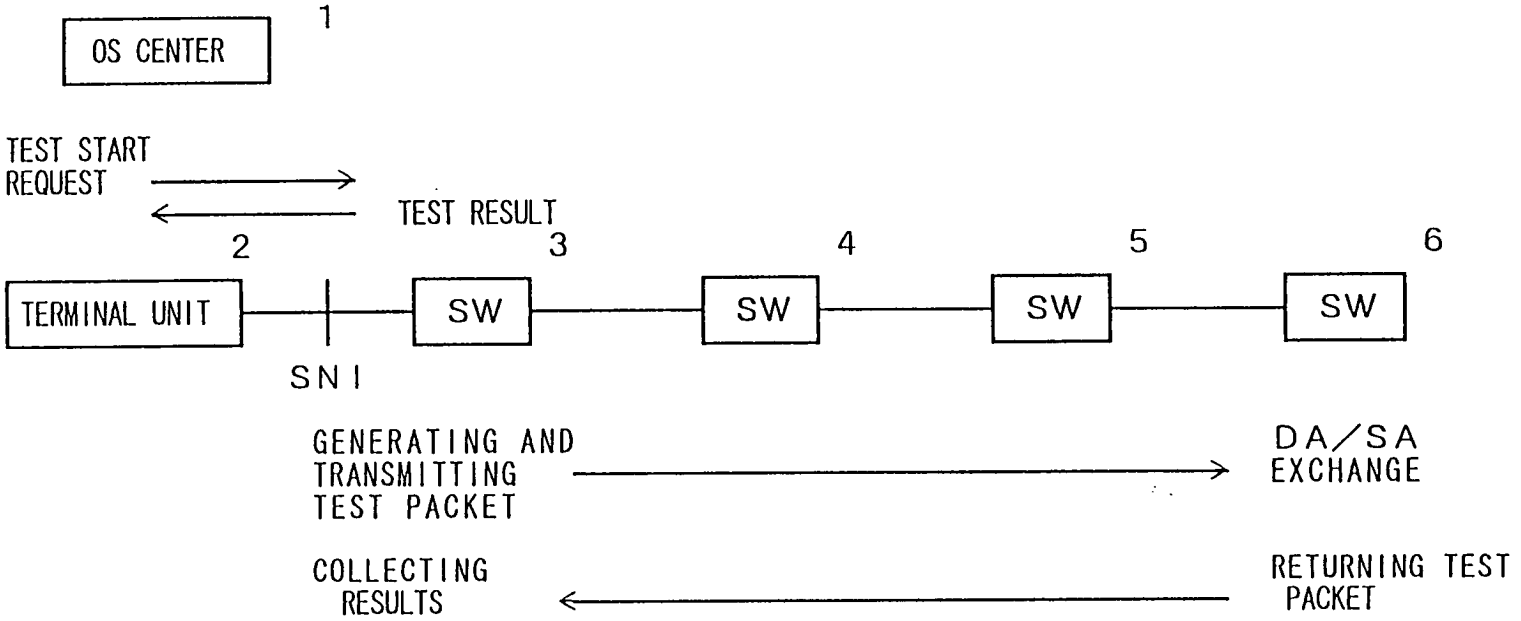

OS CENTER
1
TEST START REQUEST
TEST RESULT
2
3
4
5
6
TERMINAL UNIT
SW
SW
SW
SW
SNI
GENERATING AND TRANSMITTING TEST PACKET
DA/SA EXCHANGE
COLLECTING RESULTS
RETURNING TEST PACKET

FIG. 786

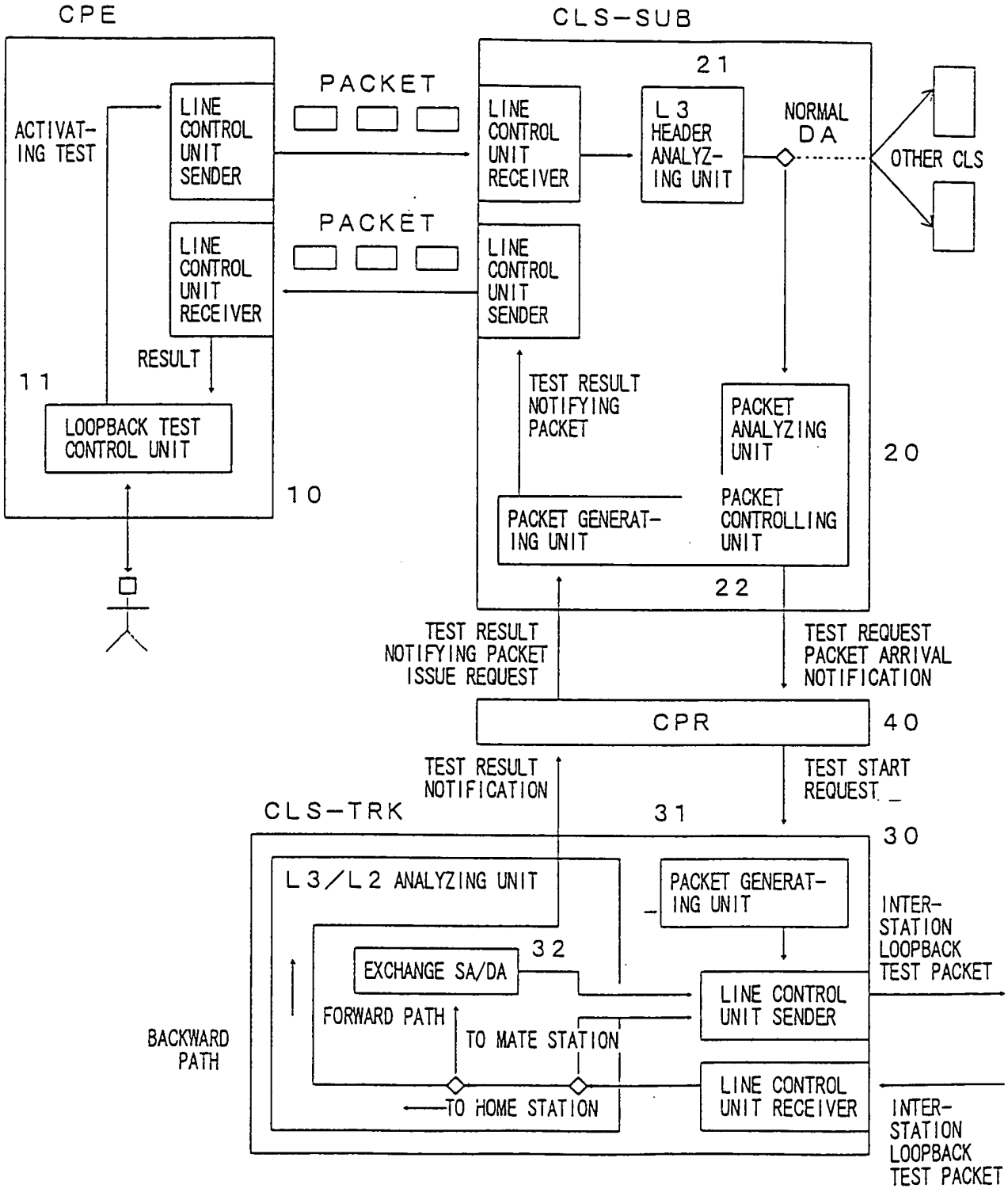

CPE
CLS-SUB
21
PACKET
ACTIVAT-
ING TEST
LINE
CONTROL
UNIT
SENDER
LINE
CONTROL
UNIT
RECEIVER
L3
HEADER
ANALYZ-
ING UNIT
NORMAL
DA
OTHER CLS
PACKET
LINE
CONTROL
UNIT
RECEIVER
LINE
CONTROL
UNIT
SENDER
RESULT
11
TEST RESULT
NOTIFYING
PACKET
PACKET
ANALYZING
UNIT
20
LOOPBACK TEST
CONTROL UNIT
10
PACKET GENERAT-
ING UNIT
PACKET
CONTROLLING
UNIT
22
TEST RESULT
NOTIFYING PACKET
ISSUE REQUEST
TEST REQUEST
PACKET ARRIVAL
NOTIFICATION
CPR
40
TEST RESULT
NOTIFICATION
TEST START
REQUEST
CLS-TRK
31
30
L3/L2 ANALYZING UNIT
PACKET GENERAT-
ING UNIT
INTER-
STATION
LOOPBACK
TEST PACKET
32
EXCHANGE SA/DA
LINE CONTROL
UNIT SENDER
FORWARD PATH
TO MATE STATION
BACKWARD
PATH
LINE CONTROL
UNIT RECEIVER
TO HOME STATION
INTER-
STATION
LOOPBACK
TEST PACKET

FIG. 787

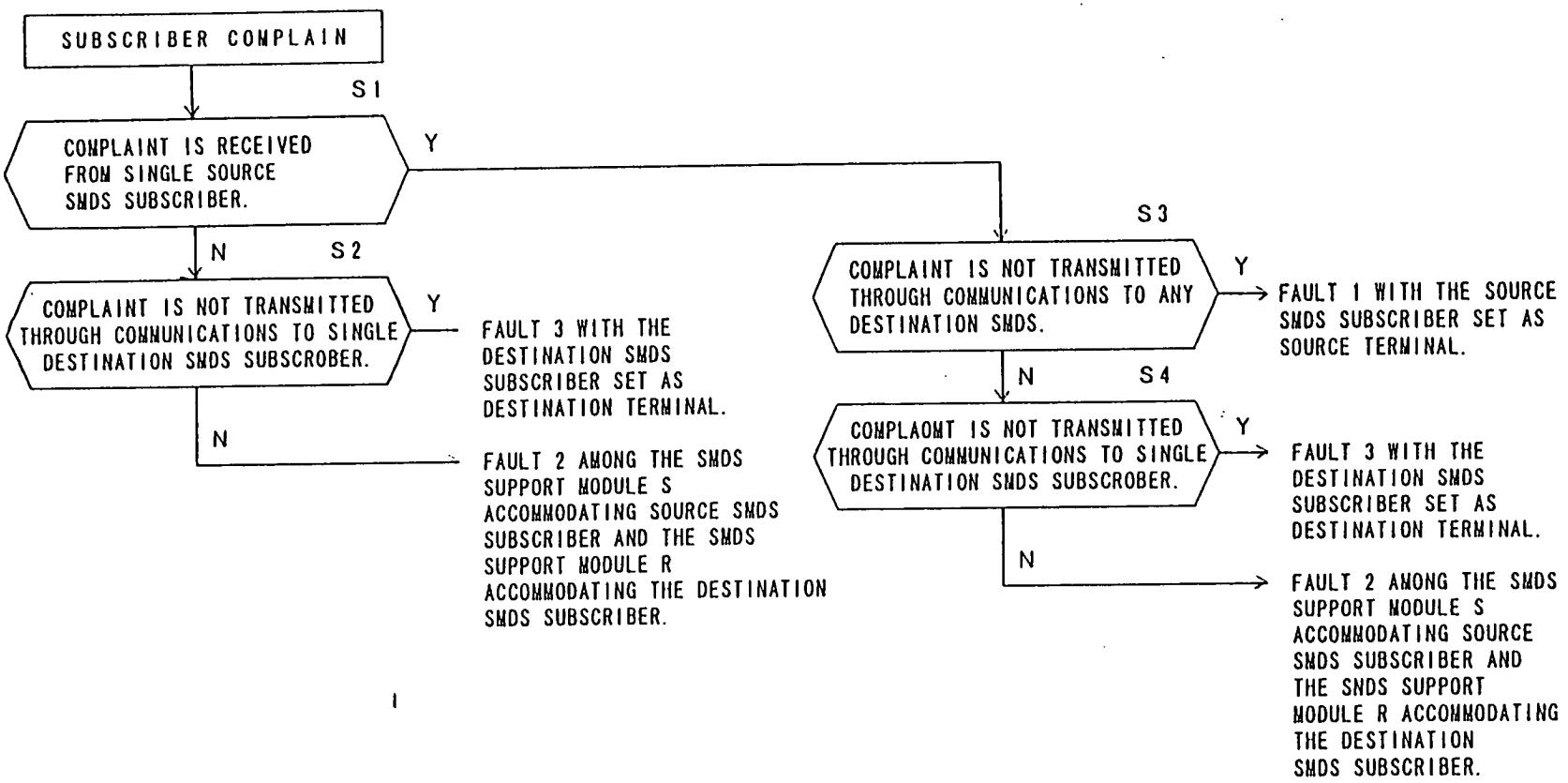

SUBSCRIBER COMPLAIN
S1
COMPLAINT IS RECEIVED FROM SINGLE SOURCE SMDS SUBSCRIBER.
Y
N
S2
COMPLAINT IS NOT TRANSMITTED THROUGH COMMUNICATIONS TO SINGLE DESTINATION SMDS SUBSCROBER.
Y
FAULT 3 WITH THE DESTINATION SMDS SUBSCRIBER SET AS DESTINATION TERMINAL.
N
FAULT 2 AMONG THE SMDS SUPPORT MODULE S ACCOMMODATING SOURCE SMDS SUBSCRIBER AND THE SMDS SUPPORT MODULE R ACCOMMODATING THE DESTINATION SMDS SUBSCRIBER.
S3
COMPLAINT IS NOT TRANSMITTED THROUGH COMMUNICATIONS TO ANY DESTINATION SMDS.
Y
FAULT 1 WITH THE SOURCE SMDS SUBSCRIBER SET AS SOURCE TERMINAL.
N
S4
COMPLAOMT IS NOT TRANSMITTED THROUGH COMMUNICATIONS TO SINGLE DESTINATION SMDS SUBSCROBER.
Y
FAULT 3 WITH THE DESTINATION SMDS SUBSCRIBER SET AS DESTINATION TERMINAL.
N
FAULT 2 AMONG THE SMDS SUPPORT MODULE S ACCOMMODATING SOURCE SMDS SUBSCRIBER AND THE SNDS SUPPORT MODULE R ACCOMMODATING THE DESTINATION SMDS SUBSCRIBER.

FIG. 788

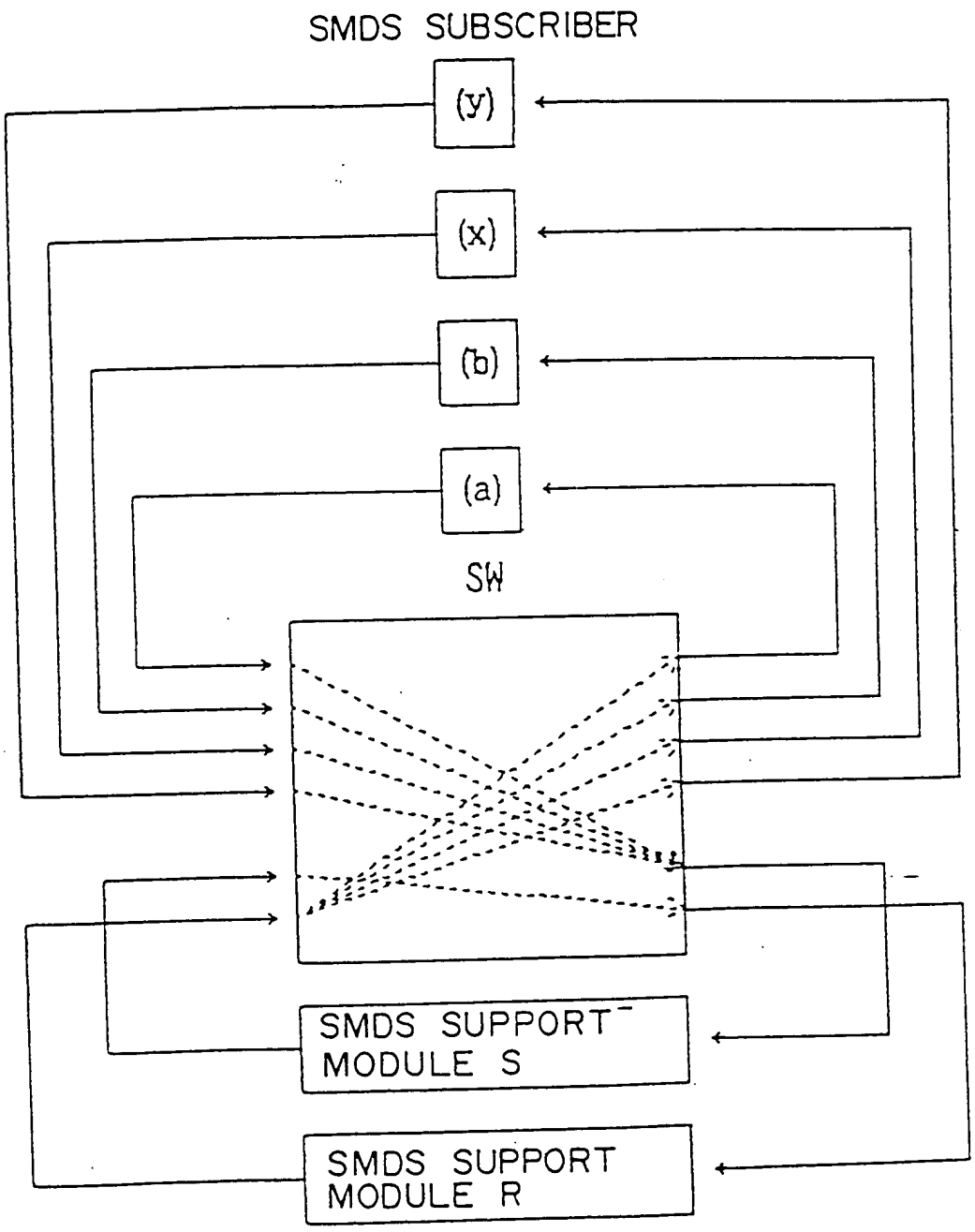

SMDS SUBSCRIBER
(y)
(x)
(b)
(a)
SW
SMDS SUPPORT MODULE S
SMDS SUPPORT MODULE R

FIG. 789

5,959,989 - 2/7/95

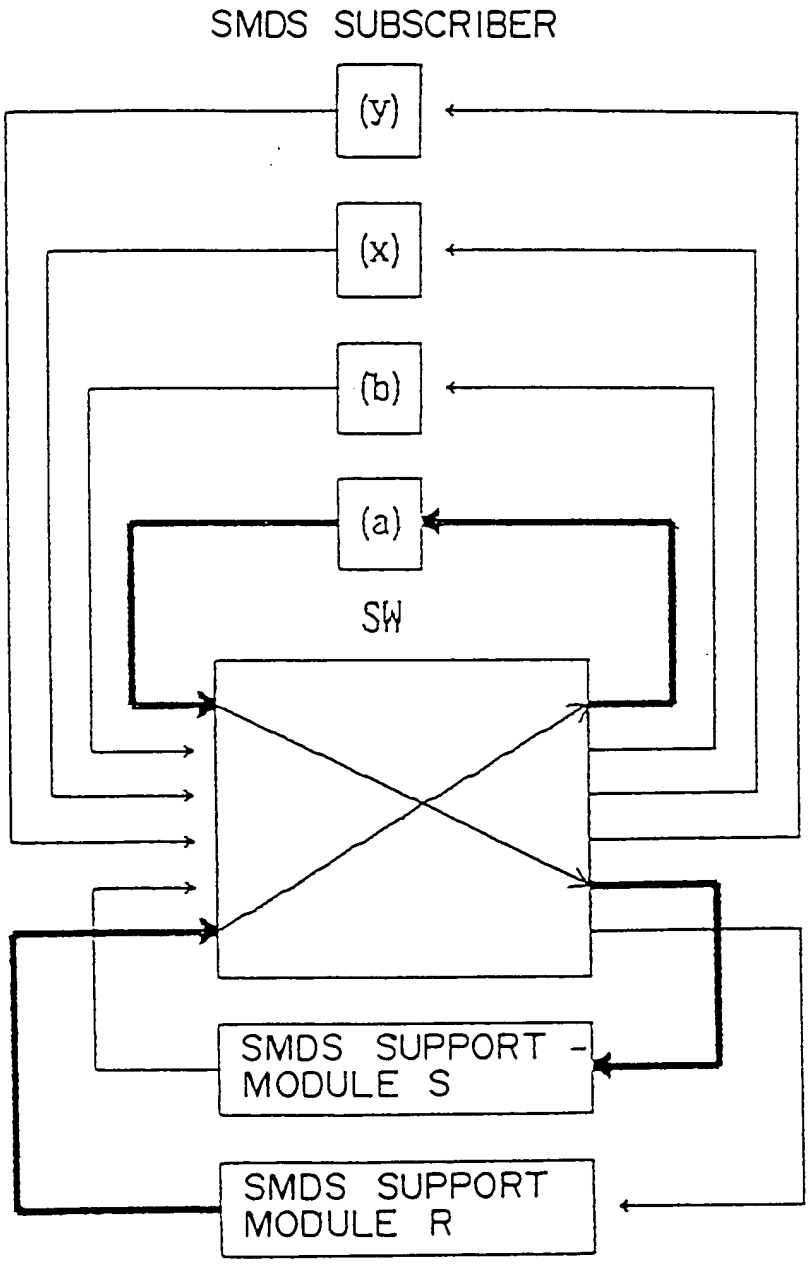


FIG. 790

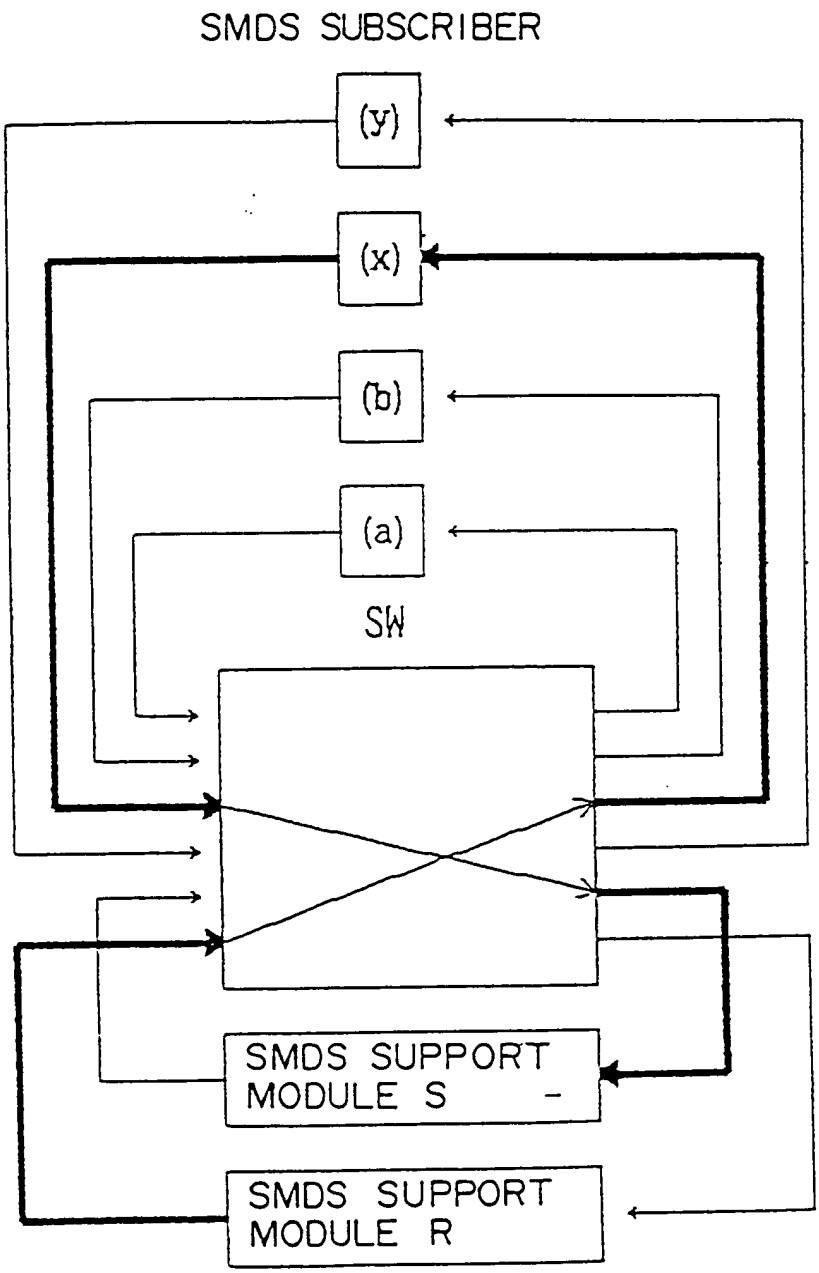

SMDS SUBSCRIBER
(y)
(x)
(b)
(a)
SW
SMDS SUPPORT MODULE S
SMDS SUPPORT MODULE R

FIG. 791

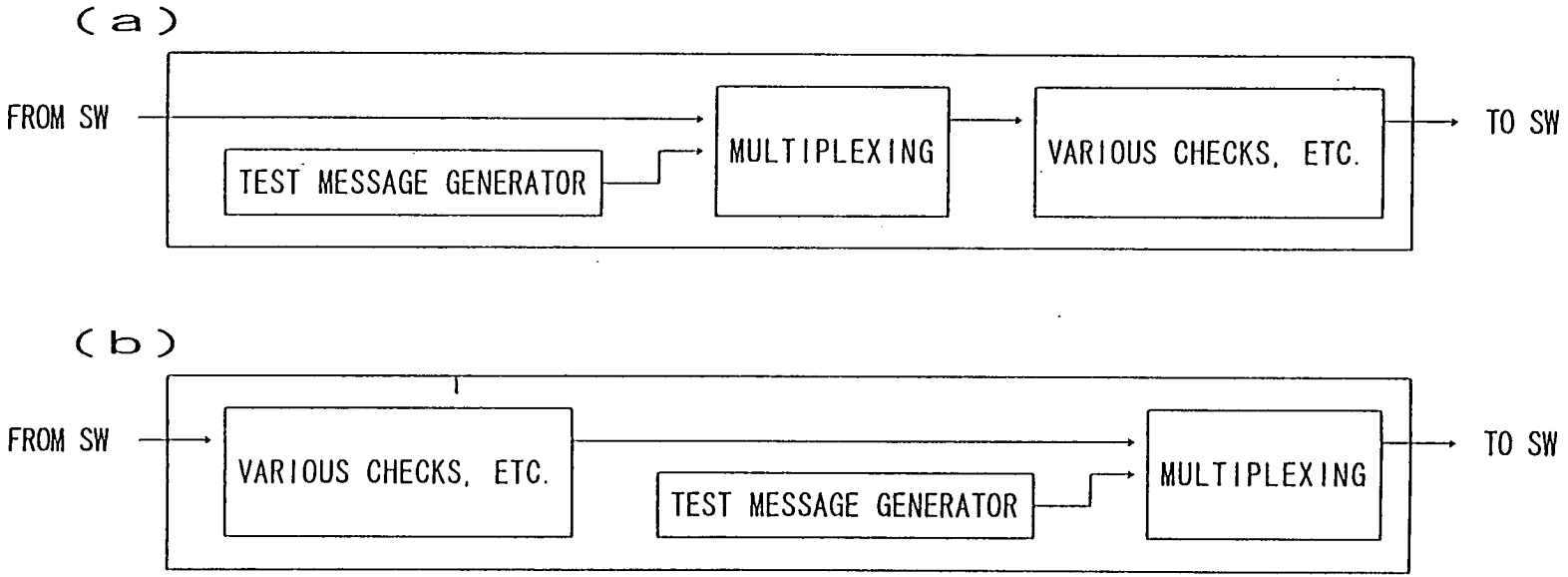

(a)
FROM SW
TEST MESSAGE GENERATOR
MULTIPLEXING
VARIOUS CHECKS, ETC.
TO SW
(b)
FROM SW
VARIOUS CHECKS, ETC.
TEST MESSAGE GENERATOR
MULTIPLEXING
TO SW

FIG. 792

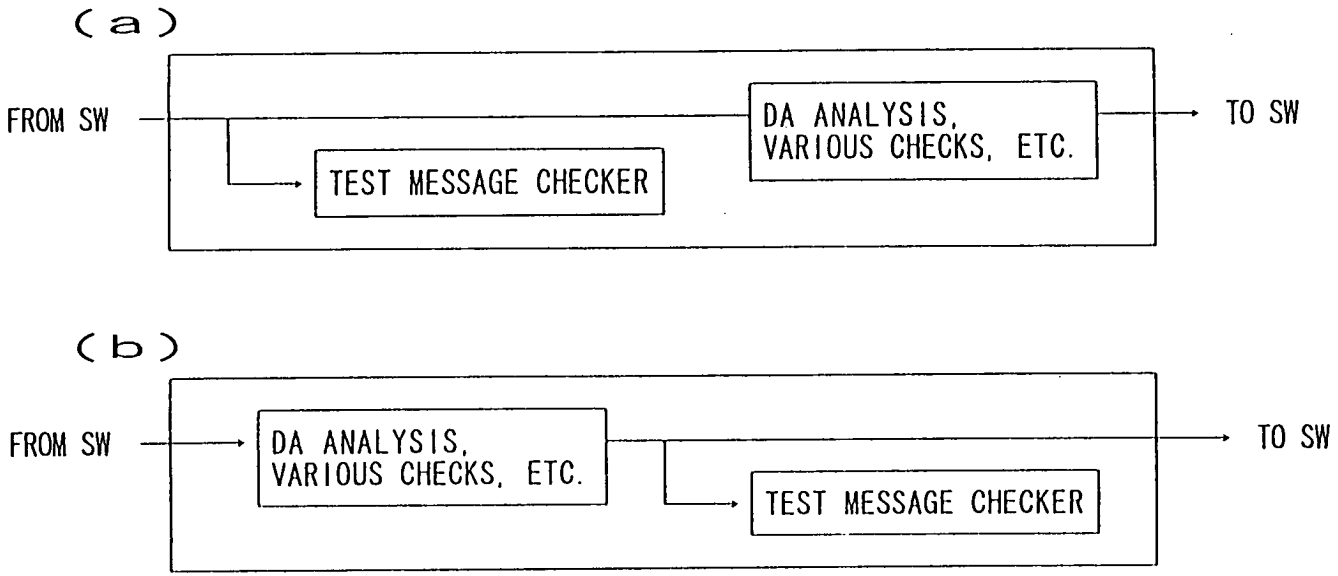

(a)
FROM SW
TEST MESSAGE CHECKER
DA ANALYSIS,
VARIOUS CHECKS, ETC.
TO SW
(b)
FROM SW
DA ANALYSIS,
VARIOUS CHECKS, ETC.
TEST MESSAGE CHECKER
TO SW

FIG. 793

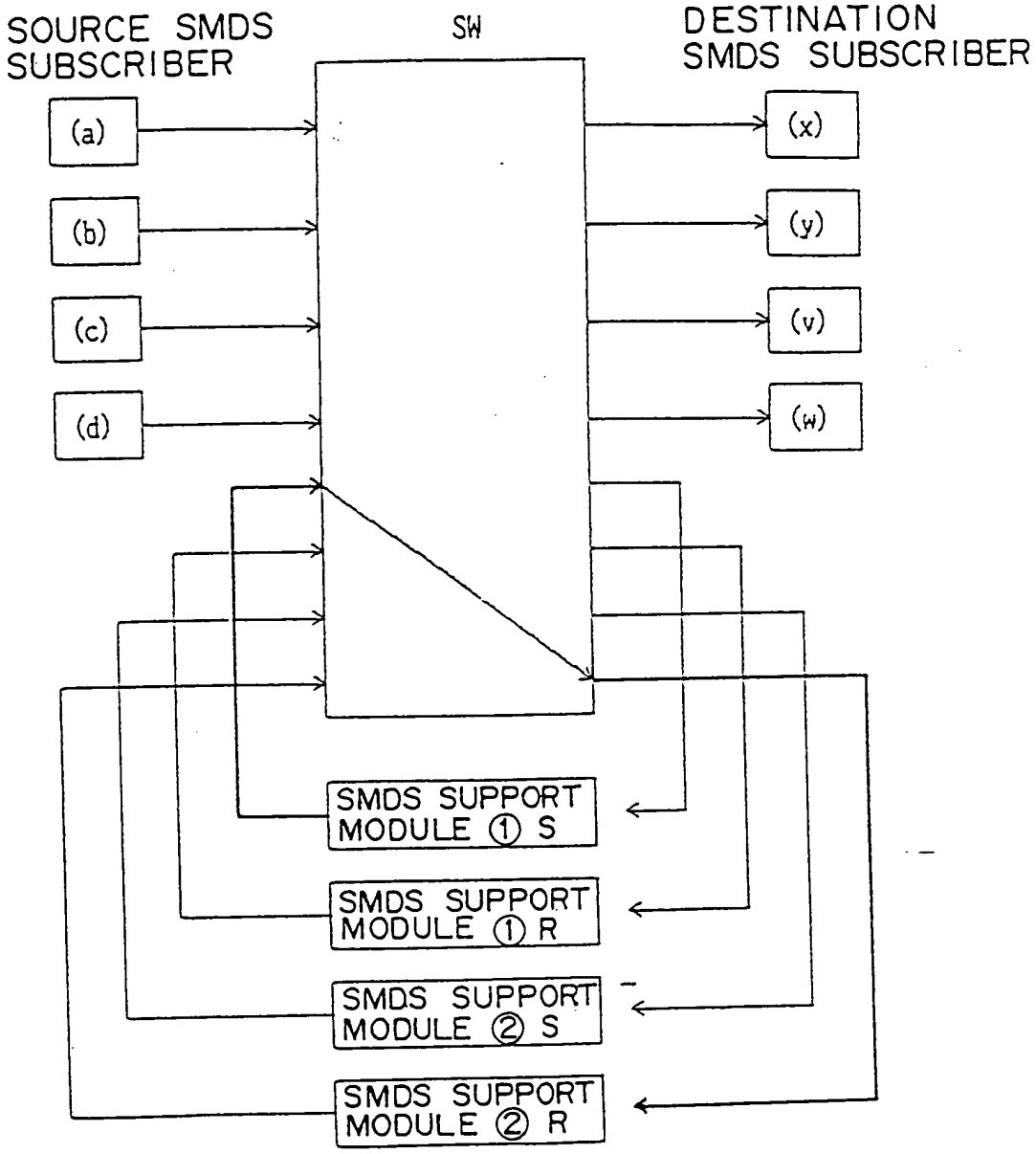

SOURCE SMDS SUBSCRIBER
SW
DESTINATION SMDS SUBSCRIBER
(a)
(b)
(c)
(d)
(x)
(y)
(v)
(w)
SMDS SUPPORT MODULE ① S
SMDS SUPPORT MODULE ① R
SMDS SUPPORT MODULE ② S
SMDS SUPPORT MODULE ② R

FIG. 794

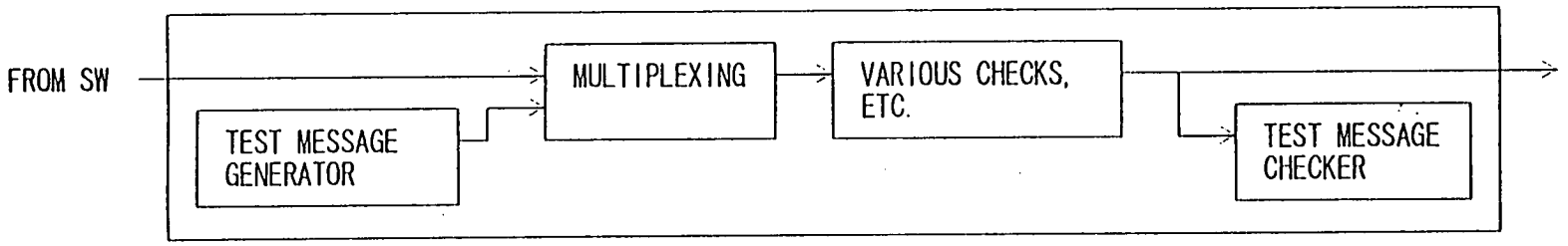
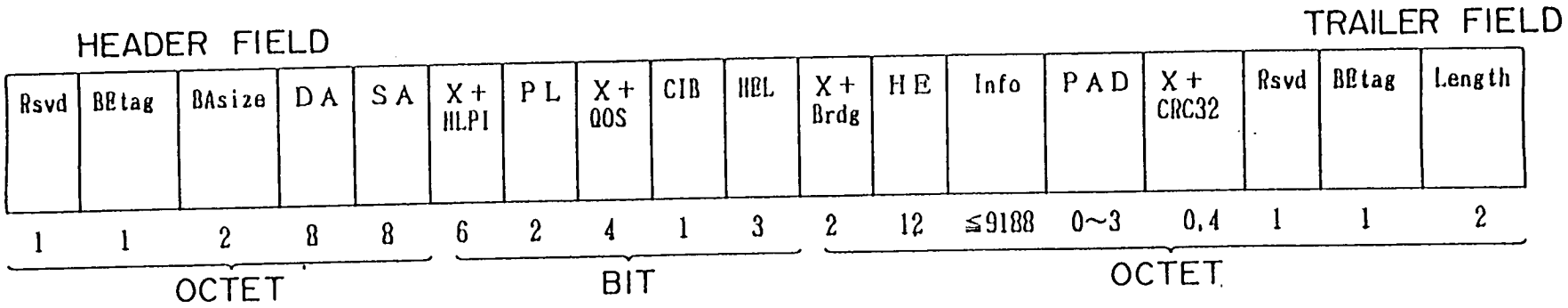

FROM SW
MULTIPLEXING
VARIOUS CHECKS, ETC.
TEST MESSAGE GENERATOR
TEST MESSAGE CHECKER

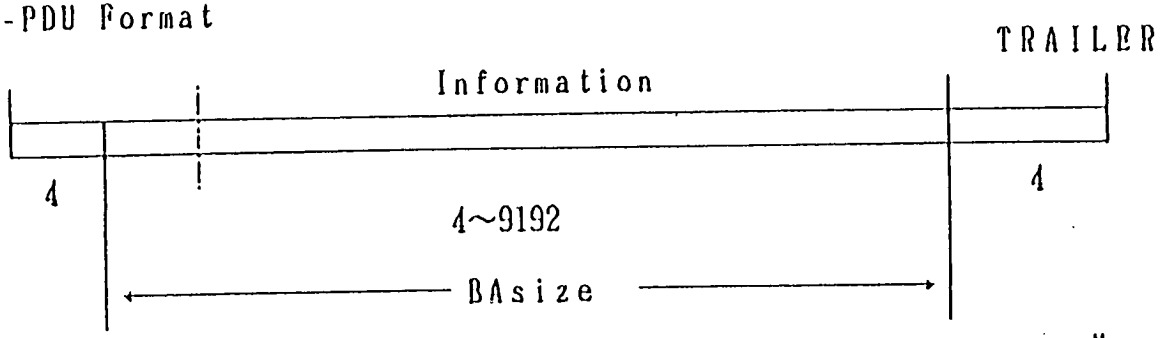
FIG. 795



Rsvd = Reserved
BEtag = Beginning-End Tag
BAsize = Buffer Allocation Size = Length
DA = Destination Address
SA = Source Address
X+ = Not processed by the network
HLPI = Higher Layer Protocol Identifier
PL = PAD Length
QOS = Quality of Service
CIB = CRC32 Indication Bit
HEL = Header Extension Length
Brdg = Bridging
HE = Header Extension
Info = Information
CRC32 = 32-bit Cyclic Redundancy Check

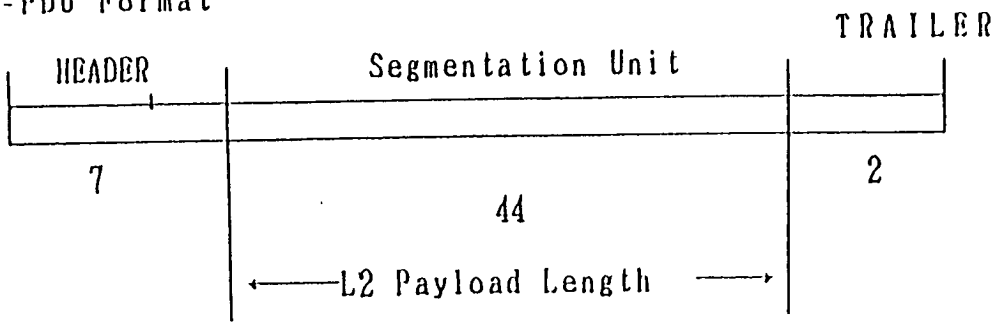
FIG. 796

L3-PDU Format



* UNIT IS ALL "OCTET"

L2-PDU Format



* UNIT IS ALL "OCTET"

FIG. 797

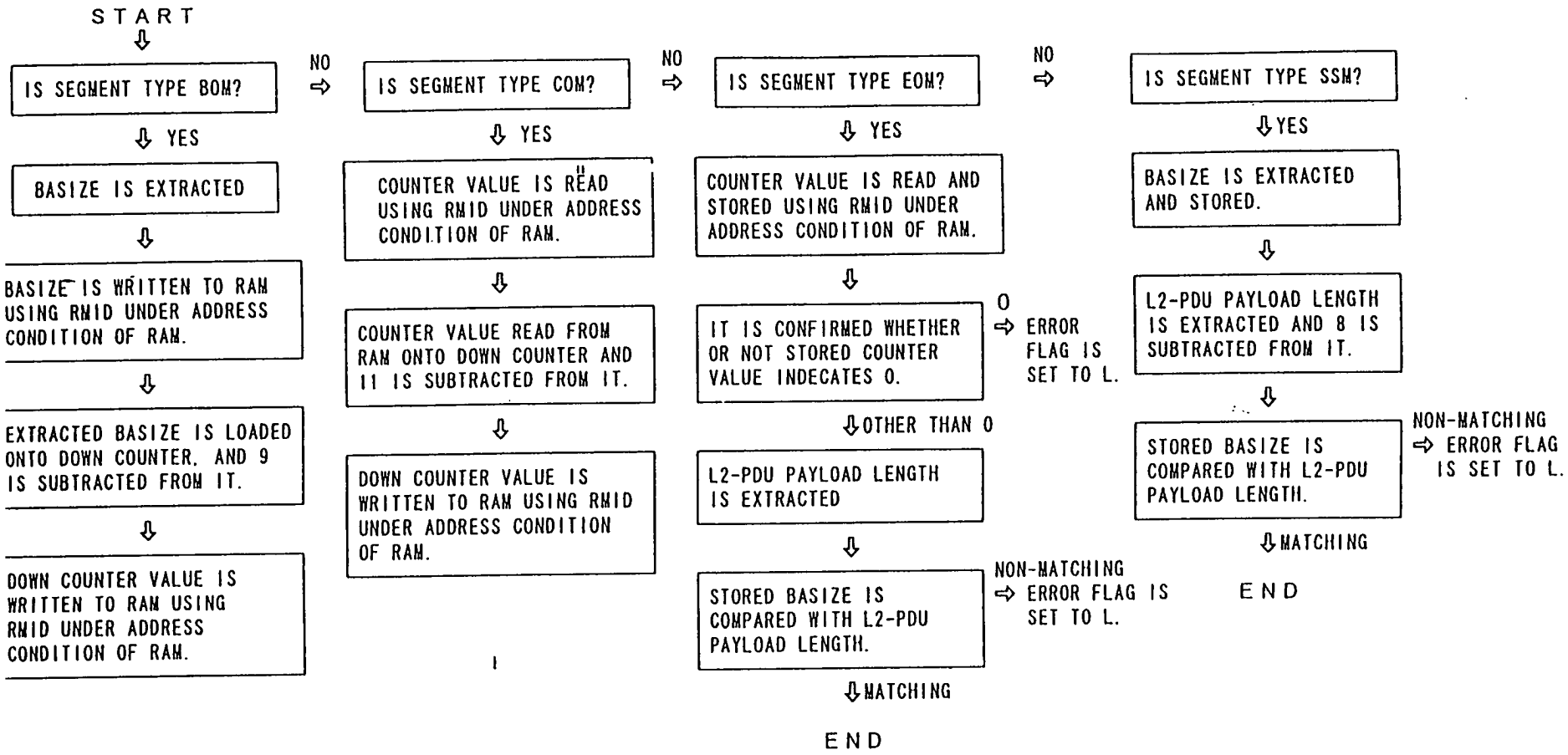

START
IS SEGMENT TYPE BOM?
NO
YES
BASIZE IS EXTRACTED
BASIZE IS WRITTEN TO RAM USING RMID UNDER ADDRESS CONDITION OF RAM.
EXTRACTED BASIZE IS LOADED ONTO DOWN COUNTER. AND 9 IS SUBTRACTED FROM IT.
DOWN COUNTER VALUE IS WRITTEN TO RAM USING RMID UNDER ADDRESS CONDITION OF RAM.
IS SEGMENT TYPE COM?
NO
YES
COUNTER VALUE IS READ USING RMID UNDER ADDRESS CONDITION OF RAM.
COUNTER VALUE READ FROM RAM ONTO DOWN COUNTER AND 11 IS SUBTRACTED FROM IT.
DOWN COUNTER VALUE IS WRITTEN TO RAM USING RMID UNDER ADDRESS CONDITION OF RAM.
IS SEGMENT TYPE EOM?
NO
YES
COUNTER VALUE IS READ AND STORED USING RMID UNDER ADDRESS CONDITION OF RAM.
IT IS CONFIRMED WHETHER OR NOT STORED COUNTER VALUE INDECATES 0.
0
ERROR FLAG IS SET TO L.
OTHER THAN 0
L2-PDU PAYLOAD LENGTH IS EXTRACTED
STORED BASIZE IS COMPARED WITH L2-PDU PAYLOAD LENGTH.
NON-MATCHING
ERROR FLAG IS SET TO L.
MATCHING
END
IS SEGMENT TYPE SSM?
NO
YES
BASIZE IS EXTRACTED AND STORED.
L2-PDU PAYLOAD LENGTH IS EXTRACTED AND 8 IS SUBTRACTED FROM IT.
STORED BASIZE IS COMPARED WITH L2-PDU PAYLOAD LENGTH.
NON-MATCHING
ERROR FLAG IS SET TO L.
MATCHING
END

FIG. 798

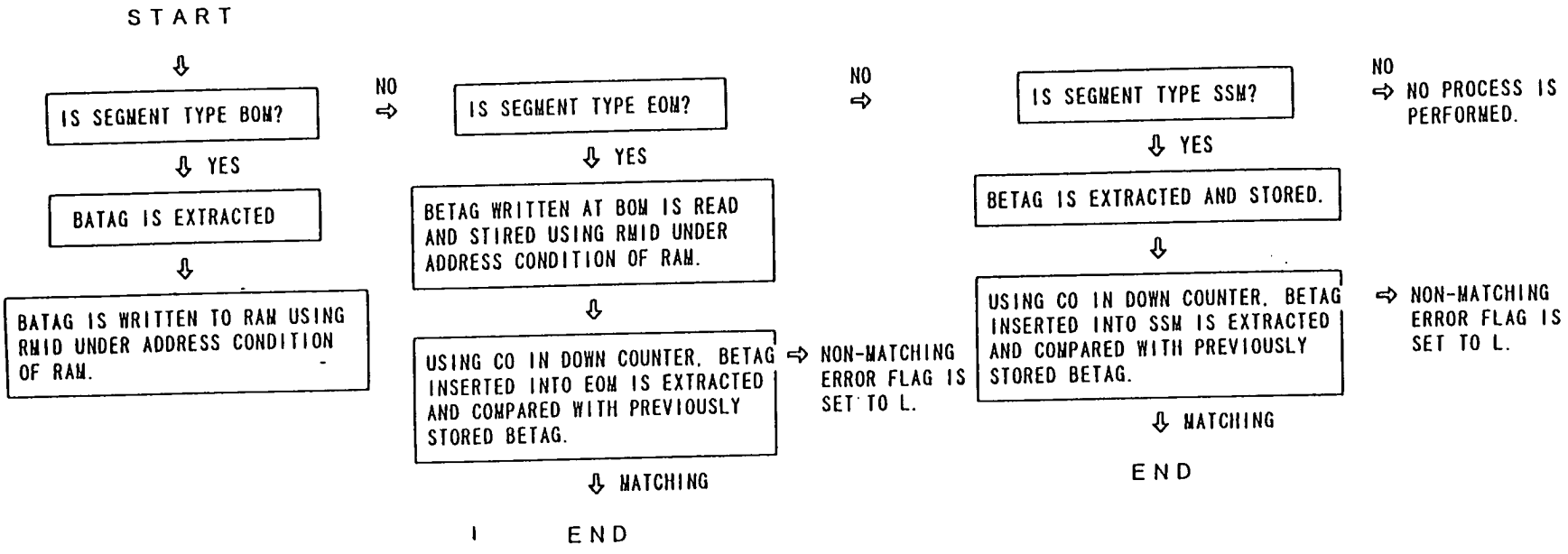

START
IS SEGMENT TYPE BOM?
YES
BATAG IS EXTRACTED
BATAG IS WRITTEN TO RAM USING RMID UNDER ADDRESS CONDITION OF RAM.
NO
IS SEGMENT TYPE EOM?
YES
BETAG WRITTEN AT BOM IS READ AND STIRED USING RMID UNDER ADDRESS CONDITION OF RAM.
USING CO IN DOWN COUNTER, BETAG INSERTED INTO EOM IS EXTRACTED AND COMPARED WITH PREVIOUSLY STORED BETAG.
NON-MATCHING ERROR FLAG IS SET TO L.
MATCHING
END
NO
IS SEGMENT TYPE SSM?
YES
BETAG IS EXTRACTED AND STORED.
USING CO IN DOWN COUNTER, BETAG INSERTED INTO SSM IS EXTRACTED AND COMPARED WITH PREVIOUSLY STORED BETAG.
NON-MATCHING ERROR FLAG IS SET TO L.
MATCHING
END
NO
NO PROCESS IS PERFORMED.

FIG. 799

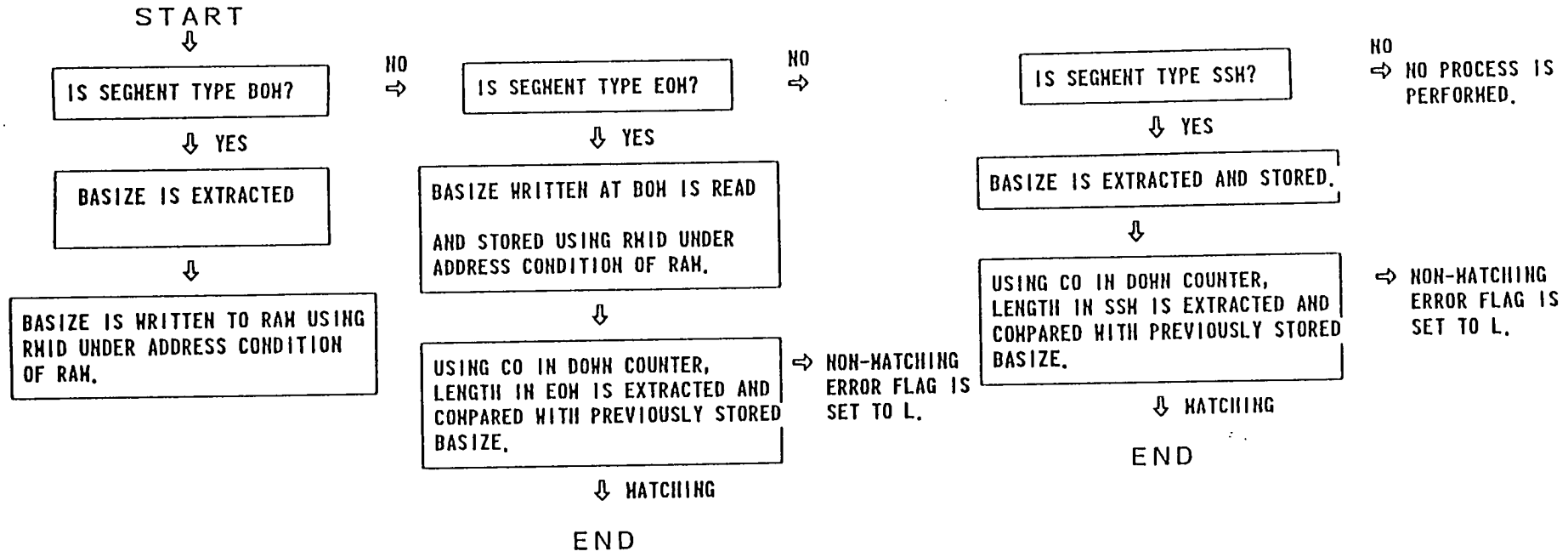

START
IS SEGMENT TYPE BOH?
NO
YES
BASIZE IS EXTRACTED
BASIZE IS WRITTEN TO RAM USING RMID UNDER ADDRESS CONDITION OF RAM.
IS SEGMENT TYPE EOH?
NO
YES
BASIZE WRITTEN AT BOH IS READ AND STORED USING RMID UNDER ADDRESS CONDITION OF RAM.
USING CO IN DOWN COUNTER, LENGTH IN EOH IS EXTRACTED AND COMPARED WITH PREVIOUSLY STORED BASIZE.
NON-MATCHING ERROR FLAG IS SET TO L.
MATCHING
END
IS SEGMENT TYPE SSH?
NO
NO PROCESS IS PERFORMED.
YES
BASIZE IS EXTRACTED AND STORED.
USING CO IN DOWN COUNTER, LENGTH IN SSH IS EXTRACTED AND COMPARED WITH PREVIOUSLY STORED BASIZE.
NON-MATCHING ERROR FLAG IS SET TO L.
MATCHING
END

FIG. 800

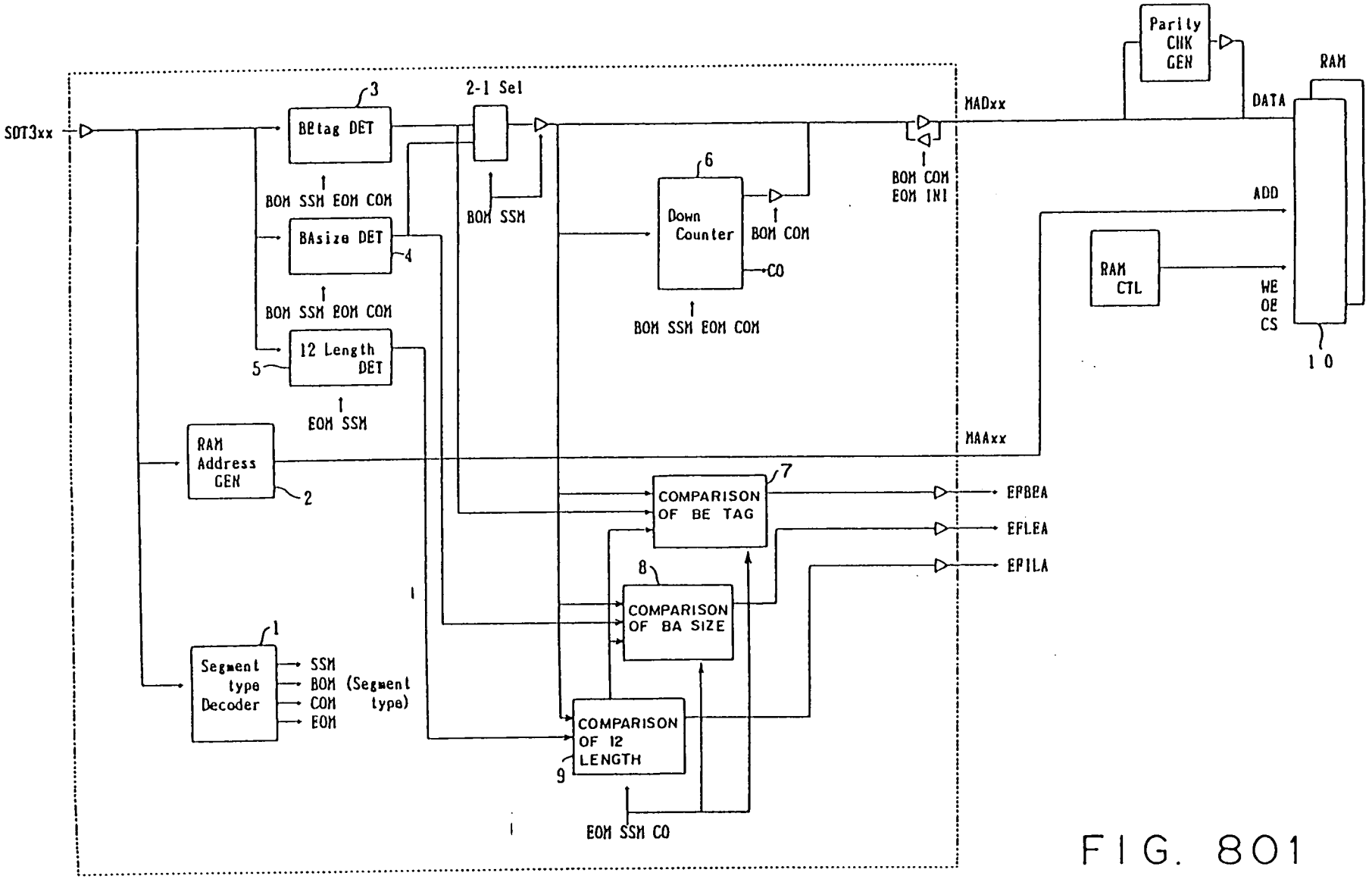

SDT3xx
BEtag DET
3
2-1 Sel
BOM SSM EOM COM
BOM SSM
BAsize DET
4
BOM SSM EOM COM
12 Length DET
5
EOM SSM
RAM Address GEN
2
Segment type Decoder
1
SSM
BOM (Segment type)
COM
EOM
Down Counter
6
BOM COM
CO
BOM SSM EOM COM
BOM COM EOM INI
MADxx
Parity CHK GEN
DATA
RAM
ADD
RAM CTL
WE
OE
CS
10
MAAxx
COMPARISON OF BE TAG
7
EPBEA
EFLEA
EPILA
8
COMPARISON OF BA SIZE
COMPARISON OF 12 LENGTH
9
EOM SSM CO

FIG. 801

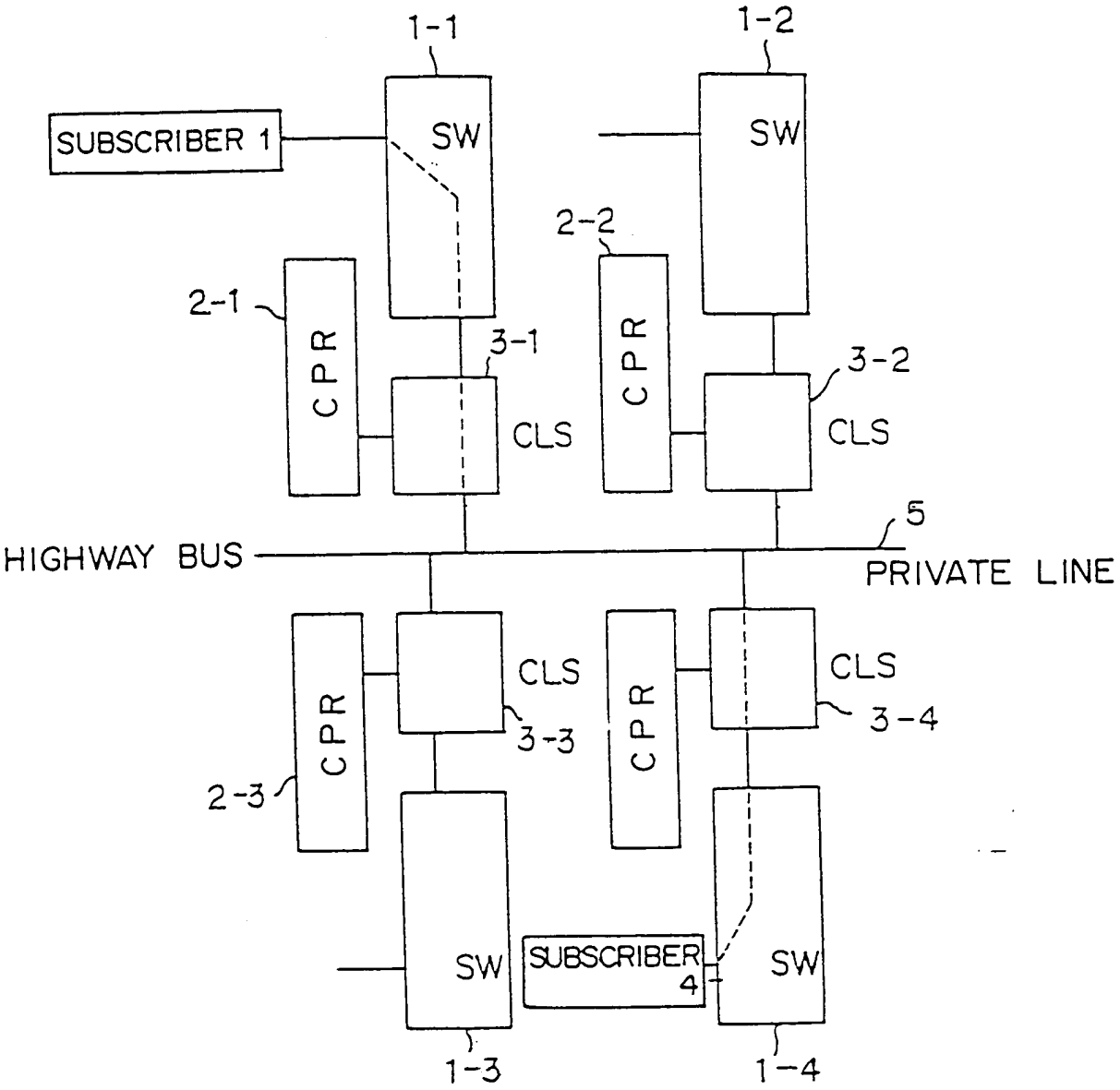

1-1
1-2
SUBSCRIBER 1
SW
SW
2-2
2-1
CPR
3-1
CPR
3-2
CLS
CLS
5
HIGHWAY BUS
PRIVATE LINE
CPR
CLS
CPR
CLS
3-3
3-4
2-3
SW
SUBSCRIBER 4
SW
1-3
1-4

FIG. 802

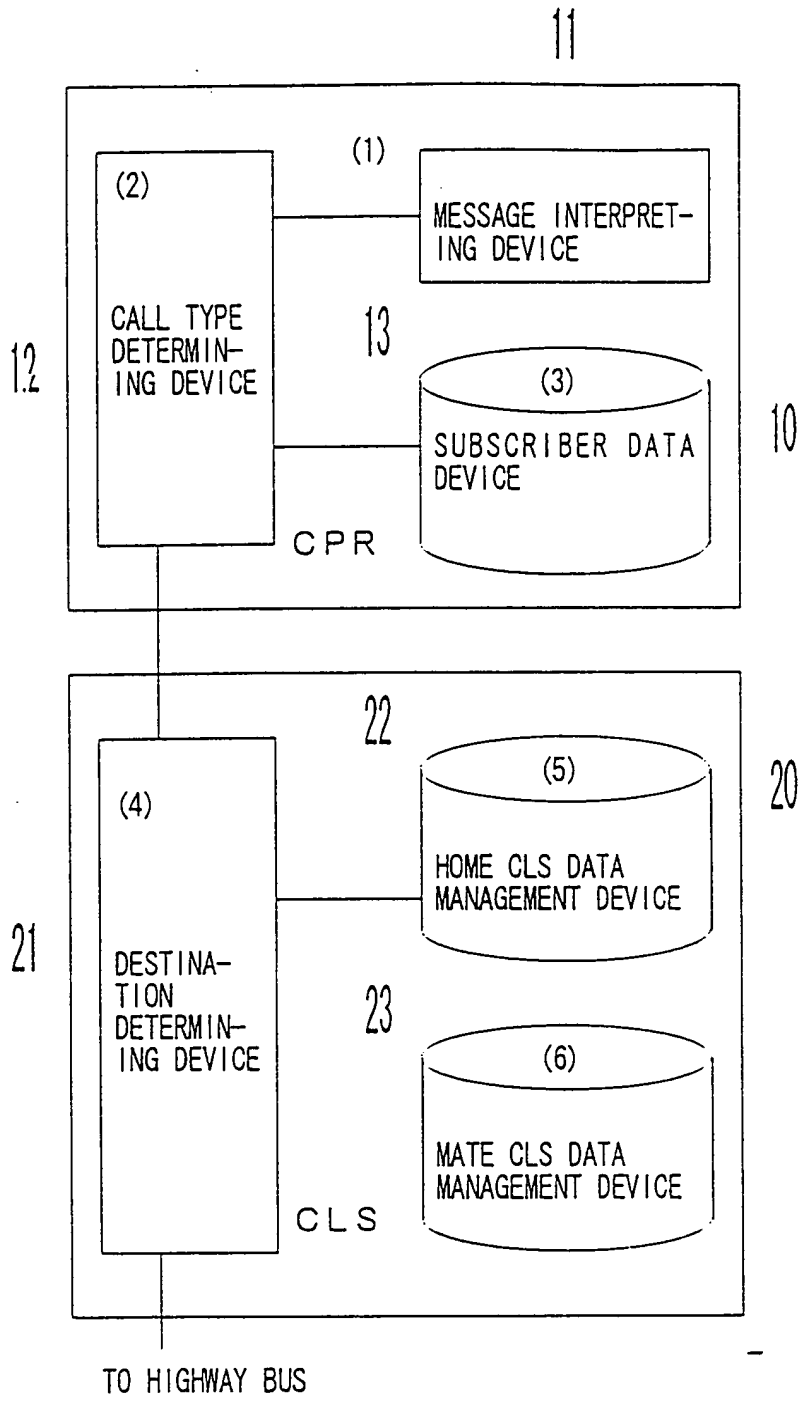

11
(1)
(2)
MESSAGE INTERPRET-
ING DEVICE
CALL TYPE
DETERMIN-
ING DEVICE
12
13
(3)
SUBSCRIBER DATA
DEVICE
10
CPR
22
(5)
20
(4)
HOME CLS DATA
MANAGEMENT DEVICE
21
DESTINA-
TION
DETERMIN-
ING DEVICE
23
(6)
MATE CLS DATA
MANAGEMENT DEVICE
CLS
TO HIGHWAY BUS

FIG. 803

(a) MANAGEMENT DATA ADDRESSED TO HOME CLS

TELEPHONE NUMBER	CONNECTION ID
0001	VCI=112, VPI=100
0002	VCI=113, VPI=100
0003	VCI=114, VPI=100
0004	VCI=115, VPI=100
⋮	⋮

(b) MANAGEMENT DATA ADDRESSED TO MATE CLS

TELEPHONE NUMBER	CLS IDENTIFICATION NUMBER
1001	0002
1002	0002
1003	0003
1004	0003
⋮	⋮

FIG. 804

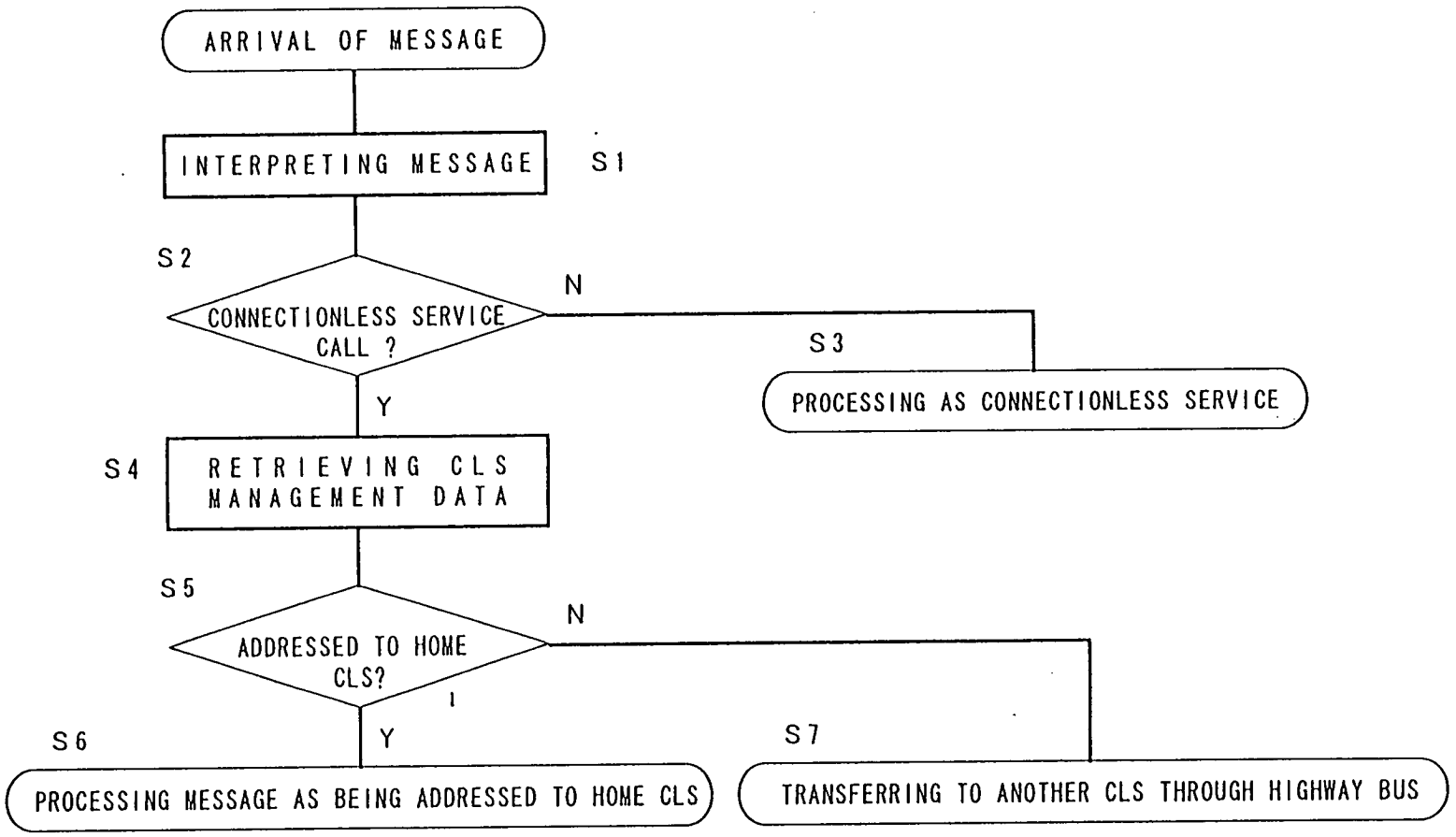

ARRIVAL OF MESSAGE
INTERPRETING MESSAGE
S1
S2
CONNECTIONLESS SERVICE CALL ?
N
S3
PROCESSING AS CONNECTIONLESS SERVICE
Y
S4
RETRIEVING CLS MANAGEMENT DATA
S5
ADDRESSED TO HOME CLS?
N
Y
S6
PROCESSING MESSAGE AS BEING ADDRESSED TO HOME CLS
S7
TRANSFERRING TO ANOTHER CLS THROUGH HIGHWAY BUS

FIG. 805

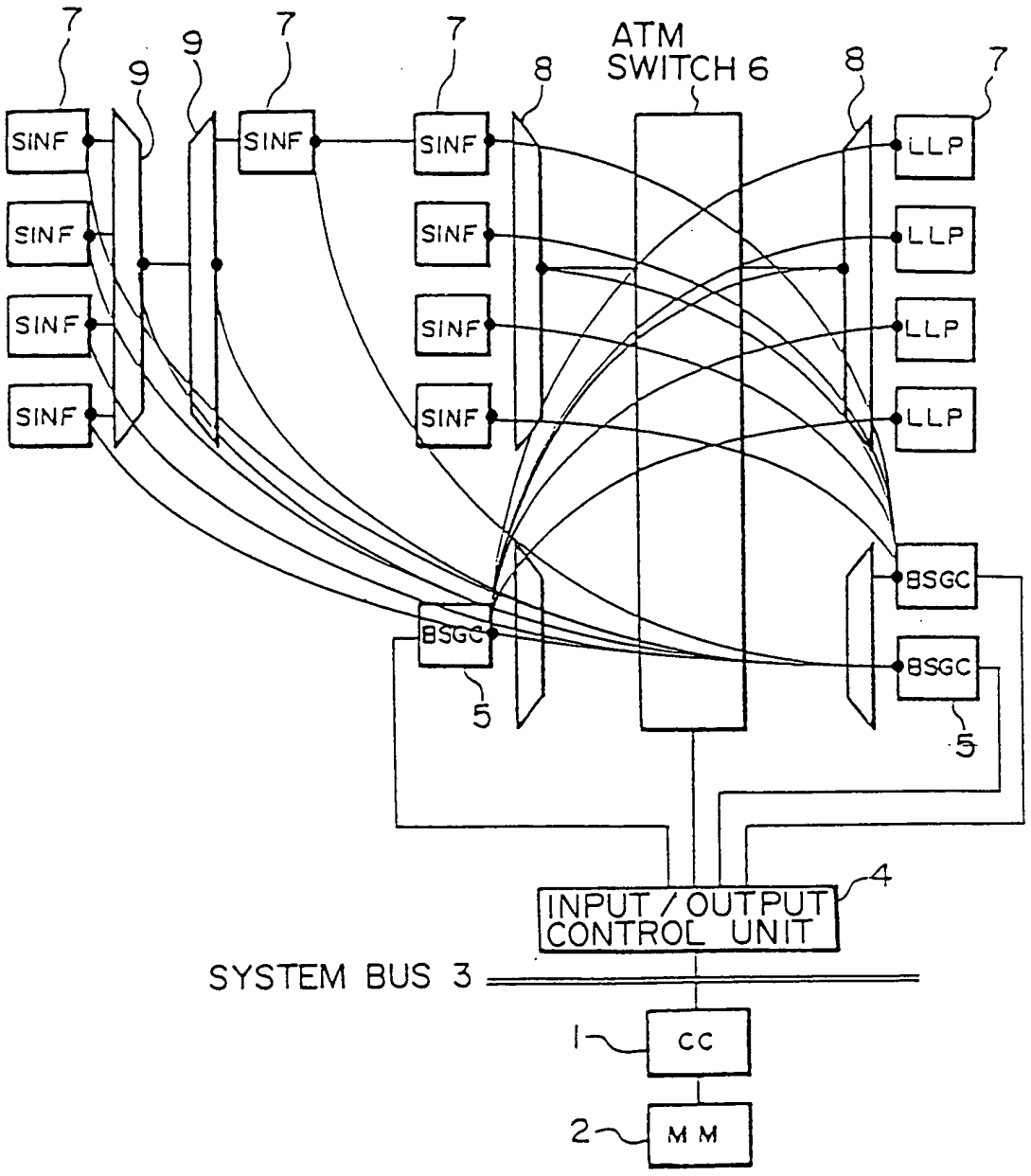

7
9
9
7
7
ATM
SWITCH 6
8
8
7
SINF
SINF
SINF
SINF
SINF
SINF
SINF
SINF
LLP
LLP
LLP
LLP
BSGC
BSGC
BSGC
5
5
INPUT / OUTPUT
CONTROL UNIT
4
SYSTEM BUS 3
1
CC
2
MM

FIG. 806

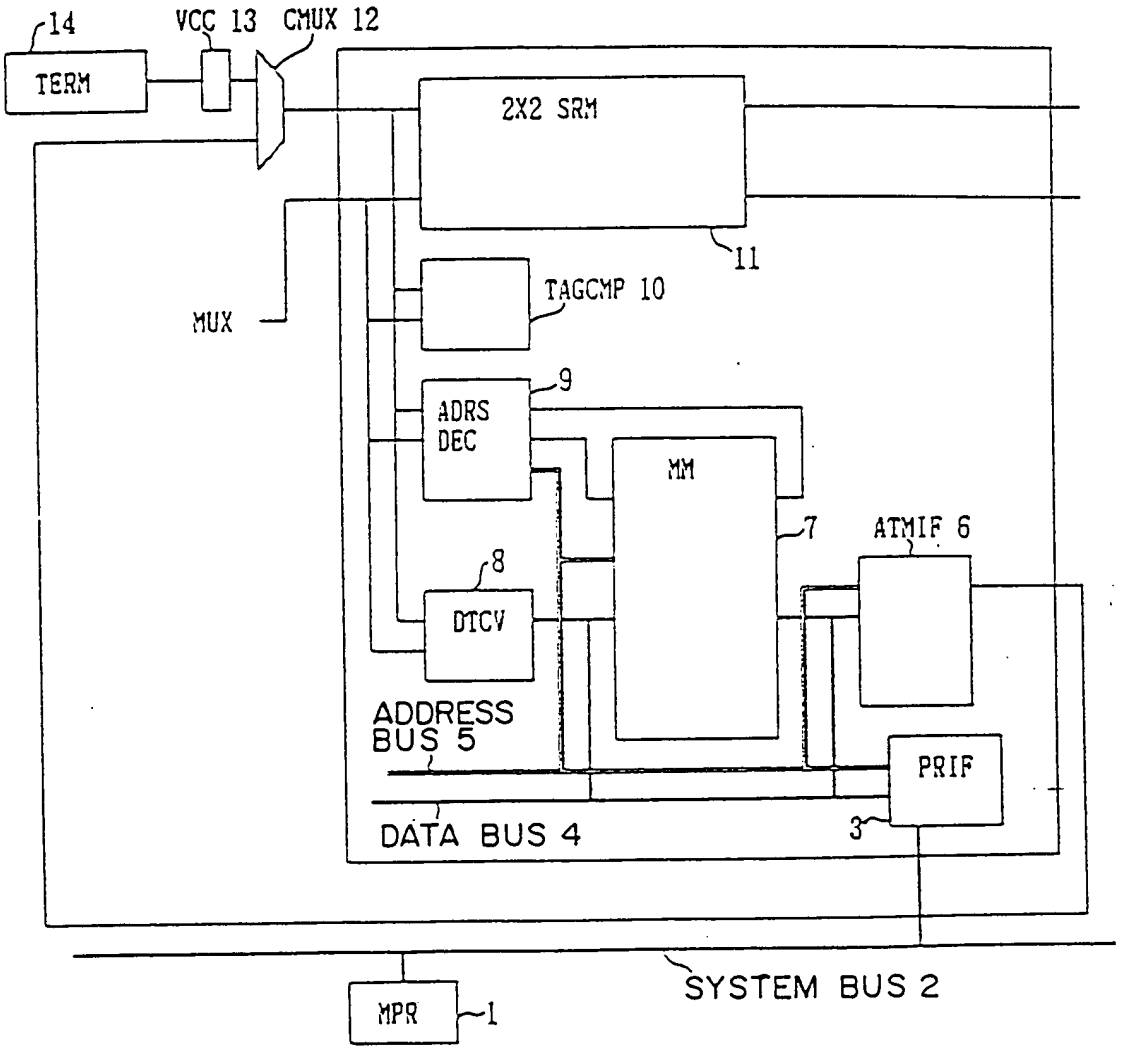

14
VCC 13
CMUX 12
TERM
2X2 SRM
11
MUX
TAGCMP 10
9
ADRS
DEC
MM
7
ATMIF 6
8
DTCV
ADDRESS
BUS 5
PRIF
3
DATA BUS 4
SYSTEM BUS 2
MPR
1

FIG. 807

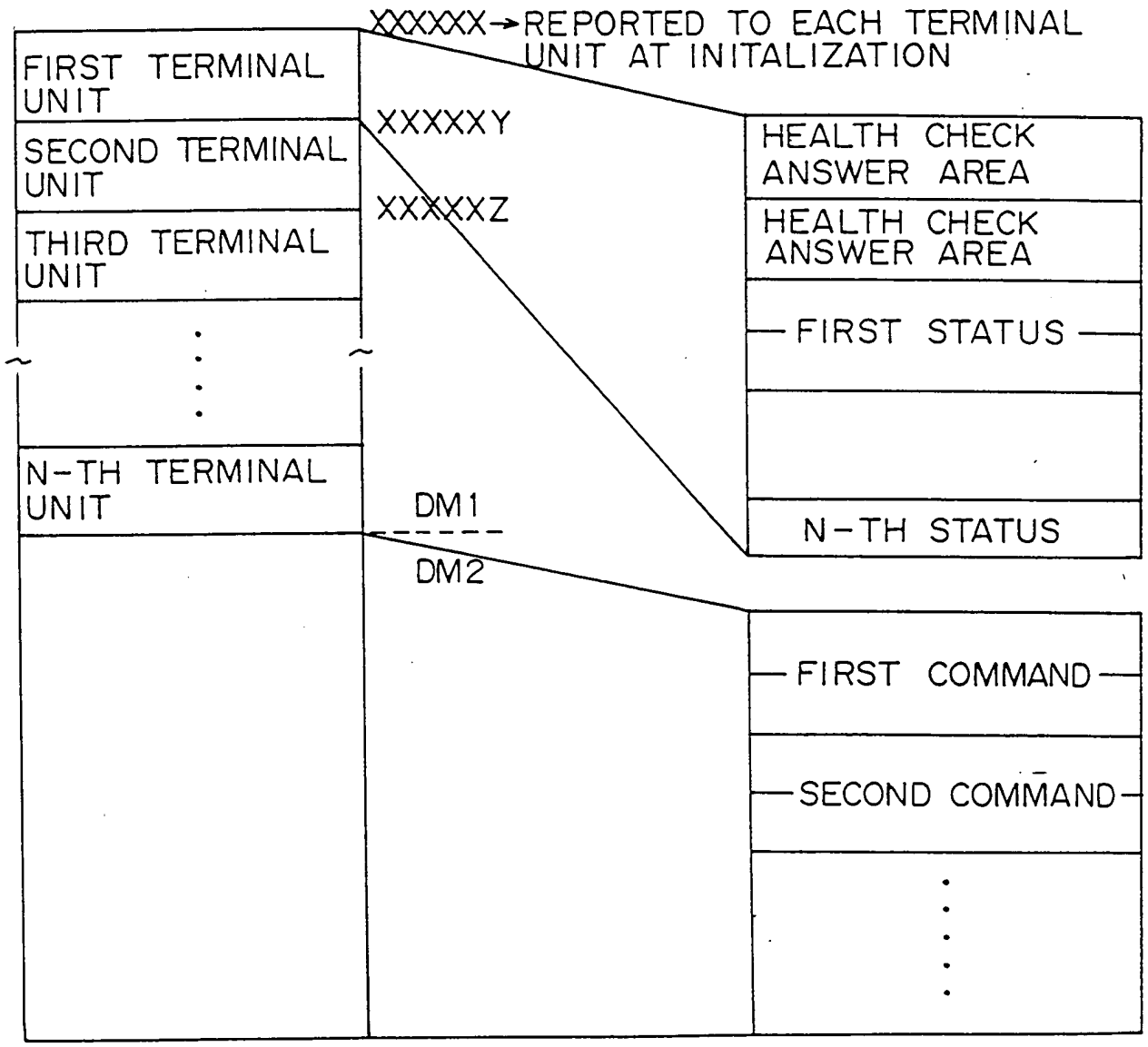
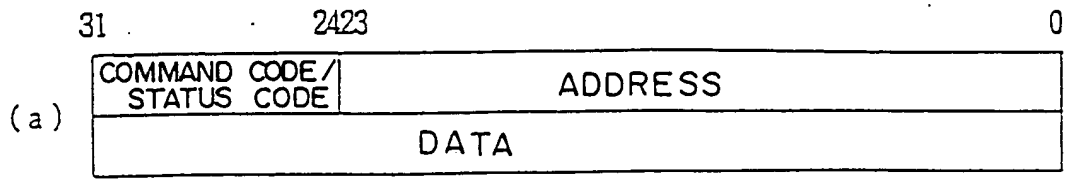
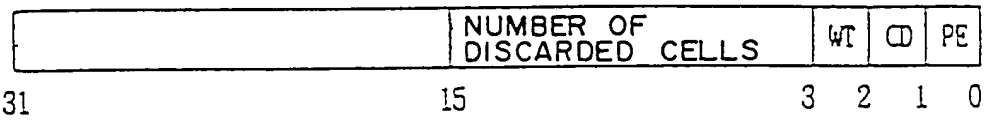

XXXXX→REPORTED TO EACH TERMINAL UNIT AT INITALIZATION
FIRST TERMINAL UNIT
SECOND TERMINAL UNIT
THIRD TERMINAL UNIT
N-TH TERMINAL UNIT
XXXXXY
XXXXXZ
DM1
DM2
HEALTH CHECK ANSWER AREA
HEALTH CHECK ANSWER AREA
FIRST STATUS
N-TH STATUS
FIRST COMMAND
SECOND COMMAND

FIG. 808

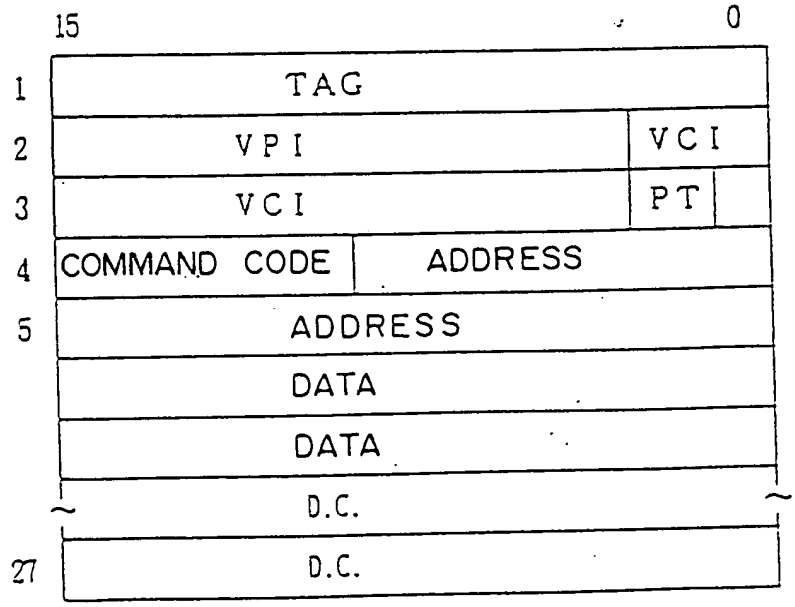


(a)



(b)

PE: PARITY ERROR
CD: CLOCK DISCONNECTION
WT: PROCESSOR FAULT



(c)

FIG. 809

669260 ET2772B0

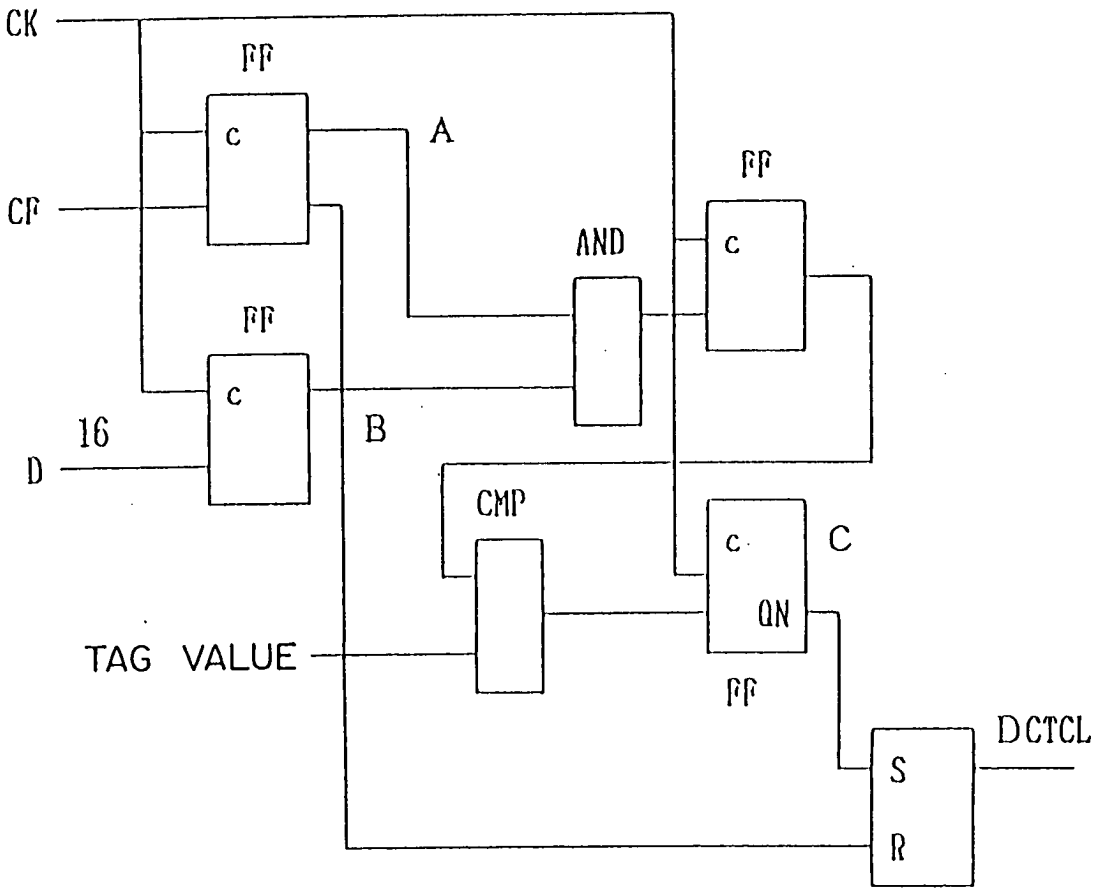


FIG. 810

6656646 2006

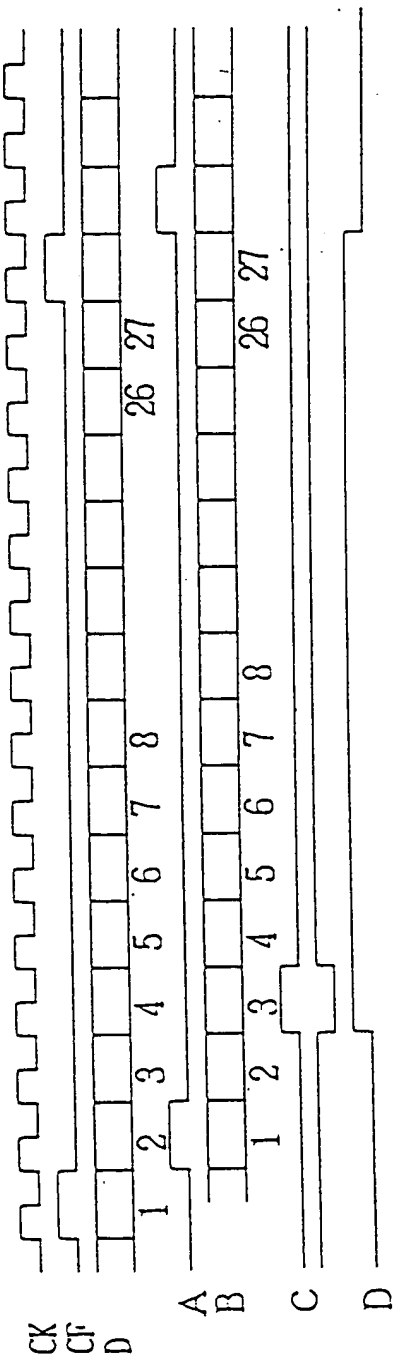


FIG. 811

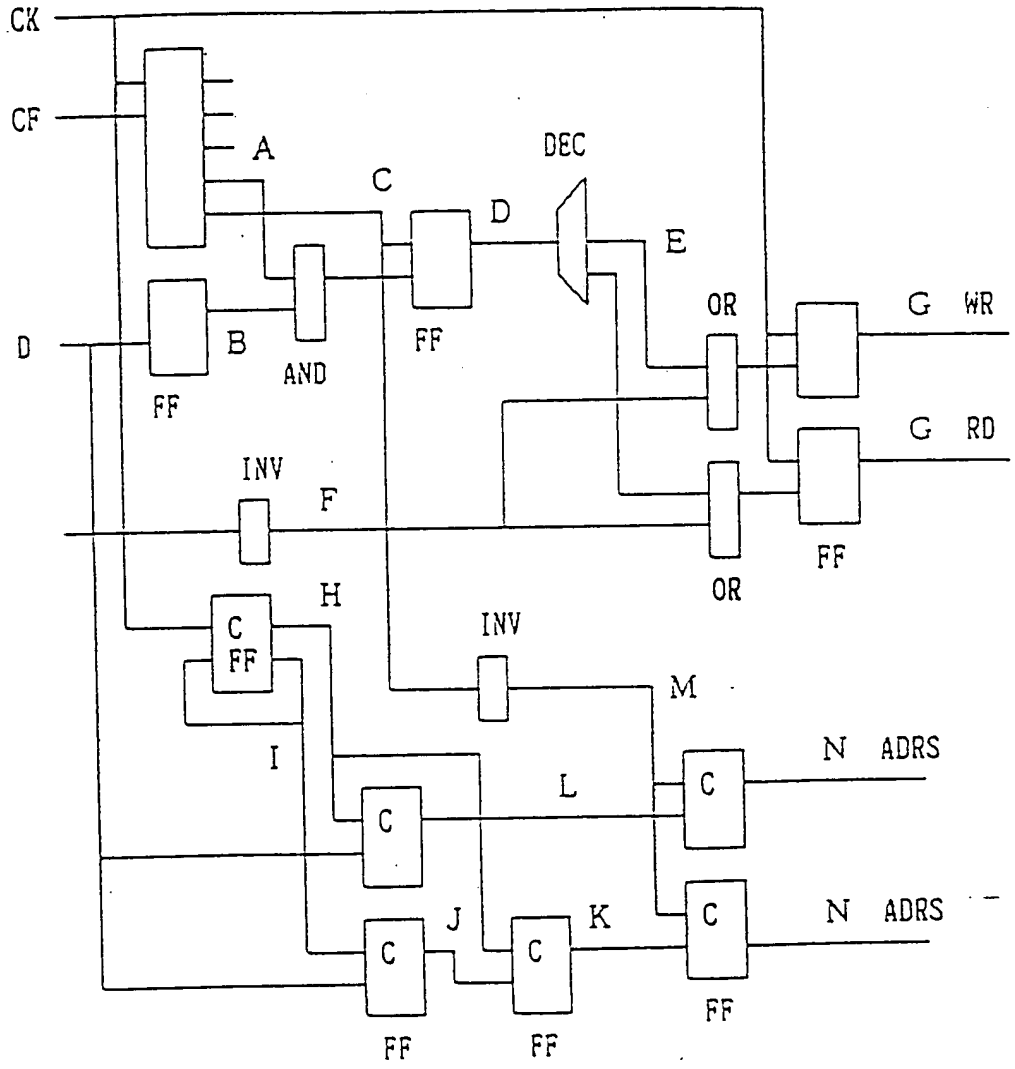

CK
CF
D
A
B
FF
AND
C
FF
D
DEC
E
OR
G WR
G RD
FF
OR
INV
F
H
C
FF
INV
M
I
L
C
N ADRS
C
J
K
C
C
N ADRS
FF
FF
FF

FIG. 812

0626260 0026260

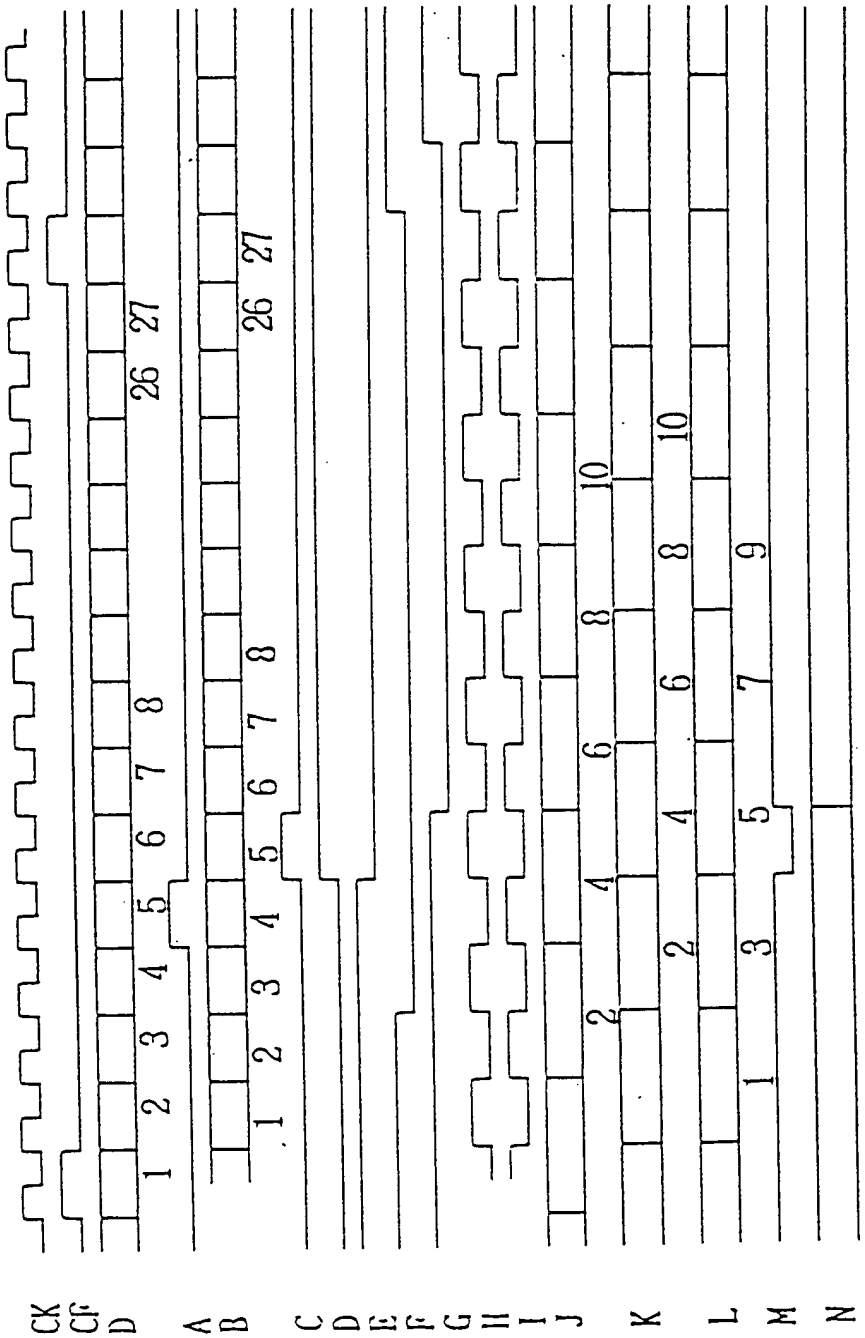


FIG. 813

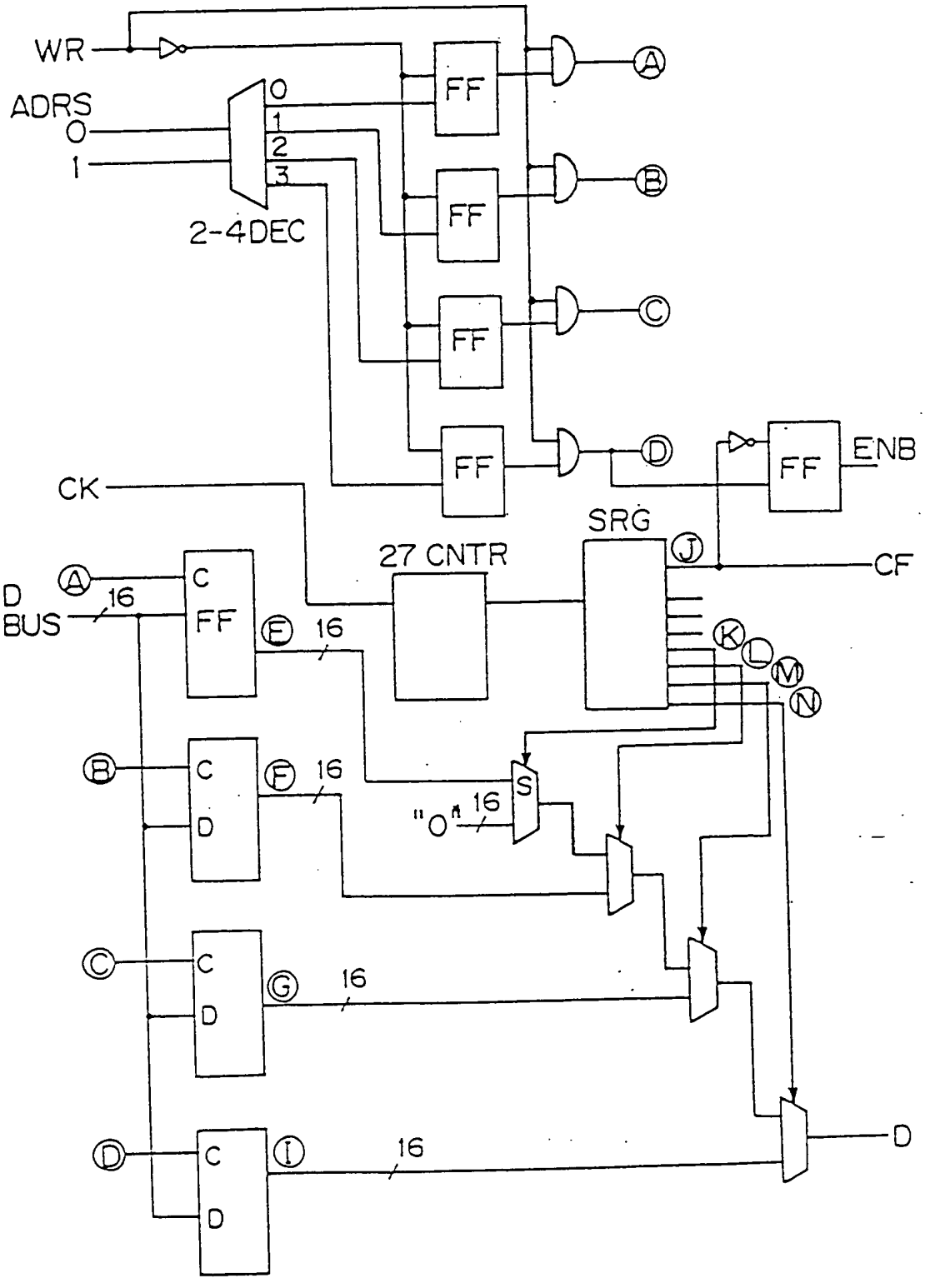

WR
ADRS
0
1
2-4DEC
0
1
2
3
FF
FF
FF
FF
A
B
C
D
FF
ENB
CK
SRG
27 CNTR
J
CF
D
BUS
16
A
C
FF
E
16
K
L
M
N
B
C
D
F
16
S
"0"
16
C
C
D
G
16
D
C
D
I
16
D

FIG. 814

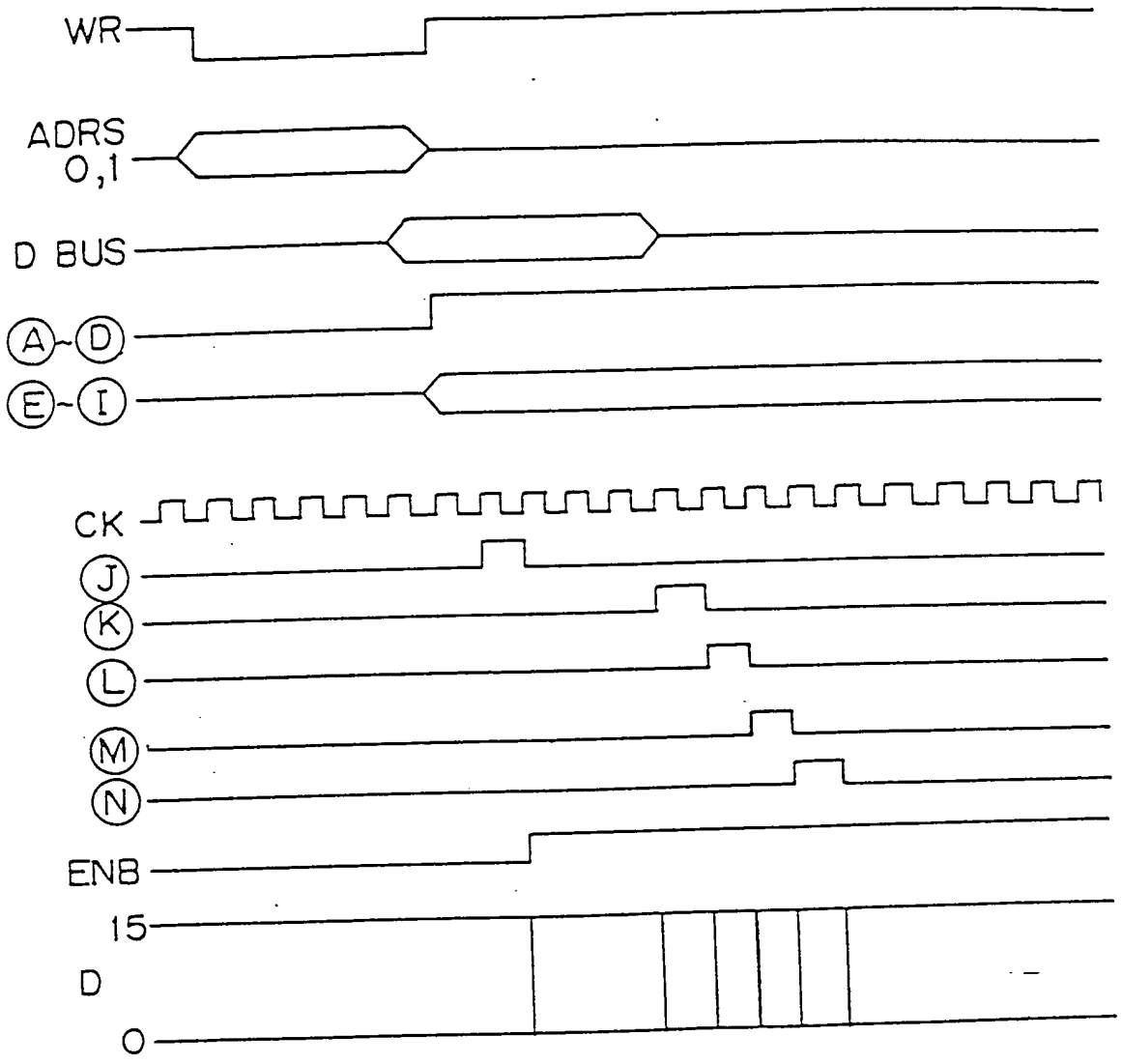
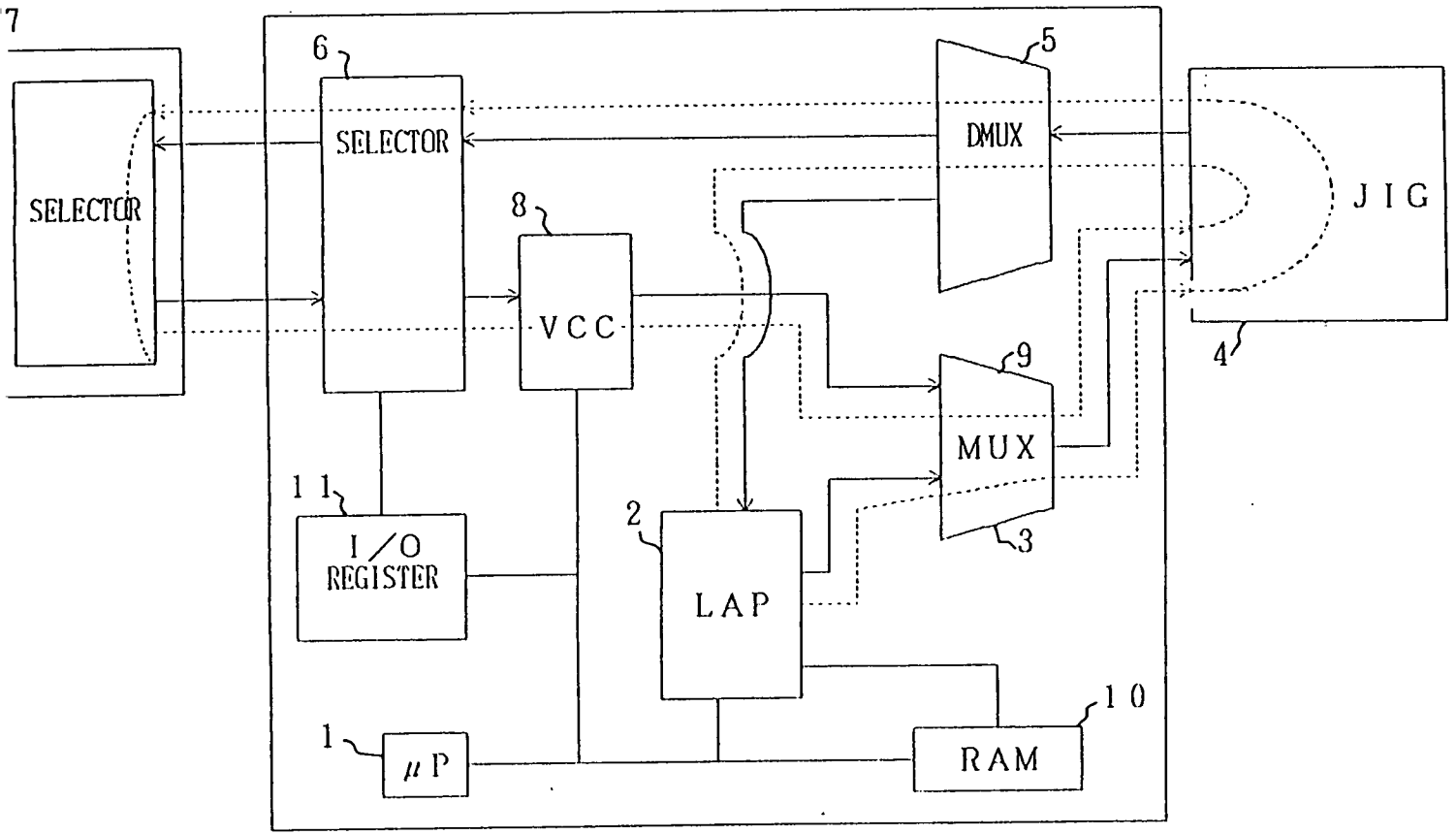


FIG. 815



VCC : ROUTING SYMBOL ASSIGNING UNIT ····· CELL DATA FLOW
LAP : LAP COMMUNICATING UNIT
μP : MICROPROCESSOR
MUX : MULTIPLEXING
DMUX : DEMULTIPLEXING

FIG. 816

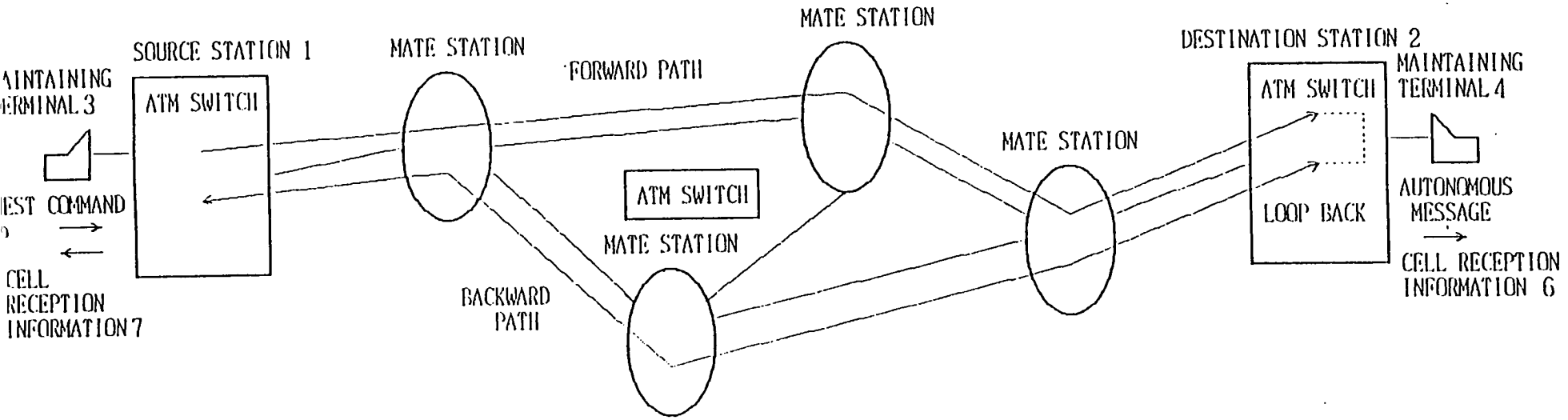

SOURCE STATION 1
ATM SWITCH
MATE STATION
FORWARD PATH
MATE STATION
ATM SWITCH
MATE STATION
BACKWARD PATH
MATE STATION
DESTINATION STATION 2
ATM SWITCH
LOOP BACK
MAINTAINING TERMINAL 4
AUTONOMOUS MESSAGE
CELL RECEPTION INFORMATION 6
CELL RECEPTION INFORMATION 7

FIG. 817

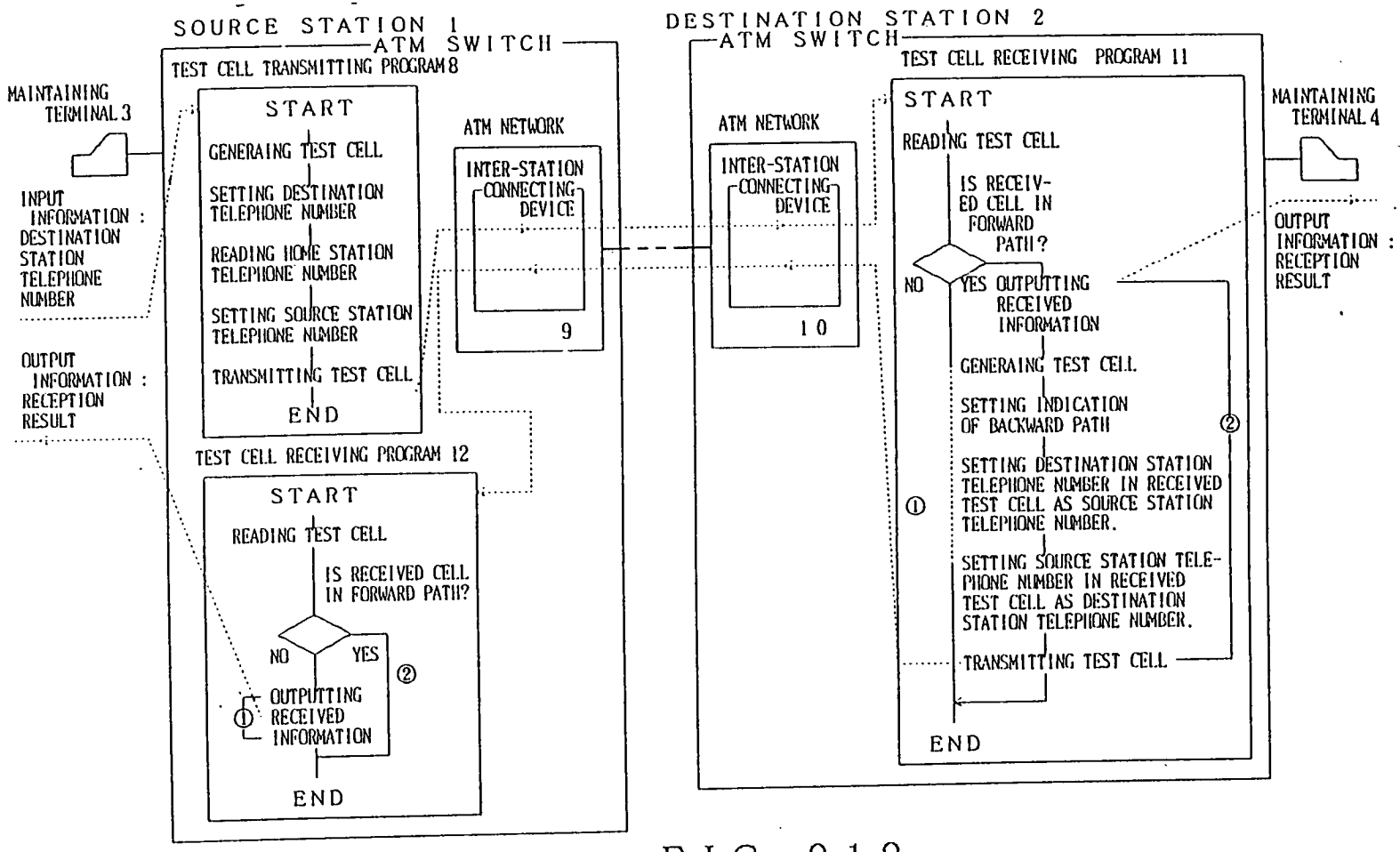

SOURCE STATION 1
ATM SWITCH
TEST CELL TRANSMITTING PROGRAM 8
START
GENERAING TEST CELL
SETTING DESTINATION TELEPHONE NUMBER
READING HOME STATION TELEPHONE NUMBER
SETTING SOURCE STATION TELEPHONE NUMBER
TRANSMITTING TEST CELL
END
MAINTAINING TERMINAL 3
INPUT INFORMATION : DESTINATION STATION TELEPHONE NUMBER
OUTPUT INFORMATION : RECEPTION RESULT
ATM NETWORK
INTER-STATION CONNECTING DEVICE
9
TEST CELL RECEIVING PROGRAM 12
START
READING TEST CELL
IS RECEIVED CELL IN FORWARD PATH?
NO
YES
②
① OUTPUTTING RECEIVED INFORMATION
END
DESTINATION STATION 2
ATM SWITCH
ATM NETWORK
INTER-STATION CONNECTING DEVICE
10
TEST CELL RECEIVING PROGRAM 11
START
READING TEST CELL
IS RECEIVED CELL IN FORWARD PATH?
NO
YES OUTPUTTING RECEIVED INFORMATION
GENERAING TEST CELL
SETTING INDICATION OF BACKWARD PATH
②
SETTING DESTINATION STATION TELEPHONE NUMBER IN RECEIVED TEST CELL AS SOURCE STATION TELEPHONE NUMBER.
①
SETTING SOURCE STATION TELEPHONE NUMBER IN RECEIVED TEST CELL AS DESTINATION STATION TELEPHONE NUMBER.
TRANSMITTING TEST CELL
END
MAINTAINING TERMINAL 4
OUTPUT INFORMATION : RECEPTION RESULT

FIG. 818

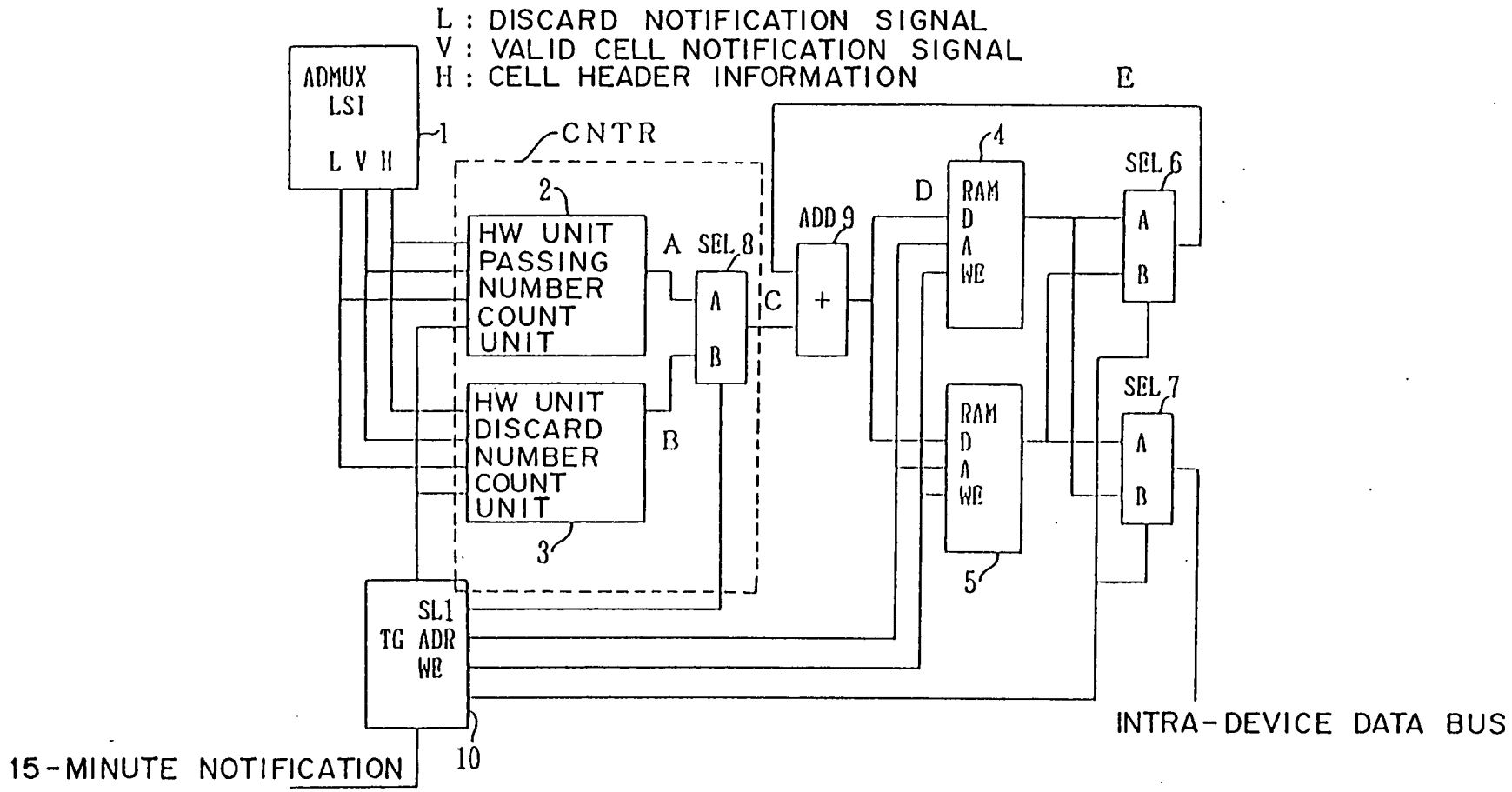

L : DISCARD NOTIFICATION SIGNAL
V : VALID CELL NOTIFICATION SIGNAL
H : CELL HEADER INFORMATION
ADMUX LSI
L V H
1
CNTR
2
HW UNIT PASSING NUMBER COUNT UNIT
HW UNIT DISCARD NUMBER COUNT UNIT
3
A
B
SEL 8
ADD 9
C
+
D
E
4
RAM D A WE
5
SEL 6
SEL 7
SL1
TG ADR WE
10
15-MINUTE NOTIFICATION
INTRA-DEVICE DATA BUS

FIG. 819

00H	DISCARD CELL NUMBER	LOWER	8	bit
01H	DISCARD CELL NUMBER		8	bit
02H	DISCARD CELL NUMBER		8	bit
03H	DISCARD CELL NUMBER	HIGHER	8	bit
04H	PASSING CELL NUMBER	LOWER	8	bit
05H	PASSING CELL NUMBER		8	bit
06H	PASSING CELL NUMBER		8	bit
07H	PASSING CELL NUMBER	HIGHER	8	bit

FIG. 820

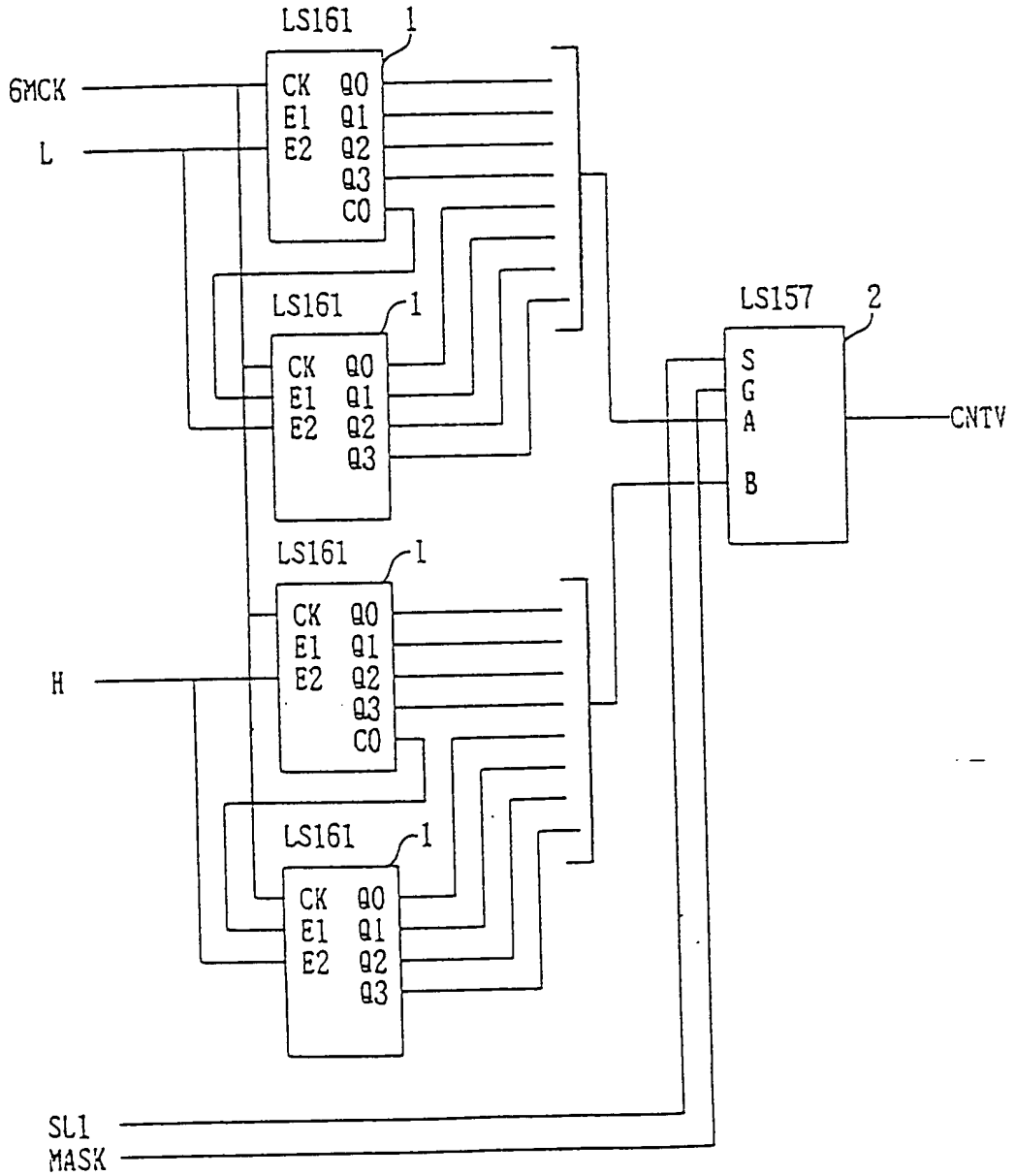

LS161
1
6MCK
L
CK
E1
E2
Q0
Q1
Q2
Q3
CO
LS161
1
CK
E1
E2
Q0
Q1
Q2
Q3
LS157
2
S
G
A
B
CNTV
LS161
1
H
CK
E1
E2
Q0
Q1
Q2
Q3
CO
LS161
1
CK
E1
E2
Q0
Q1
Q2
Q3
SL1
MASK

FIG. 821

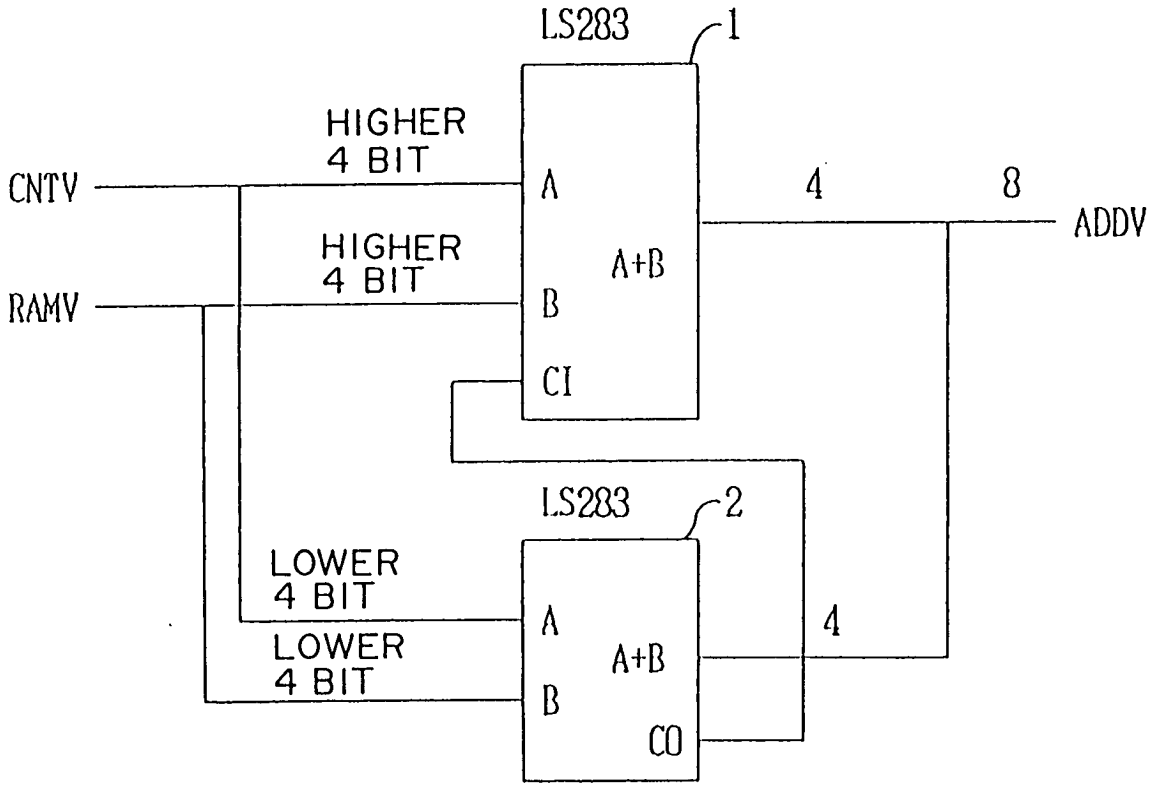

LS283
1
HIGHER
4 BIT
CNTV
A
4
8
ADDV
HIGHER
4 BIT
A+B
RAMV
B
CI
LS283
2
LOWER
4 BIT
A
4
LOWER
4 BIT
A+B
B
CO

FIG. 822

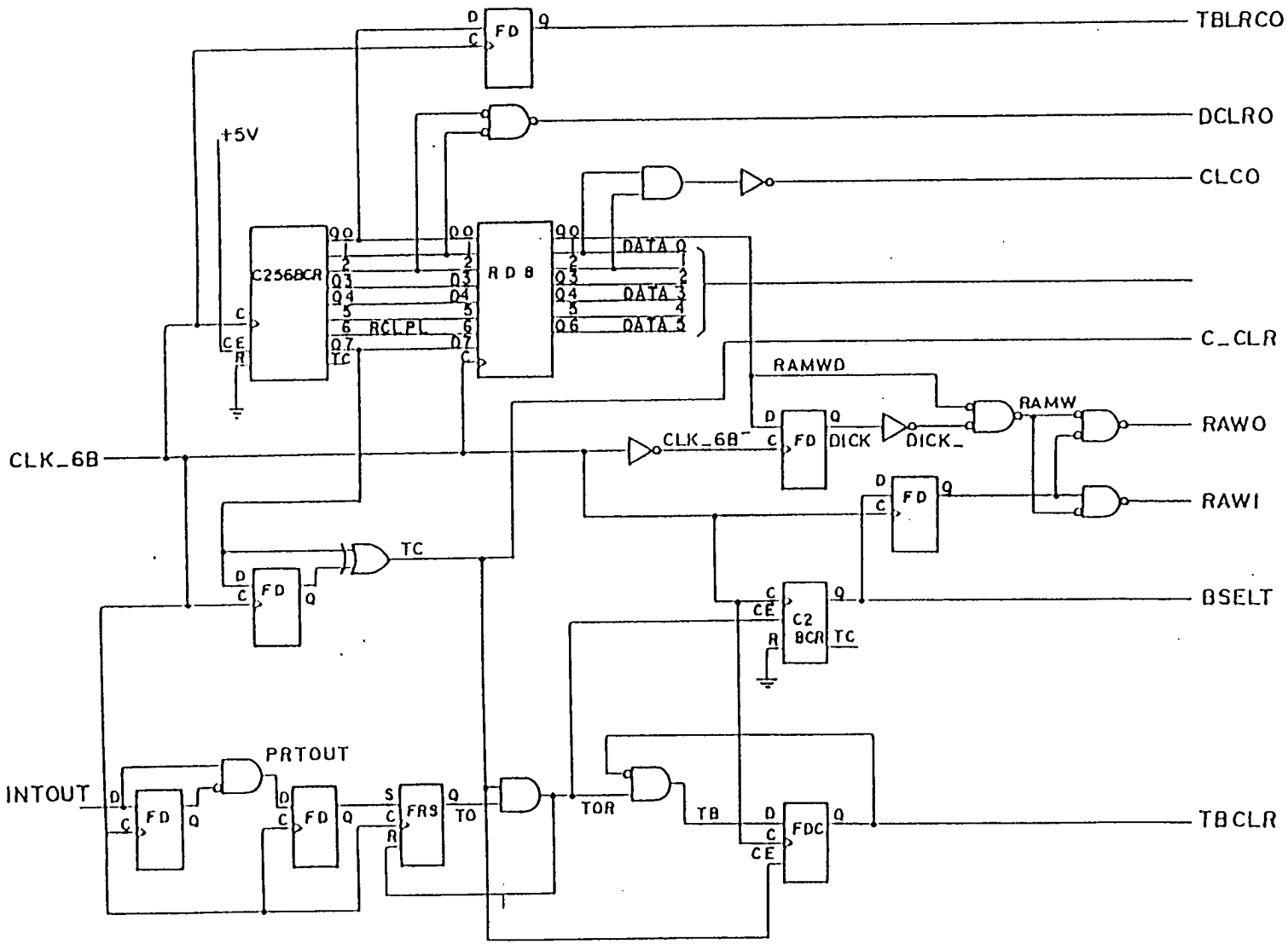

TBLRCO
DCLRO
CLCO
C_CLR
RAWO
RAWI
BSELT
TBCLR
+5V
CLK_68
C2568CR
RDB
RCLPL
DATA 0
DATA 1
DATA 3
RAMWD
RAMW
CLK_68
DICK
DICK_
TC
PRTOUT
INTOUT
FRS
TO
TOR
TB
C2 BCR
FDC
FD

FIG. 823

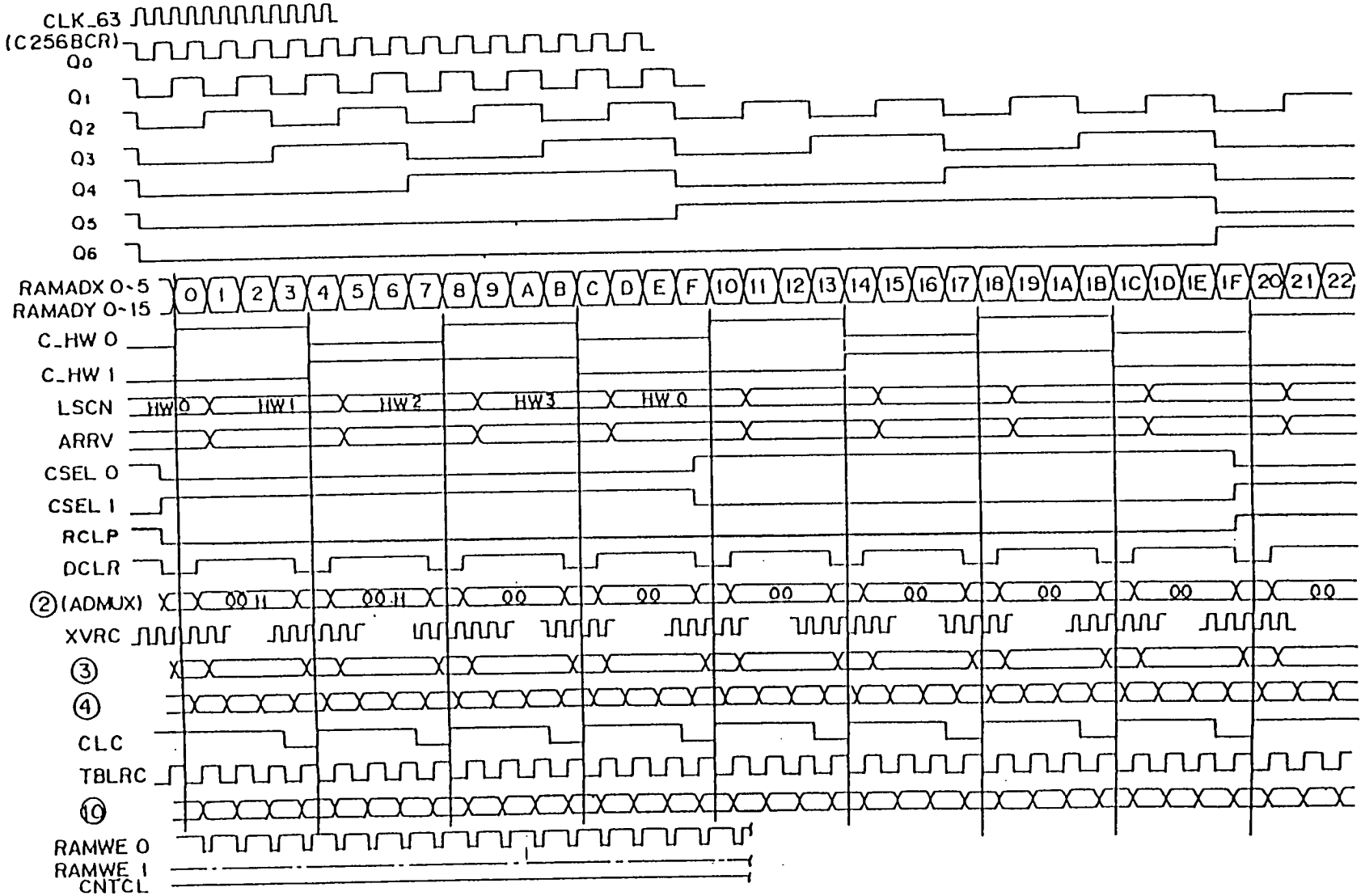

CLK_63
(C256BCR)
Q0
Q1
Q2
Q3
Q4
Q5
Q6
RAMADX 0~5
RAMADY 0~15
0 1 2 3 4 5 6 7 8 9 A B C D E F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22
C_HW 0
C_HW 1
LSCN
HW0
HW1
HW2
HW3
HW0
ARRV
CSEL 0
CSEL 1
RCLP
DCLR
② (ADMUX)
00 11
00 11
00
00
00
00
00
00
00
00
XVRC
③
④
CLC
TBLRC
⑩
RAMWE 0
RAMWE 1
CNTCL

FIG. 824

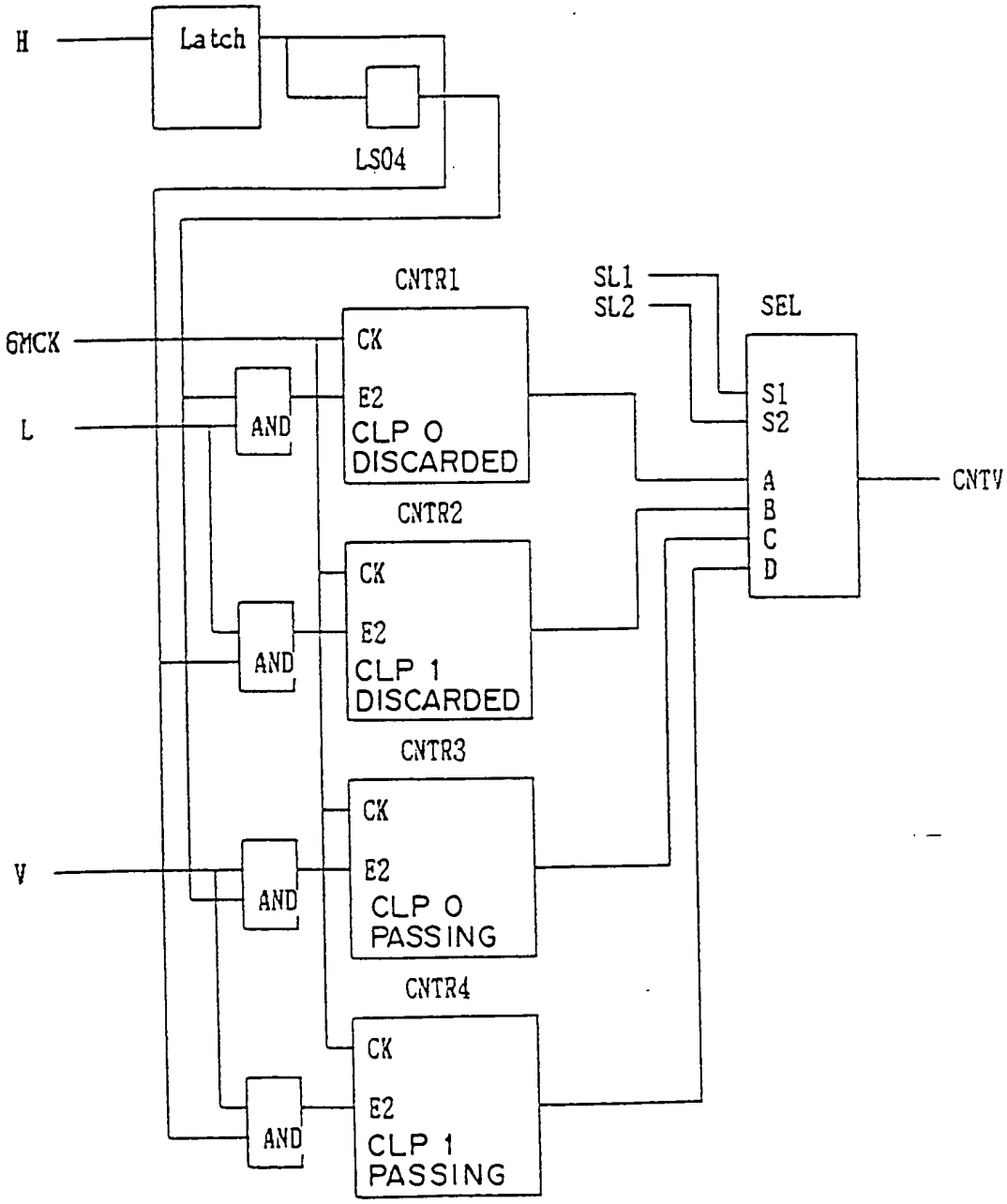

H
Latch
LS04
6MCK
L
V
AND
AND
AND
AND
CNTR1
CK
E2
CLP 0
DISCARDED
CNTR2
CK
E2
CLP 1
DISCARDED
CNTR3
CK
E2
CLP 0
PASSING
CNTR4
CK
E2
CLP 1
PASSING
SL1
SL2
SEL
S1
S2
A
B
C
D
CNTV

FIG. 825

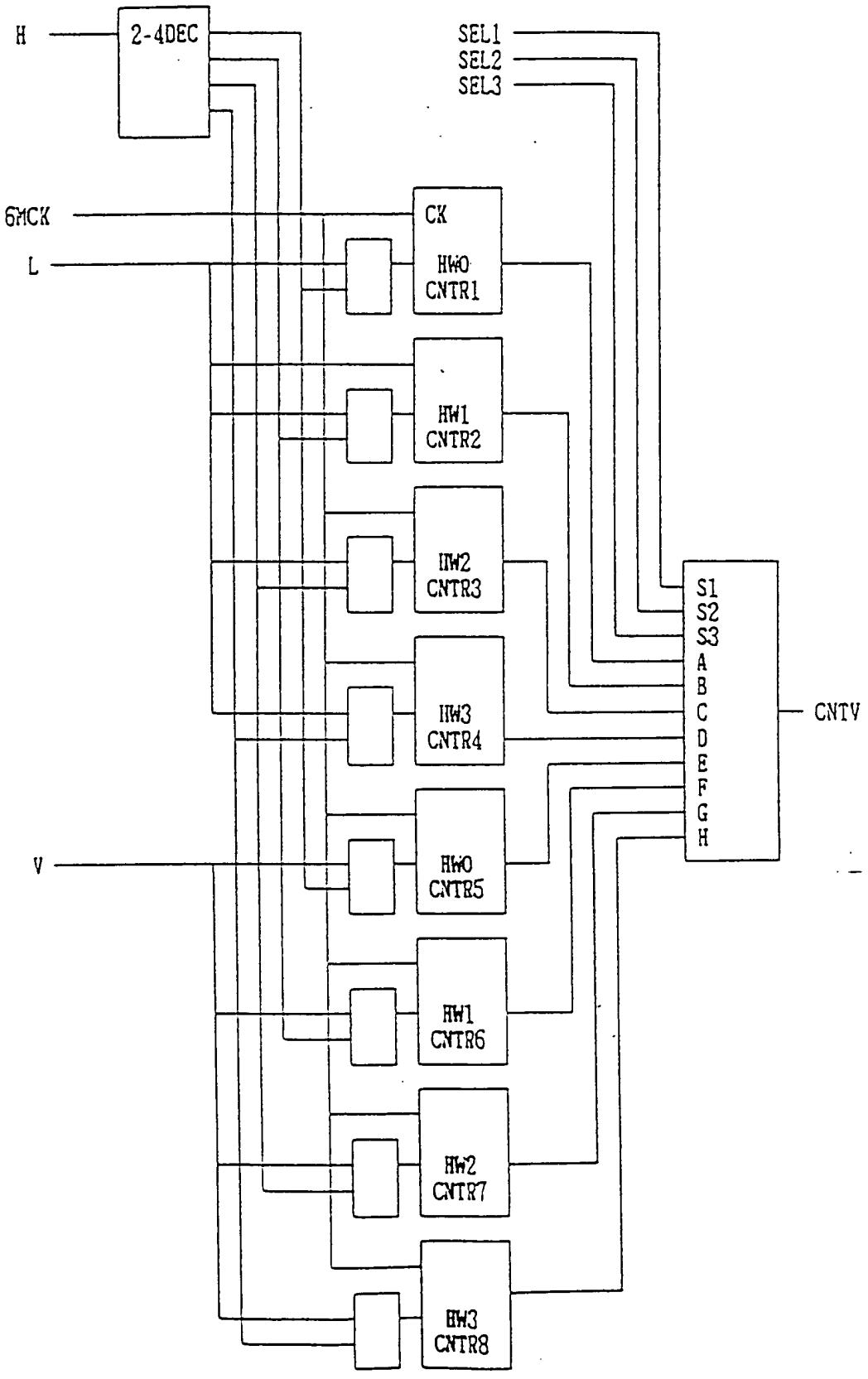

H
2-4DEC
SEL1
SEL2
SEL3
6MCK
CK
L
HW0
CNTR1
HW1
CNTR2
HW2
CNTR3
HW3
CNTR4
S1
S2
S3
A
B
C
D
E
F
G
H
CNTV
V
HW0
CNTR5
HW1
CNTR6
HW2
CNTR7
HW3
CNTR8

FIG. 826

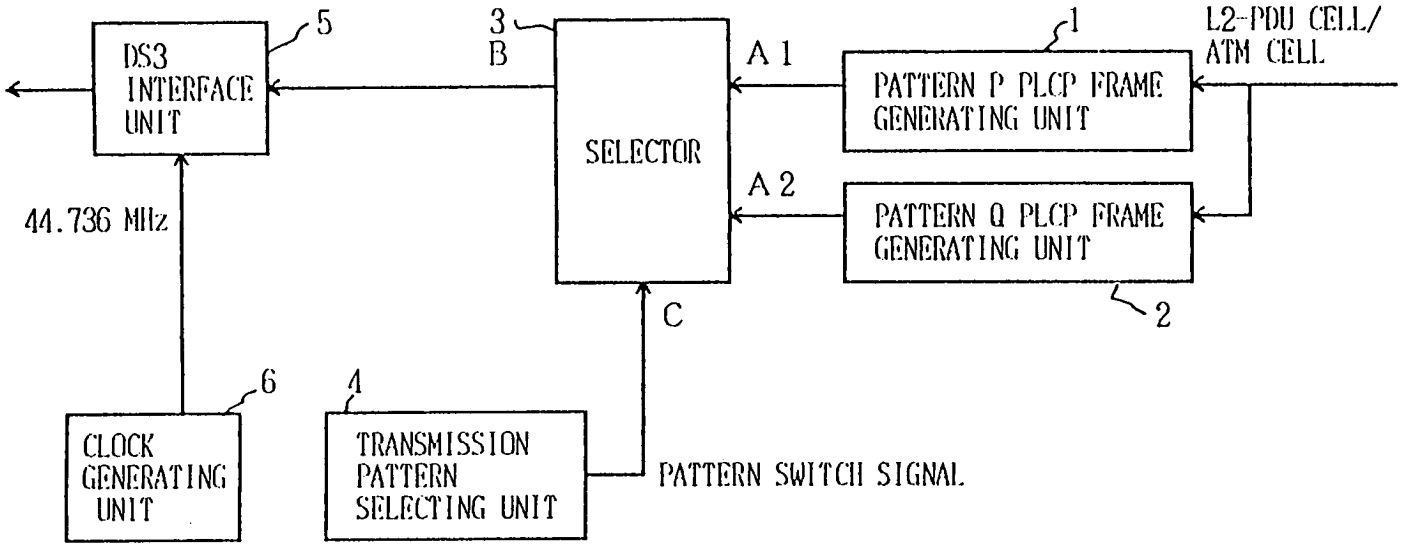

DS3
INTERFACE
UNIT
5
3
B
SELECTOR
A 1
A 2
1
PATTERN P PLCP FRAME
GENERATING UNIT
PATTERN Q PLCP FRAME
GENERATING UNIT
2
L2-PDU CELL/
ATM CELL
C
44.736 MHz
6
CLOCK
GENERATING
UNIT
4
TRANSMISSION
PATTERN
SELECTING UNIT
PATTERN SWITCH SIGNAL

FIG. 827

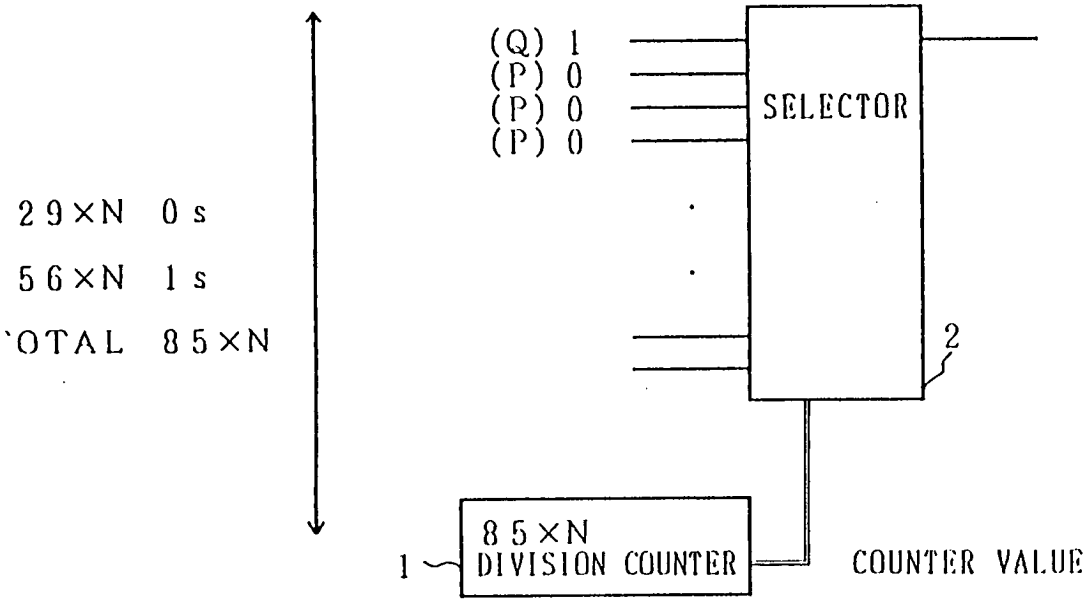

(Q) 1
(P) 0
(P) 0
(P) 0
SELECTOR
2
29×N 0s
56×N 1s
TOTAL 85×N
1
85×N
DIVISION COUNTER
COUNTER VALUE

FIG. 828

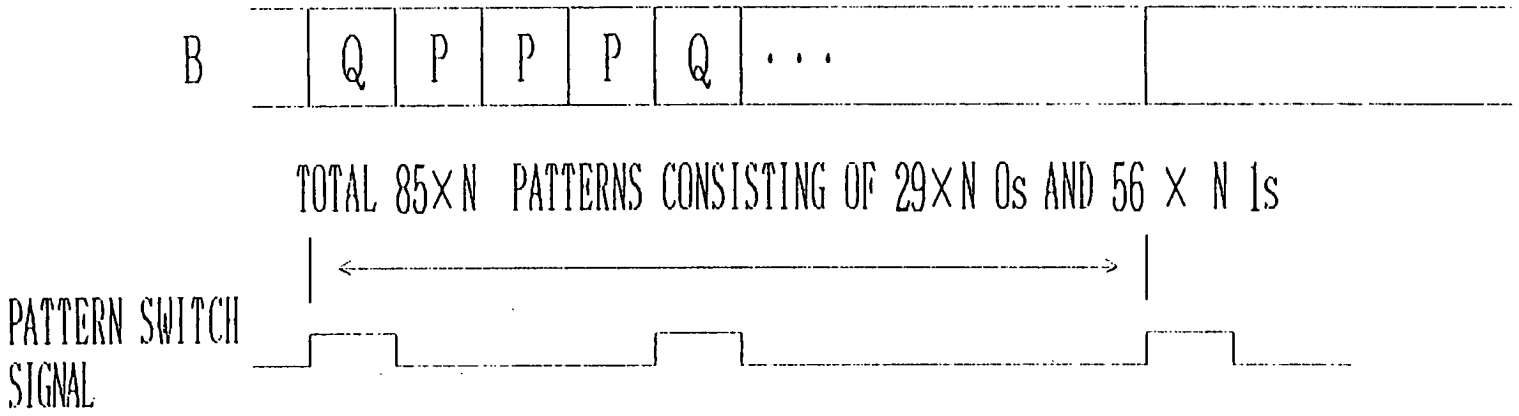

B
Q
P
P
P
Q
• • •
TOTAL 85×N PATTERNS CONSISTING OF 29×N 0s AND 56 × N 1s
PATTERN SWITCH SIGNAL

FIG. 829

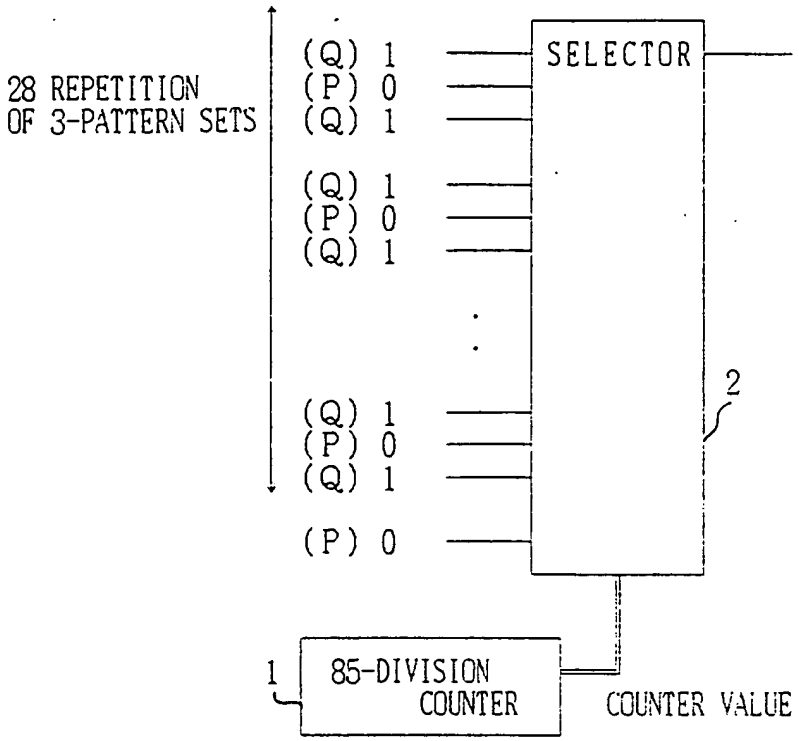

28 REPETITION
OF 3-PATTERN SETS
(Q) 1
(P) 0
(Q) 1
(Q) 1
(P) 0
(Q) 1
(Q) 1
(P) 0
(Q) 1
(P) 0
SELECTOR
2
1
85-DIVISION
COUNTER
COUNTER VALUE

FIG. 830

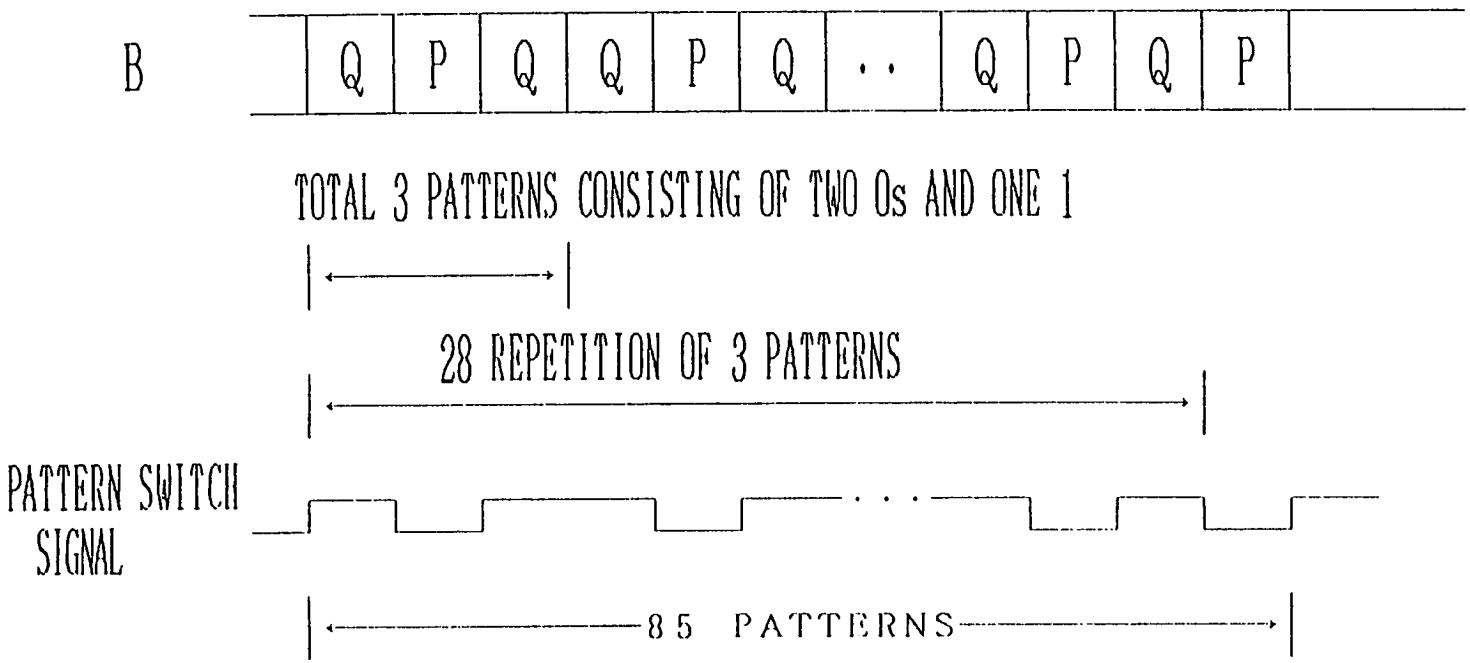

B
Q
P
Q
Q
P
Q
Q
P
Q
P
TOTAL 3 PATTERNS CONSISTING OF TWO 0s AND ONE 1
28 REPETITION OF 3 PATTERNS
PATTERN SWITCH SIGNAL
85 PATTERNS

FIG. 831

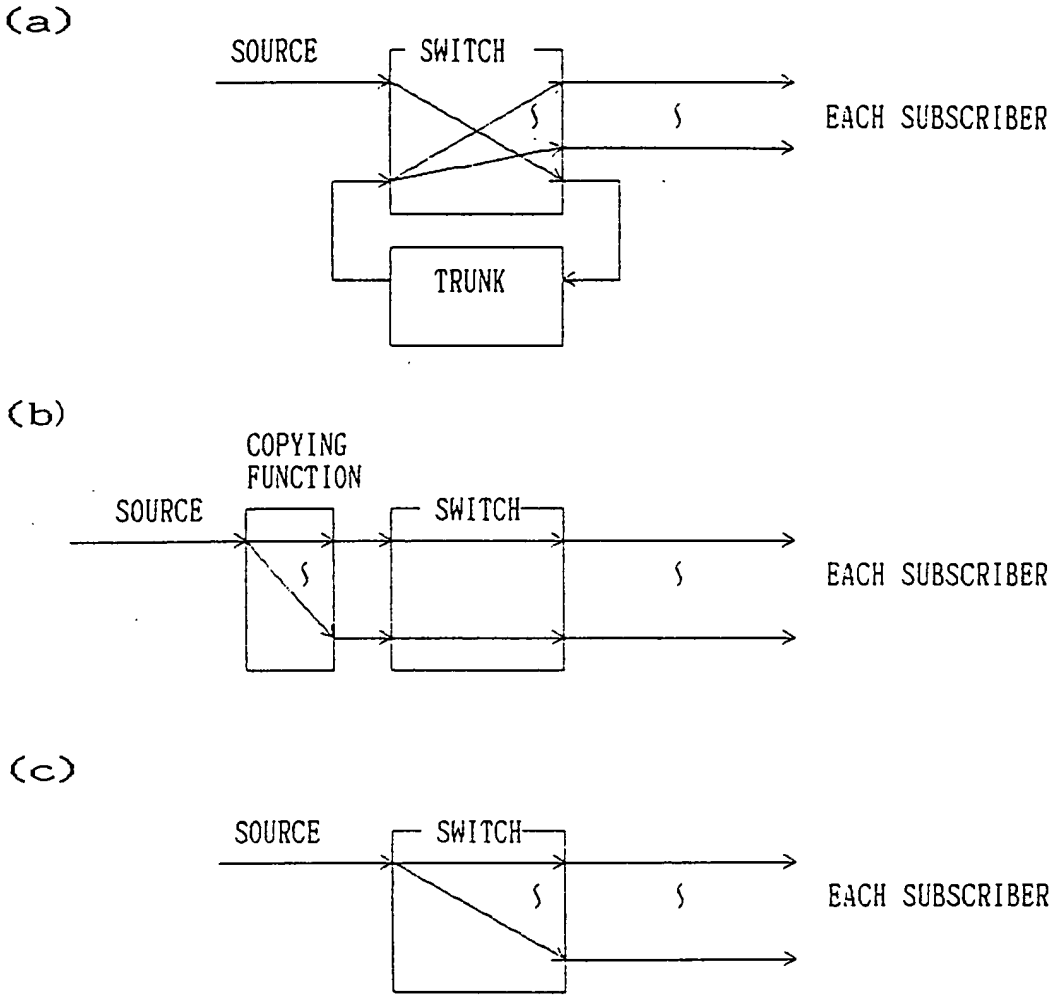

(a)
SOURCE
SWITCH
EACH SUBSCRIBER
TRUNK
(b)
COPYING
FUNCTION
SOURCE
SWITCH
EACH SUBSCRIBER
(c)
SOURCE
SWITCH
EACH SUBSCRIBER

FIG. 832

SYSTEM	MERITS	DEMERITS
TRUNK SYSTEM	· EASY TO CONTROL SWITCHES ONLY POINT-TO-POINT CONNECTION · REASSIGNMENT OF VPI/VCI IS NOT REQUIRED	· TRUNK IS REQUIRED · NUMBER OF PATHS DEPENDS ON CAPACITY OF TRUNK · BAND OF PATH SUPPORTED BY SYSTEM DECREASES FOR TRUNKS · DOUBLE DELAY OVER POINT-TO-POINT CONNECTION BECAUSE OF TEMPORARY ACCOMMODATION IN TRUNK
INPUT COPY SYSTEM	· EASY TO CONTROL SWITCHES ONLY POINT-TO-POINT CONNECTION	· REASSIGNMENT OF VPI/VCI IS REQUIED · COPYING FUNCTION SHOULD BE ADDED · BAND OF PATH SUPPORTED BY SYSTEM DECREASES FOR COPY IN PREVIOUS STEP
INTERNAL COPY SYSTEM	· BAND OF PATH SUPPORTED BY SYSTEM IS ALLOWED FOR MAXIMUM CAPACITY OF SYSTEM	· REASSIGNMENT OF VPI/VCI IS REQUIRED · COPYING FUNCTION SHOULD BE INCORPORATED. · COMPLICATED SWITCH CONTROL

FIG. 833

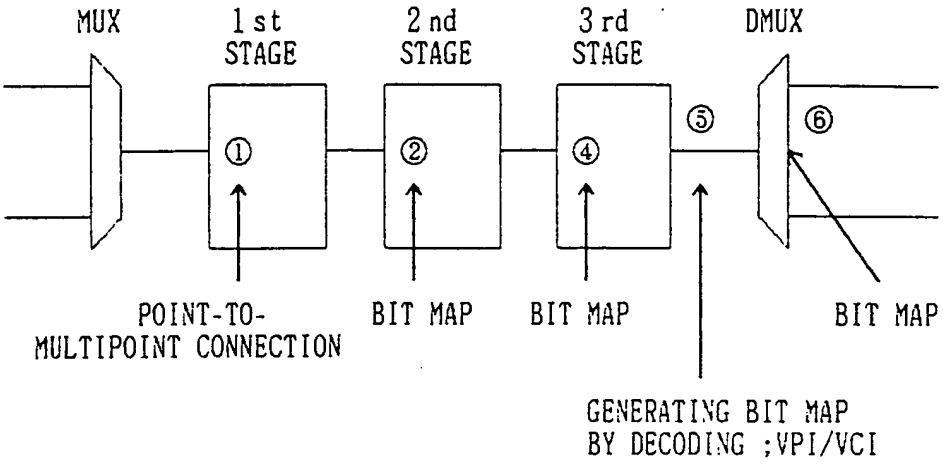

MUX
1 st STAGE
2 nd STAGE
3 rd STAGE
DMUX
①
②
④
⑤
⑥
POINT-TO-MULTIPOINT CONNECTION
BIT MAP
BIT MAP
BIT MAP
GENERATING BIT MAP BY DECODING ;VPI/VCI

FIG. 834

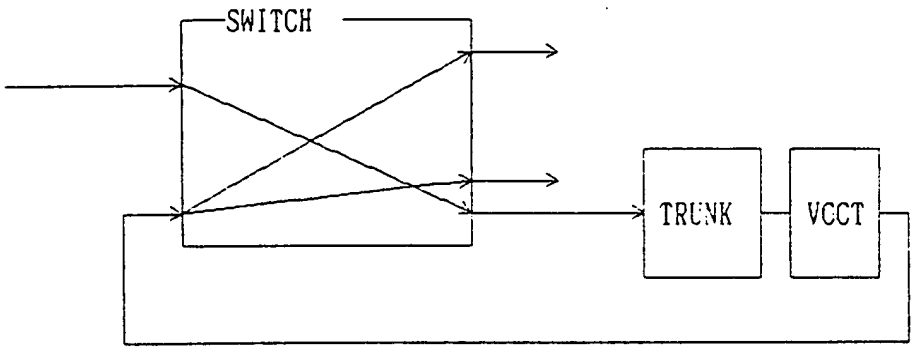


FIG. 835

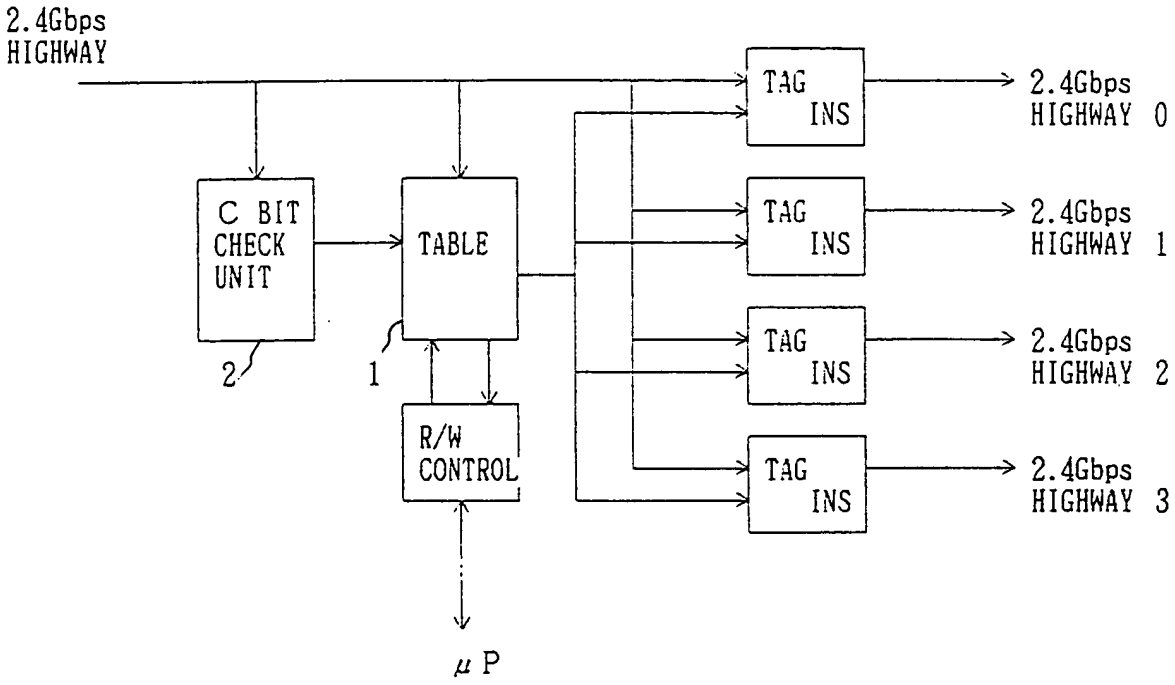

2.4Gbps
HIGHWAY
C BIT
CHECK
UNIT
TABLE
R/W
CONTROL
μP
1
2
TAG
INS
TAG
INS
TAG
INS
TAG
INS
2.4Gbps
HIGHWAY 0
2.4Gbps
HIGHWAY 1
2.4Gbps
HIGHWAY 2
2.4Gbps
HIGHWAY 3

FIG. 836

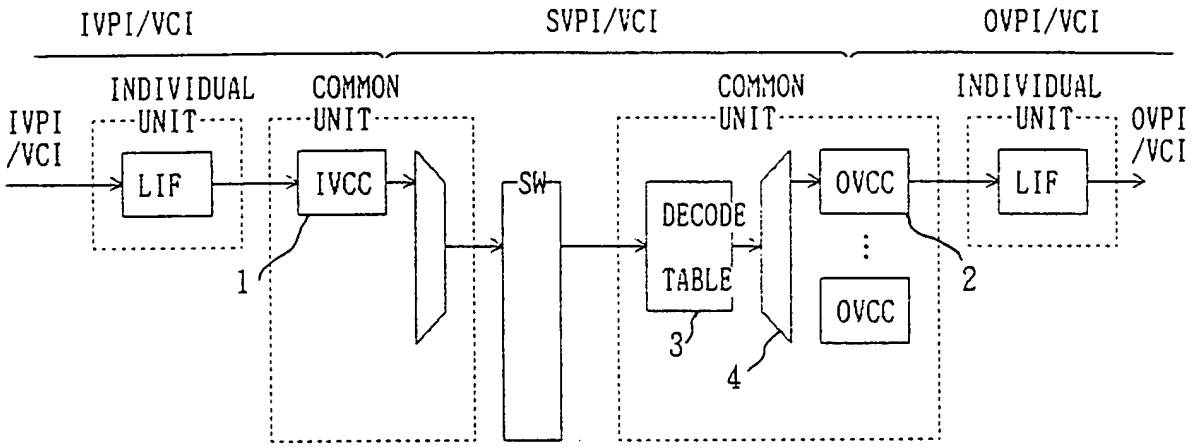

IVPI/VCI
SVPI/VCI
OVPI/VCI
INDIVIDUAL UNIT
COMMON UNIT
COMMON UNIT
INDIVIDUAL UNIT
IVPI /VCI
LIF
IVCC
SW
DECODE TABLE
OVCC
OVCC
LIF
OVPI /VCI
1
2
3
4

FIG. 837

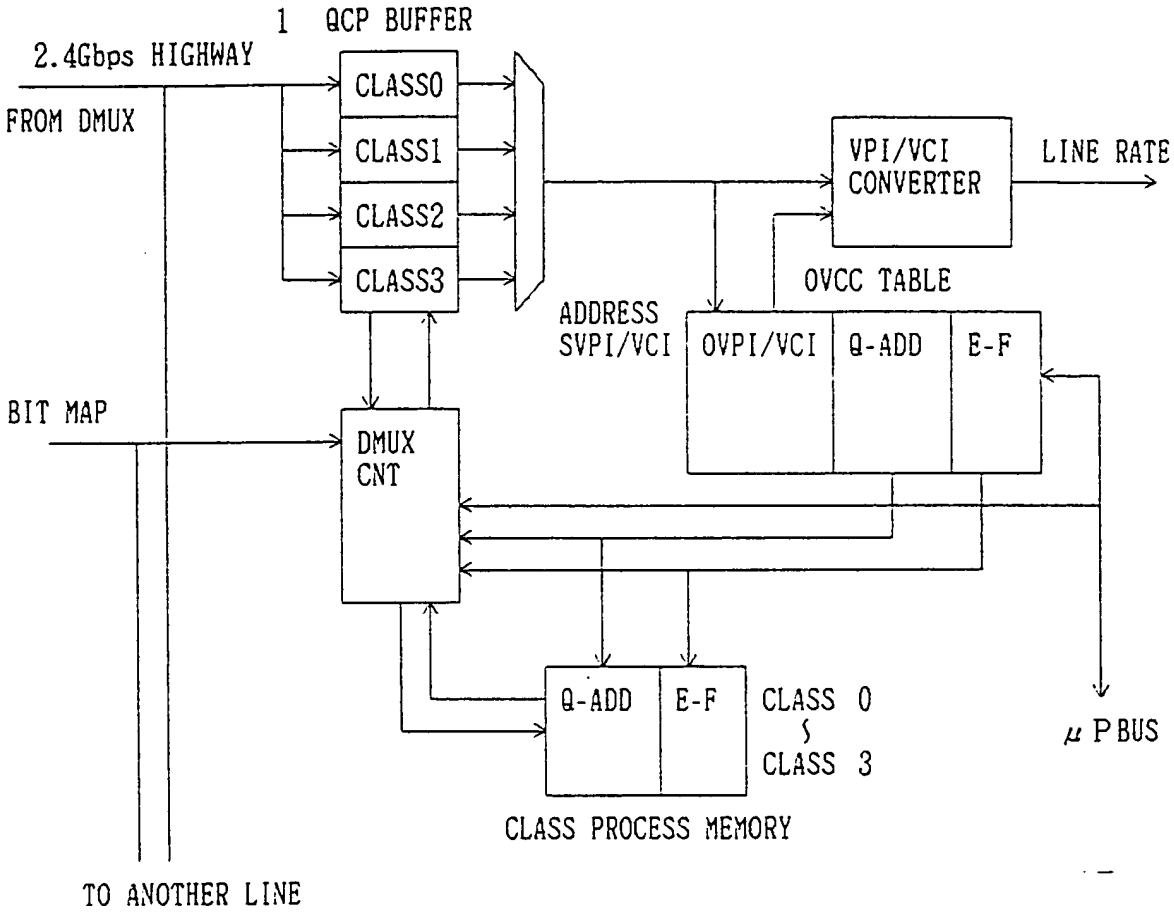

1 QCP BUFFER
2.4Gbps HIGHWAY
FROM DMUX
CLASS0
CLASS1
CLASS2
CLASS3
VPI/VCI CONVERTER
LINE RATE
OVCC TABLE
ADDRESS SVPI/VCI
OVPI/VCI
Q-ADD
E-F
BIT MAP
DMUX CNT
Q-ADD
E-F
CLASS 0
CLASS 3
μP BUS
CLASS PROCESS MEMORY
TO ANOTHER LINE

FIG. 838

	ADDRESS	CONTENTS OF OVCC TABLE OVPI/VCI	Q-ADD	E-F
POINT-TO POINT CONNECTION	SVPI/VCI	OVPI/VCI	D.C.	1
POINT-TO-MULTIPOINT CONNECTION	SVPI/VCI	OVPI/VCI	ADDRESS	x

FIG. 839

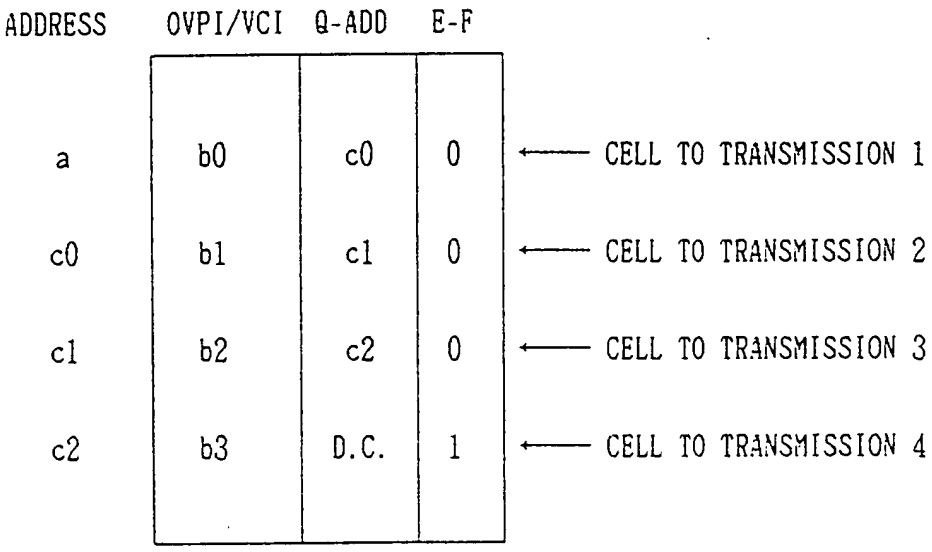

ADDRESS
OVPI/VCI
Q-ADD
E-F
a
b0
c0
0
CELL TO TRANSMISSION 1
c0
b1
c1
0
CELL TO TRANSMISSION 2
c1
b2
c2
0
CELL TO TRANSMISSION 3
c2
b3
D.C.
1
CELL TO TRANSMISSION 4

FIG. 840

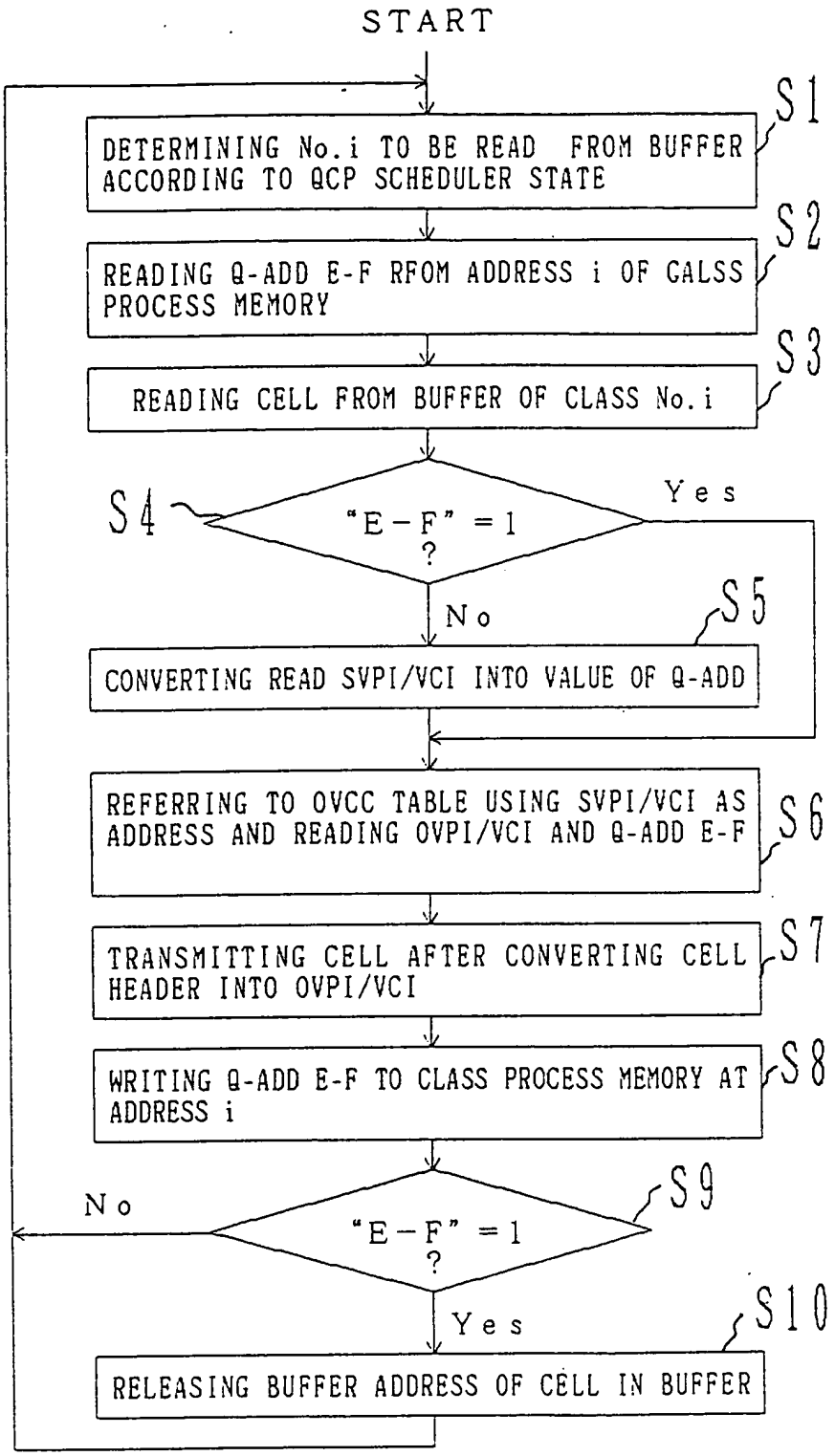

START
DETERMINING No.i TO BE READ FROM BUFFER ACCORDING TO QCP SCHEDULER STATE
S1
READING Q-ADD E-F RFOM ADDRESS i OF CALSS PROCESS MEMORY
S2
READING CELL FROM BUFFER OF CLASS No.i
S3
S4
"E-F" =1 ?
Yes
No
S5
CONVERTING READ SVPI/VCI INTO VALUE OF Q-ADD
REFERRING TO OVCC TABLE USING SVPI/VCI AS ADDRESS AND READING OVPI/VCI AND Q-ADD E-F
S6
TRANSMITTING CELL AFTER CONVERTING CELL HEADER INTO OVPI/VCI
S7
WRITING Q-ADD E-F TO CLASS PROCESS MEMORY AT ADDRESS i
S8
No
"E-F" =1 ?
S9
Yes
S10
RELEASING BUFFER ADDRESS OF CELL IN BUFFER

FIG. 841

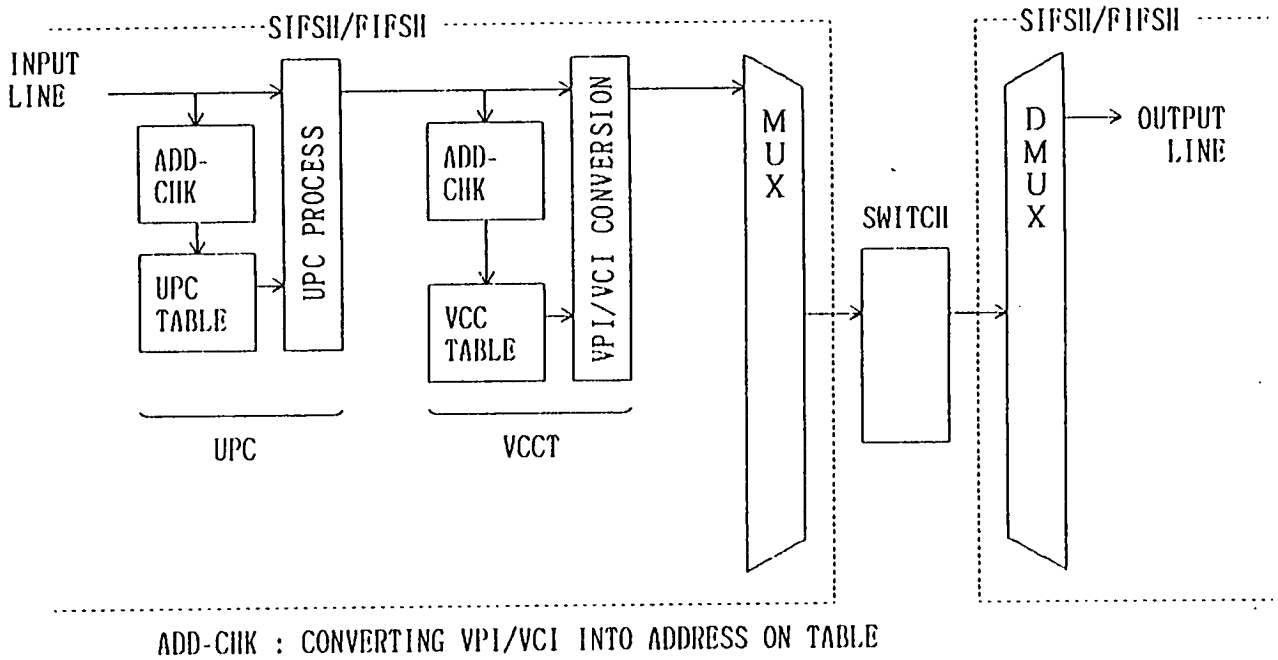
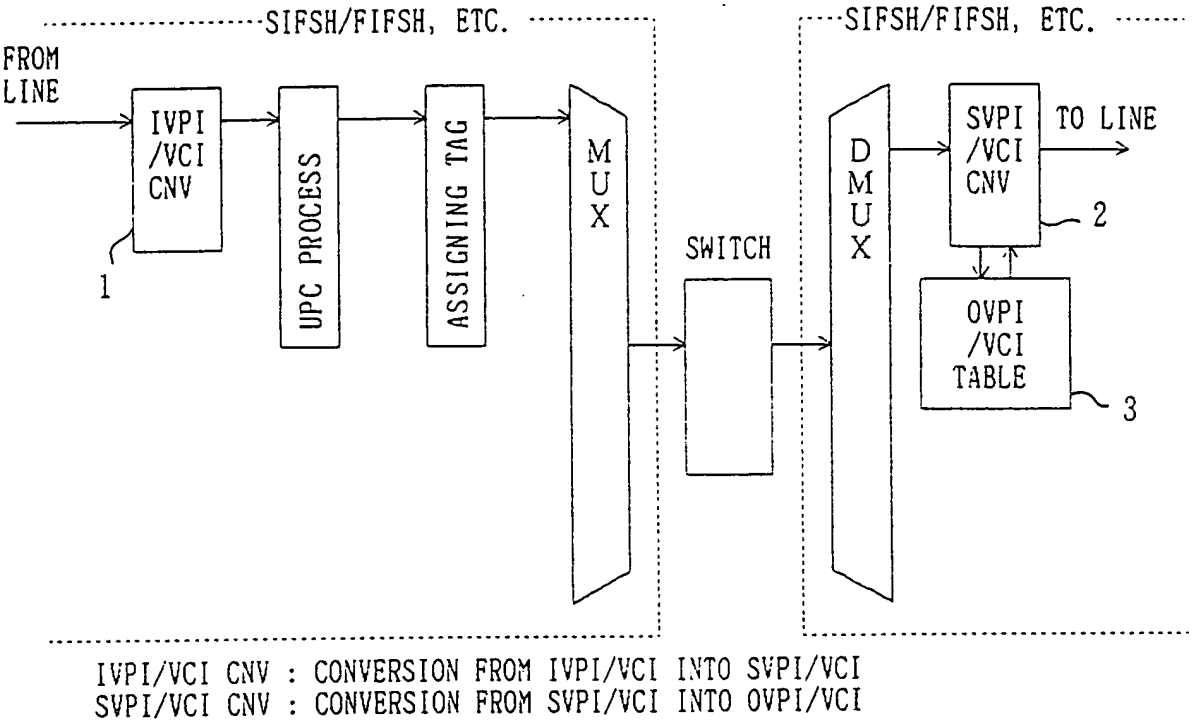

SIFSH/FIFSH
INPUT LINE
ADD-CHK
UPC TABLE
UPC PROCESS
UPC
ADD-CHK
VCC TABLE
VPI/VCI CONVERSION
VCCT
MUX
SWITCH
SIFSH/FIFSH
DMUX
OUTPUT LINE
ADD-CHK : CONVERTING VPI/VCI INTO ADDRESS ON TABLE

FIG. 842


SIFSH/FIFSH, ETC.
SIFSH/FIFSH, ETC.
FROM LINE
IVPI /VCI CNV
1
UPC PROCESS
ASSIGNING TAG
M U X
SWITCH
D M U X
SVPI /VCI CNV
TO LINE
2
OVPI /VCI TABLE
3
IVPI/VCI CNV : CONVERSION FROM IVPI/VCI INTO SVPI/VCI
SVPI/VCI CNV : CONVERSION FROM SVPI/VCI INTO OVPI/VCI

F I G. 8 4 3

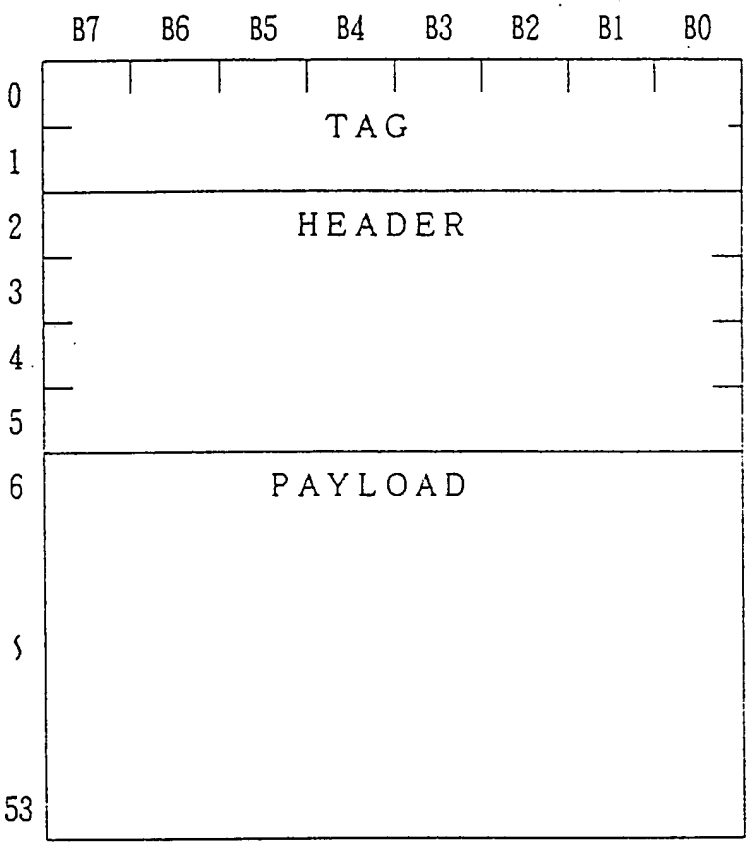


FIG. 844

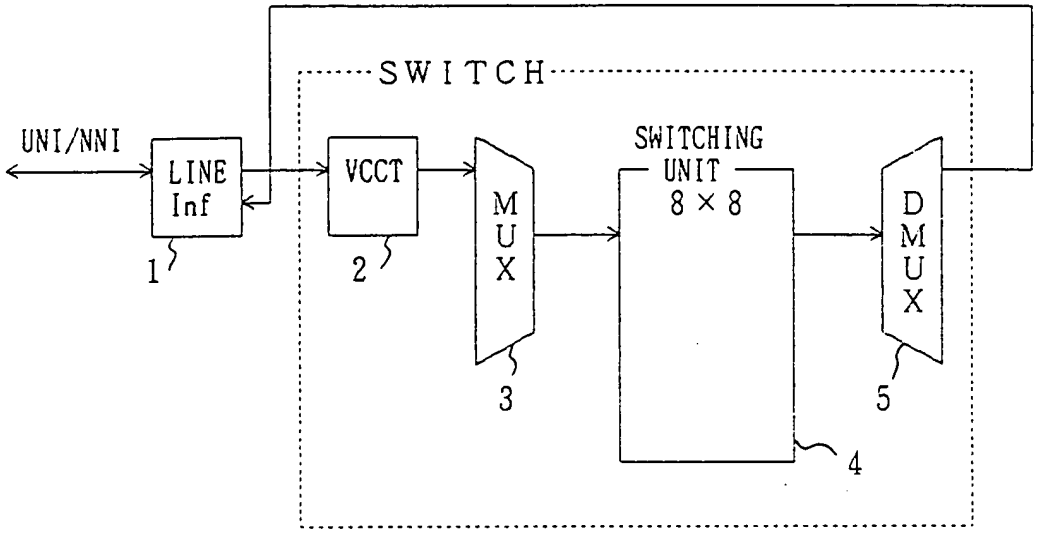

SWITCH
UNI/NNI
LINE
Inf
1
VCCT
2
M
U
X
3
SWITCHING
UNIT
8 × 8
4
D
M
U
X
5

FIG. 845

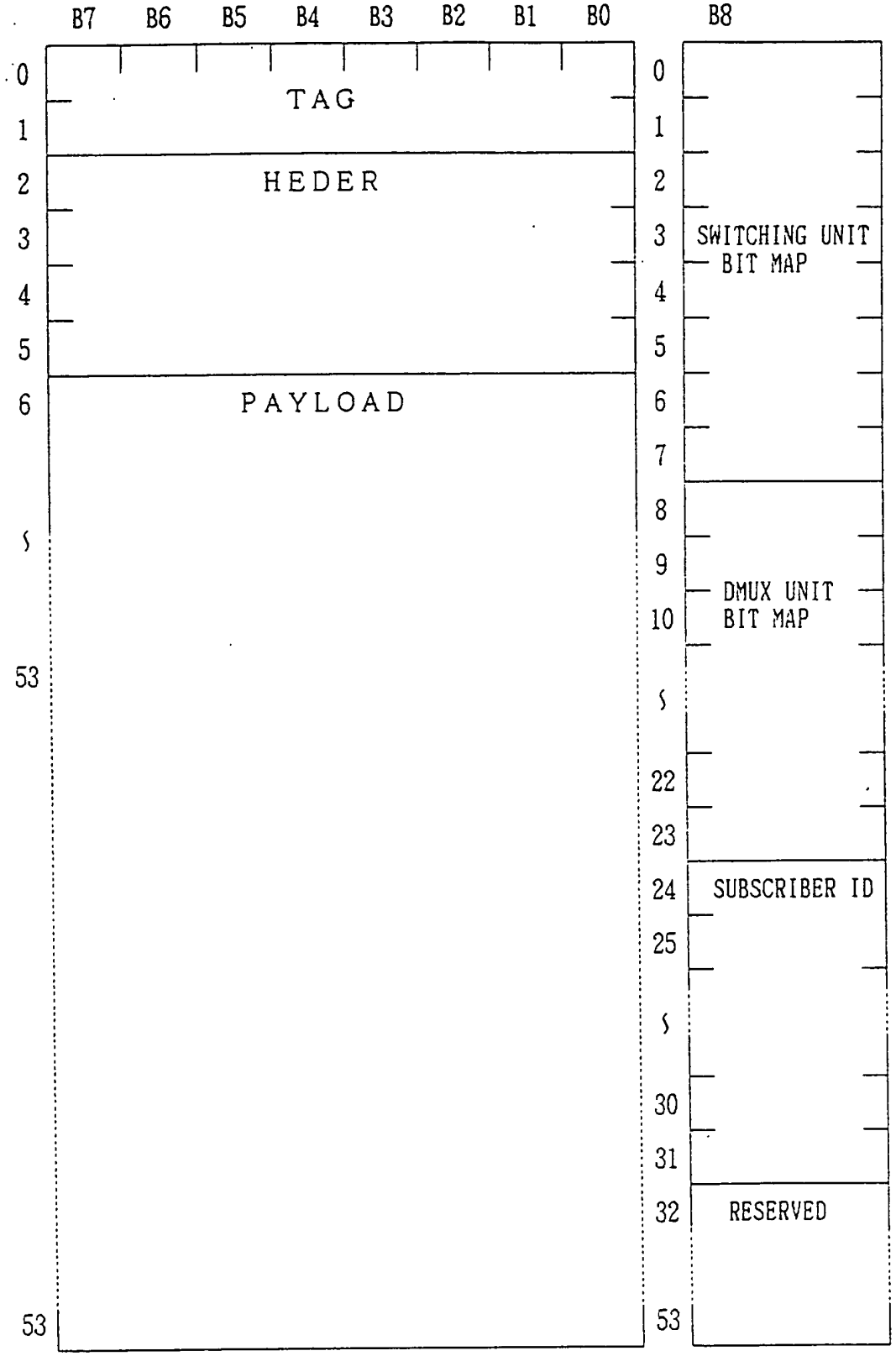
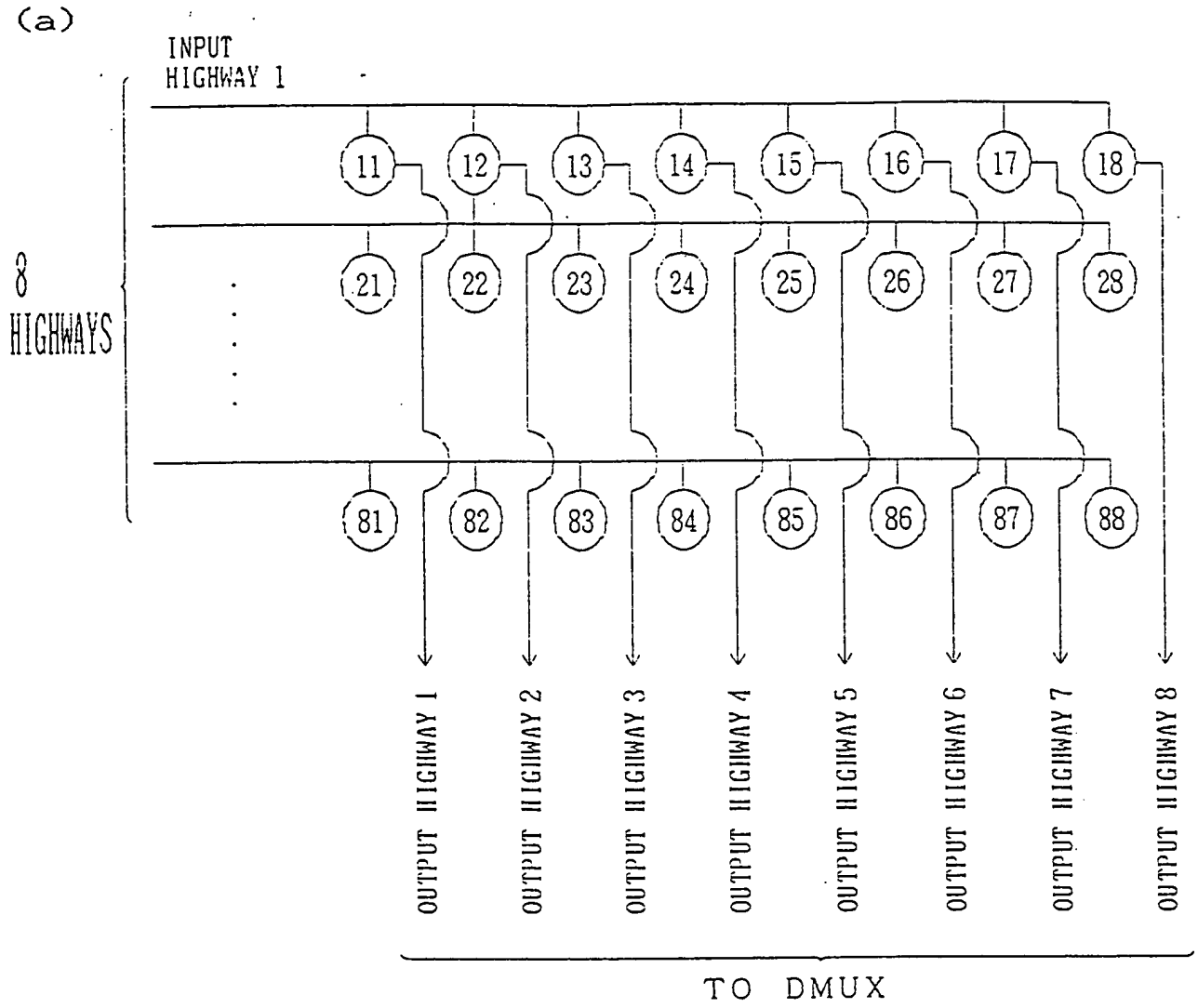

B7
B6
B5
B4
B3
B2
B1
B0
B8
TAG
HEDER
PAYLOAD
SWITCHING UNIT BIT MAP
DMUX UNIT BIT MAP
SUBSCRIBER ID
RESERVED
0
1
2
3
4
5
6
7
8
9
10
22
23
24
25
30
31
32
53

FIG. 846



(b)

0	1	1	0	1	1	0	0

SWITCHING UNIT BIT MAP

FIG. 847

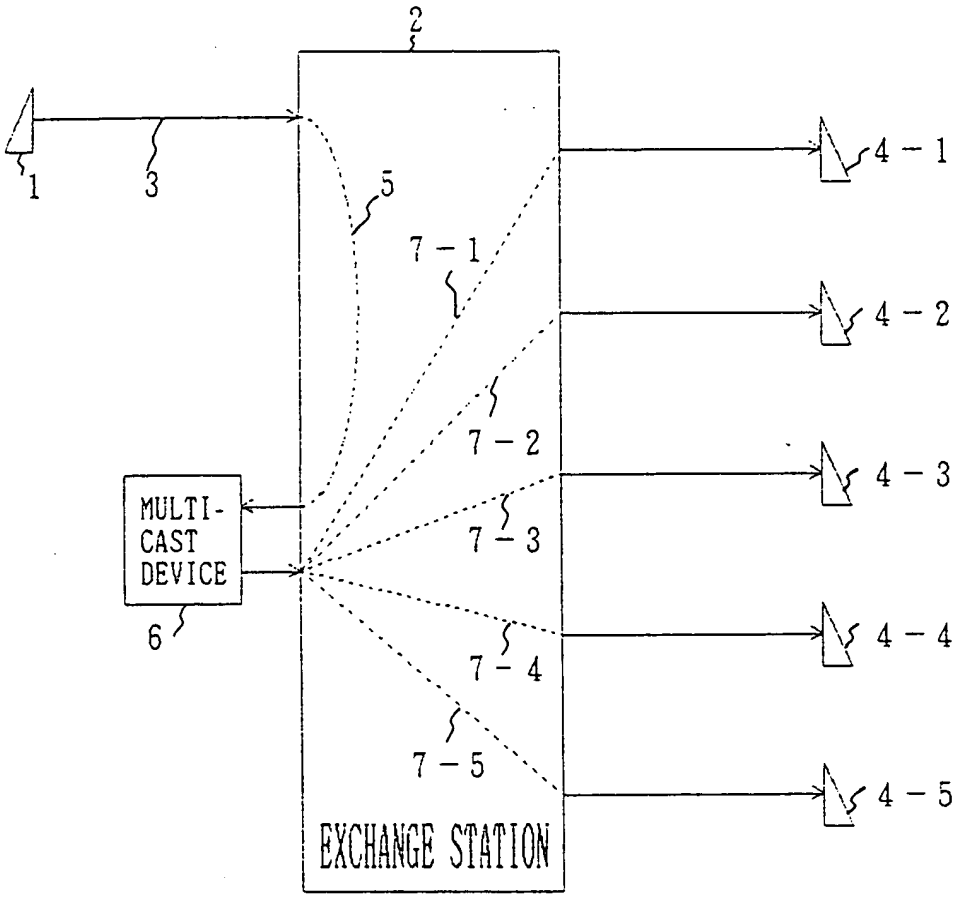

2
1
3
5
7 – 1
7 – 2
7 – 3
7 – 4
7 – 5
4 – 1
4 – 2
4 – 3
4 – 4
4 – 5
MULTI-
CAST
DEVICE
6
EXCHANGE STATION

FIG. 848

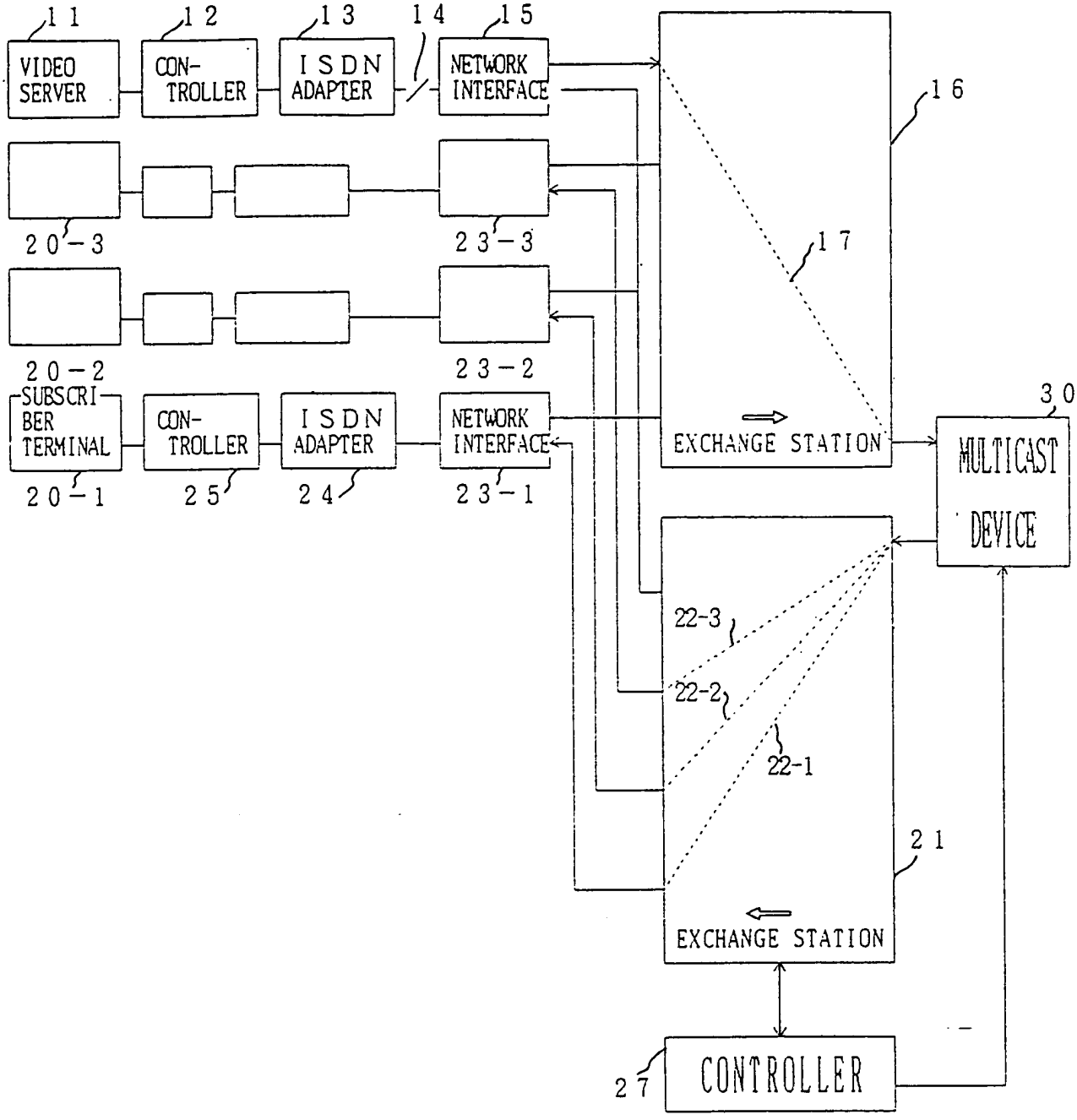

11
12
13
14
15
VIDEO SERVER
CON-TROLLER
ISDN ADAPTER
NETWORK INTERFACE
16
17
20-3
23-3
20-2
23-2
SUBSCRIBER TERMINAL
CON-TROLLER
ISDN ADAPTER
NETWORK INTERFACE
EXCHANGE STATION
30
MULTICAST DEVICE
20-1
25
24
23-1
22-3
22-2
22-1
21
EXCHANGE STATION
27
CONTROLLER

FIG. 849

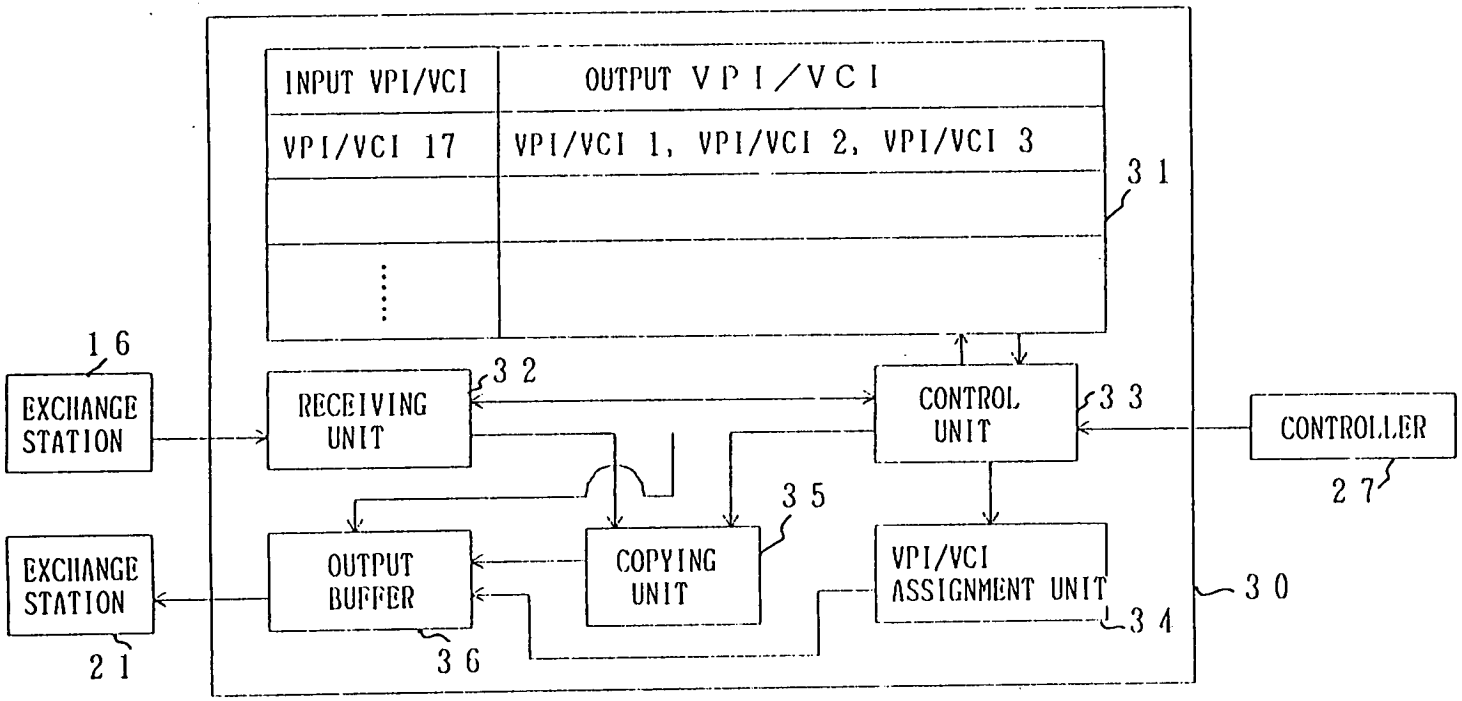
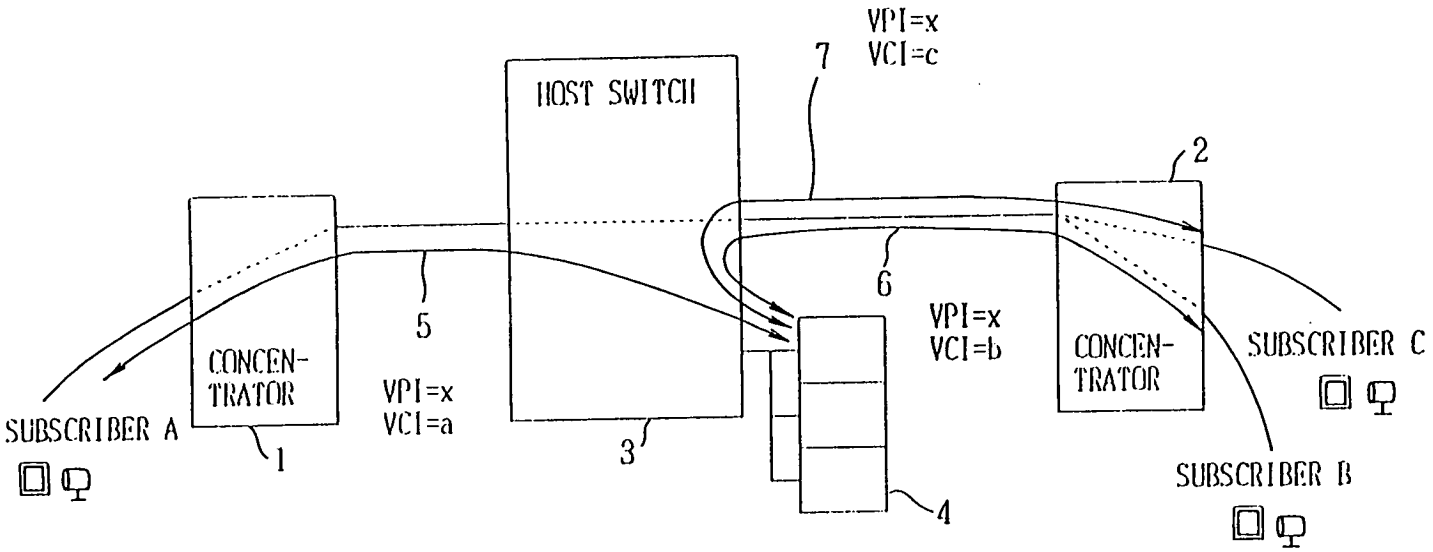

INPUT VPI/VCI
OUTPUT VPI/VCI
VPI/VCI 17
VPI/VCI 1, VPI/VCI 2, VPI/VCI 3
31
16
EXCHANGE STATION
RECEIVING UNIT
32
CONTROL UNIT
33
CONTROLLER
27
35
EXCHANGE STATION
21
OUTPUT BUFFER
36
COPYING UNIT
VPI/VCI ASSIGNMENT UNIT
34
30

FIG. 850



MULTIPLE SUBSCRIBER COMMUNICATIONS TRUNK
(IMAGE, VOICE MIXER)

FIG. 851

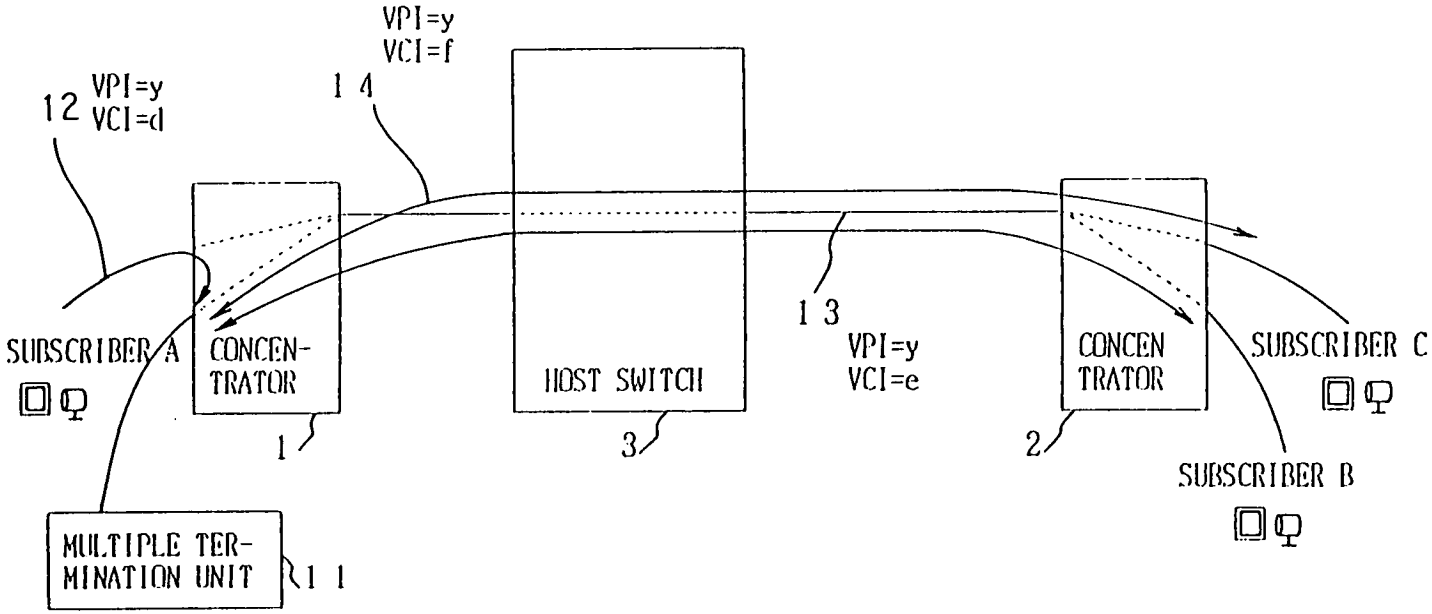

VPI=y
VCI=f
12 VPI=y
VCI=d
14
SUBSCRIBER A
CONCEN-
TRATOR
HOST SWITCH
13
VPI=y
VCI=e
CONCEN
TRATOR
SUBSCRIBER C
SUBSCRIBER B
1
3
2
MULTIPLE TER-
MINATION UNIT
11

FIG. 852

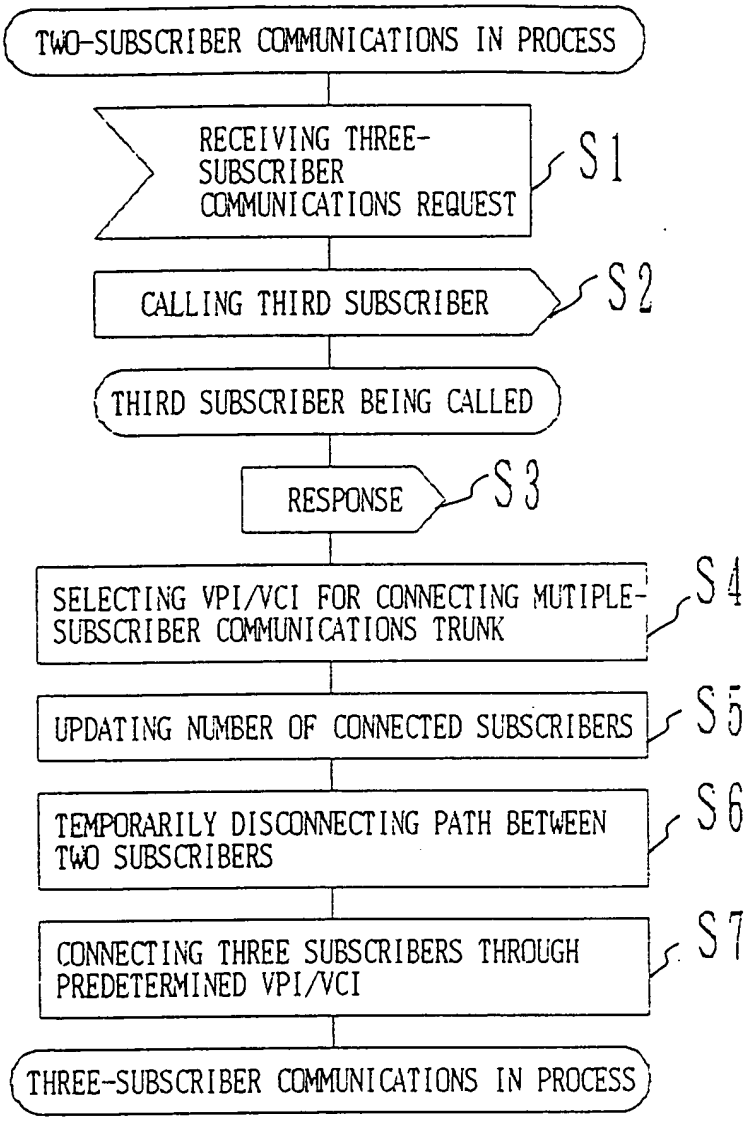

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
RECEIVING THREE-SUBSCRIBER COMMUNICATIONS REQUEST
S1
CALLING THIRD SUBSCRIBER
S2
THIRD SUBSCRIBER BEING CALLED
RESPONSE
S3
SELECTING VPI/VCI FOR CONNECTING MUTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S4
UPDATING NUMBER OF CONNECTED SUBSCRIBERS
S5
TEMPORARILY DISCONNECTING PATH BETWEEN TWO SUBSCRIBERS
S6
CONNECTING THREE SUBSCRIBERS THROUGH PREDETERMINED VPI/VCI
S7
THREE-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 853

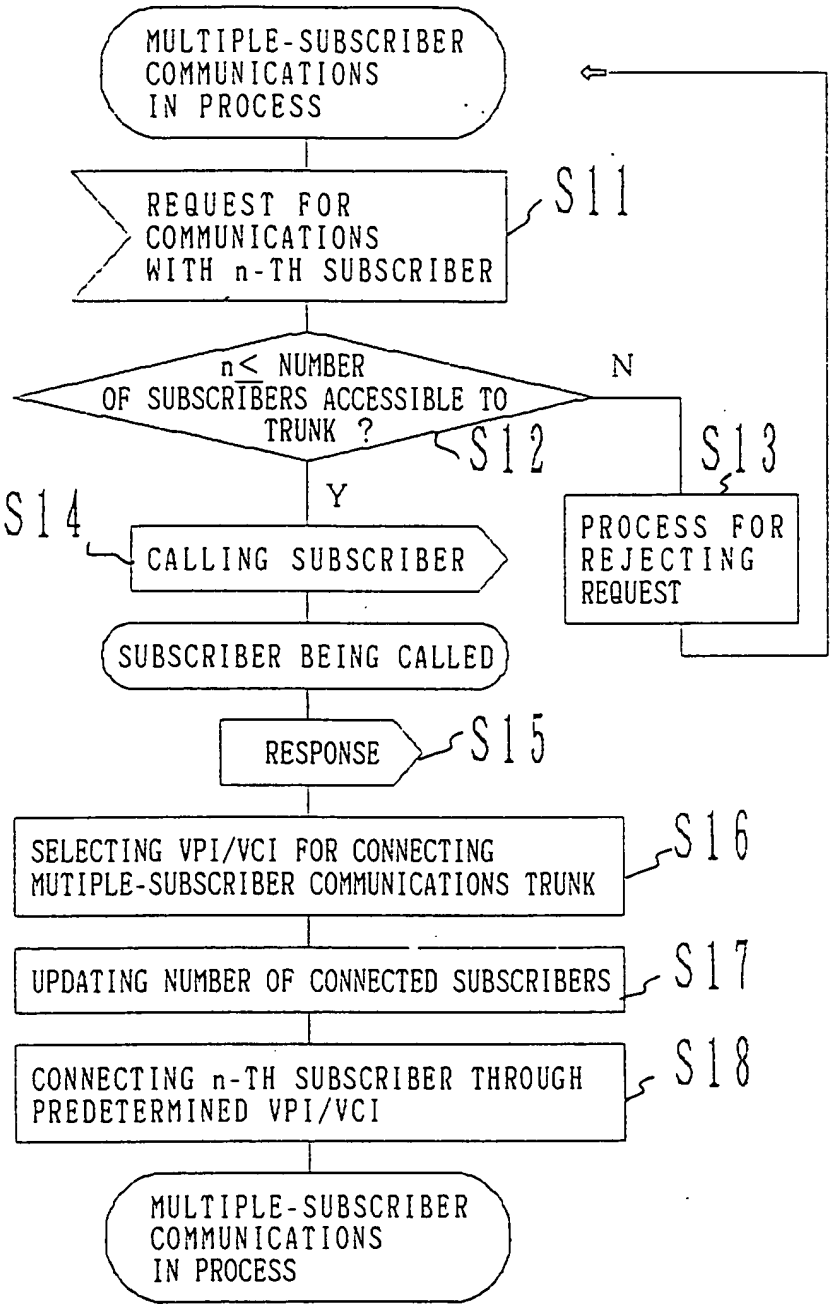

MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS
REQUEST FOR COMMUNICATIONS WITH n-TH SUBSCRIBER
S11
n≤ NUMBER OF SUBSCRIBERS ACCESSIBLE TO TRUNK ?
S12
N
S13
PROCESS FOR REJECTING REQUEST
Y
S14
CALLING SUBSCRIBER
SUBSCRIBER BEING CALLED
RESPONSE
S15
SELECTING VPI/VCI FOR CONNECTING MUTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S16
UPDATING NUMBER OF CONNECTED SUBSCRIBERS
S17
CONNECTING n-TH SUBSCRIBER THROUGH PREDETERMINED VPI/VCI
S18
MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 854

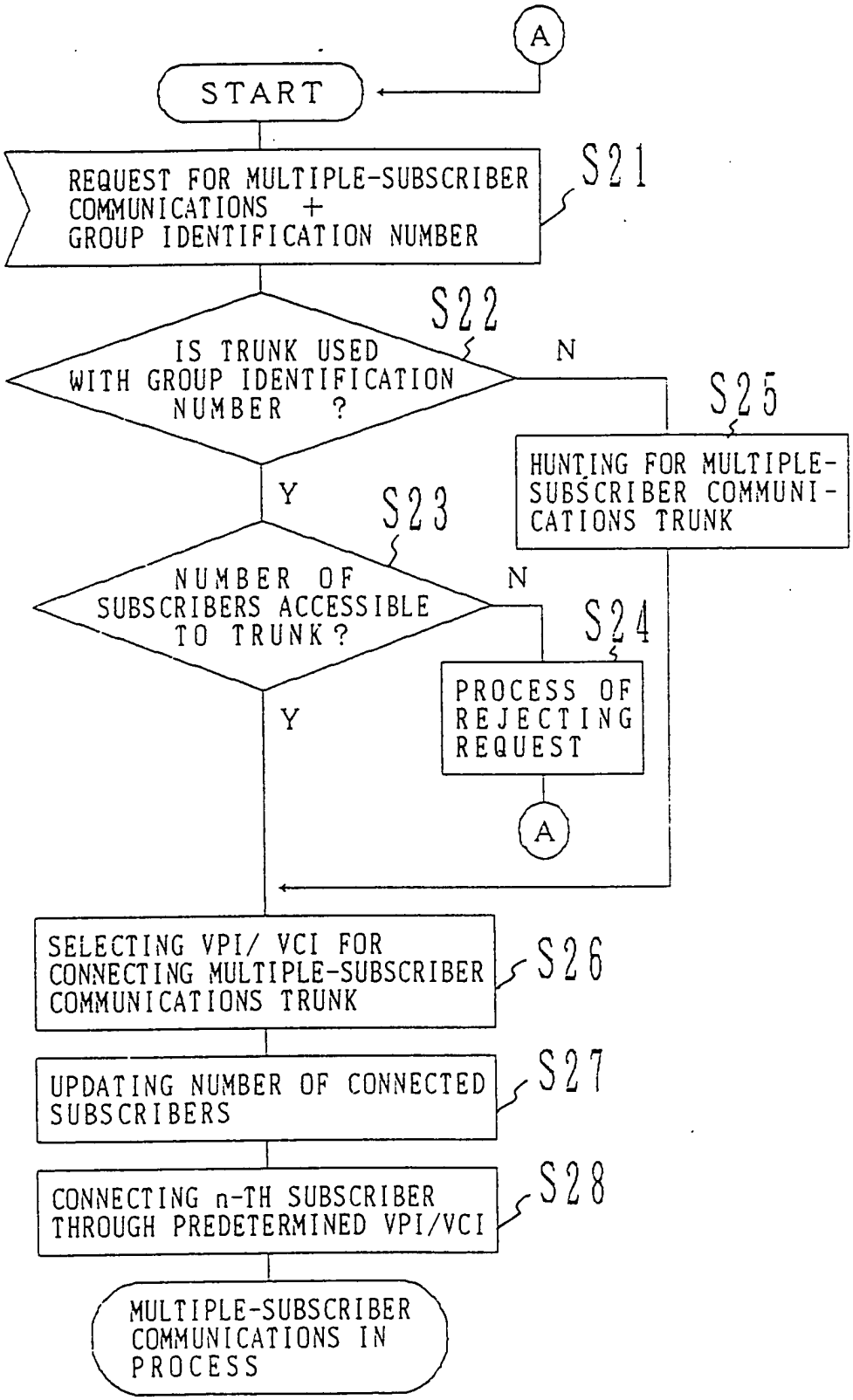

A
START
REQUEST FOR MULTIPLE-SUBSCRIBER COMMUNICATIONS + GROUP IDENTIFICATION NUMBER
S21
IS TRUNK USED WITH GROUP IDENTIFICATION NUMBER ?
S22
N
Y
S25
HUNTING FOR MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
NUMBER OF SUBSCRIBERS ACCESSIBLE TO TRUNK?
S23
N
Y
S24
PROCESS OF REJECTING REQUEST
A
SELECTING VPI/ VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S26
UPDATING NUMBER OF CONNECTED SUBSCRIBERS
S27
CONNECTING n-TH SUBSCRIBER THROUGH PREDETERMINED VPI/VCI
S28
MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 855

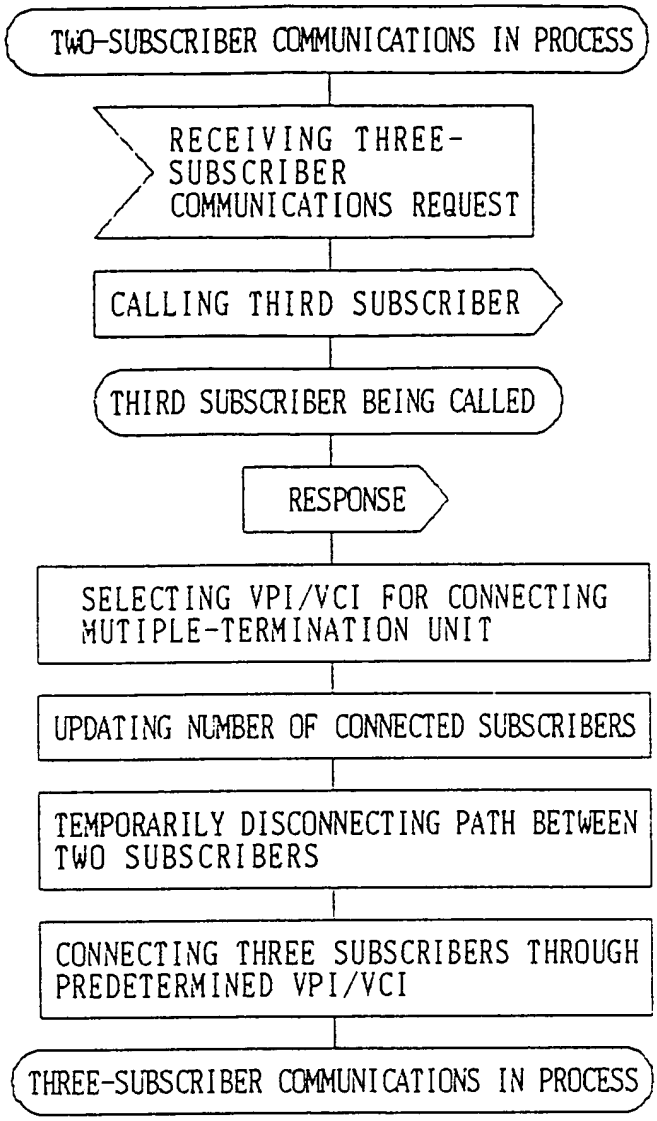

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
RECEIVING THREE-SUBSCRIBER COMMUNICATIONS REQUEST
CALLING THIRD SUBSCRIBER
THIRD SUBSCRIBER BEING CALLED
RESPONSE
SELECTING VPI/VCI FOR CONNECTING MUTIPLE-TERMINATION UNIT
UPDATING NUMBER OF CONNECTED SUBSCRIBERS
TEMPORARILY DISCONNECTING PATH BETWEEN TWO SUBSCRIBERS
CONNECTING THREE SUBSCRIBERS THROUGH PREDETERMINED VPI/VCI
THREE-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 856

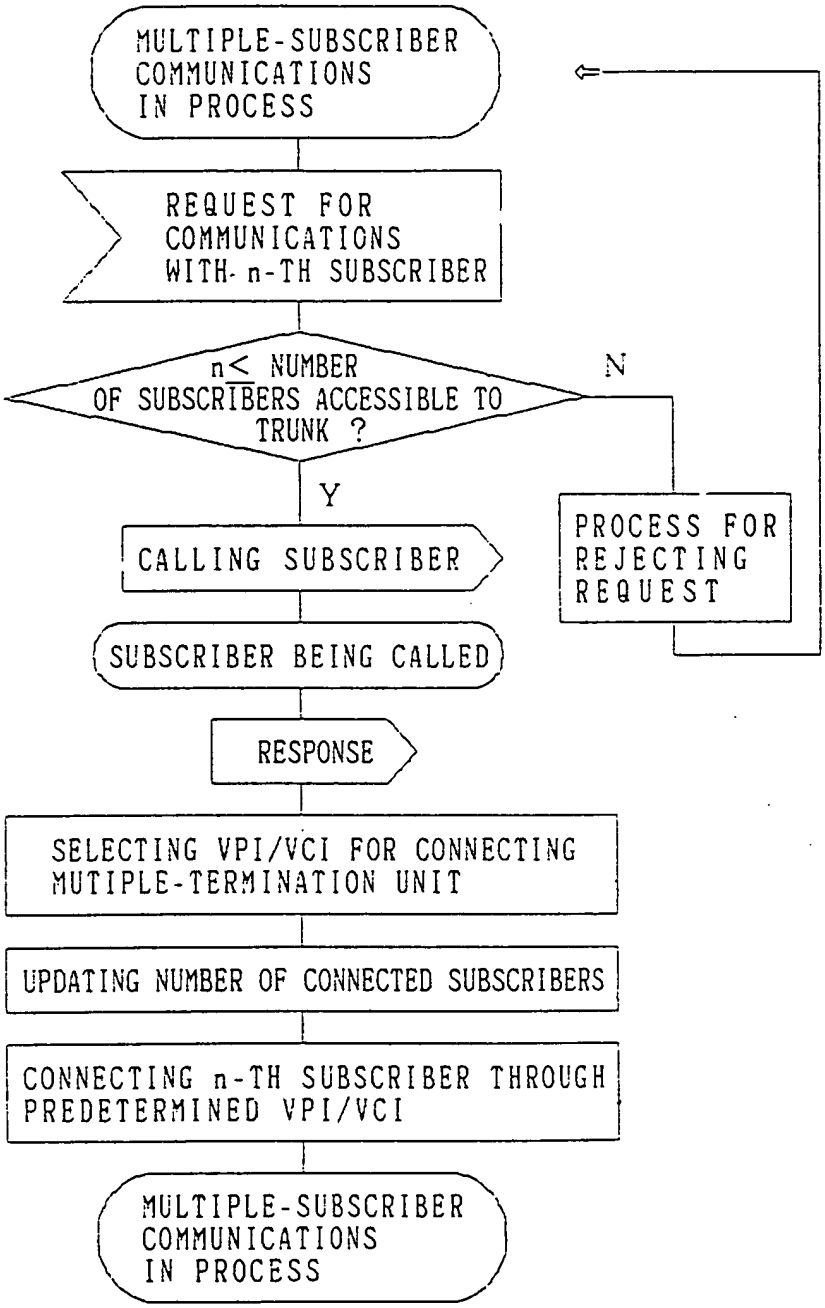

MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS
REQUEST FOR COMMUNICATIONS WITH n-TH SUBSCRIBER
n≤ NUMBER OF SUBSCRIBERS ACCESSIBLE TO TRUNK ?
N
Y
PROCESS FOR REJECTING REQUEST
CALLING SUBSCRIBER
SUBSCRIBER BEING CALLED
RESPONSE
SELECTING VPI/VCI FOR CONNECTING MUTIPLE-TERMINATION UNIT
UPDATING NUMBER OF CONNECTED SUBSCRIBERS
CONNECTING n-TH SUBSCRIBER THROUGH PREDETERMINED VPI/VCI
MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 857

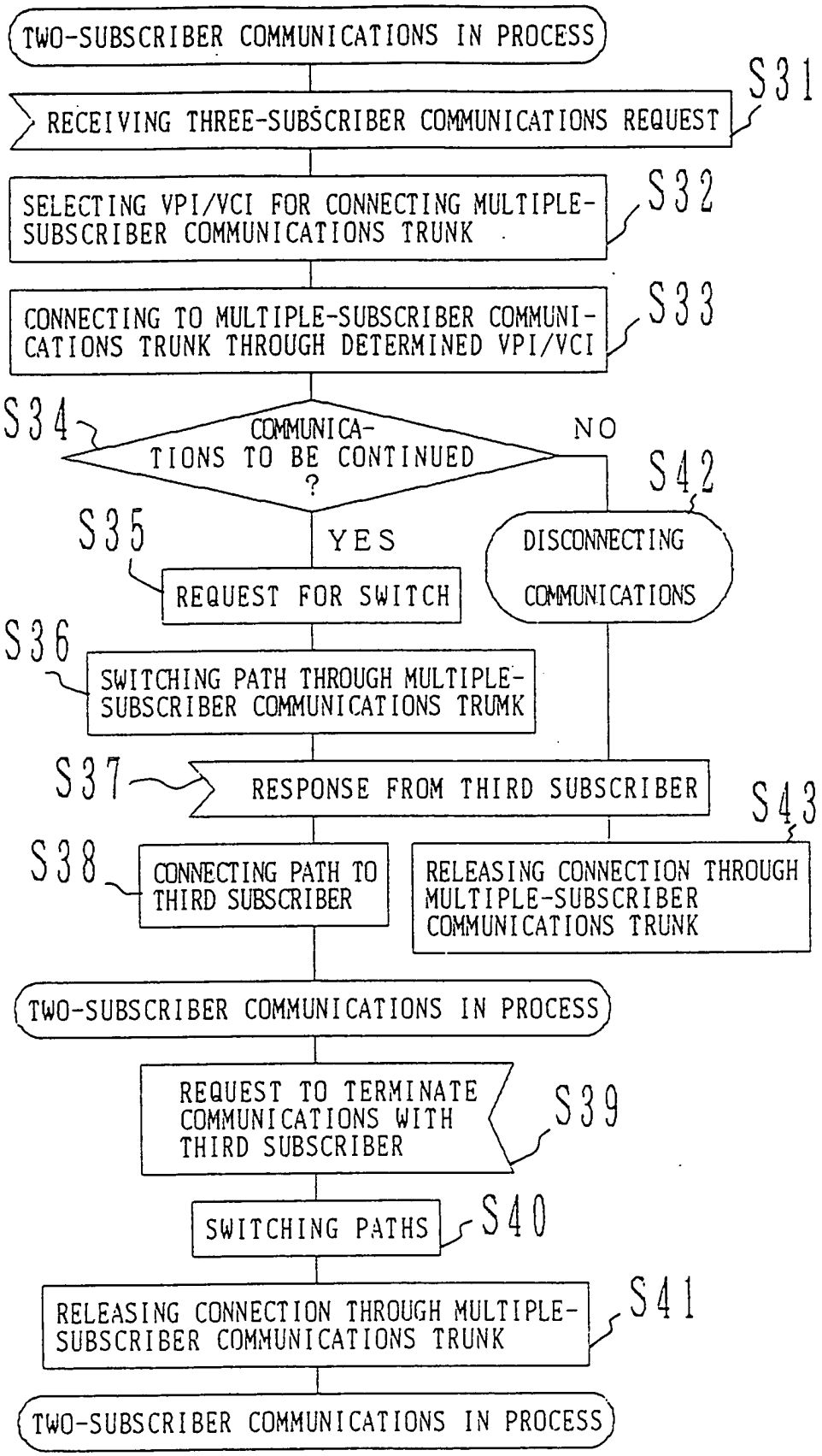

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
RECEIVING THREE-SUBSCRIBER COMMUNICATIONS REQUEST
S31
SELECTING VPI/VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S32
CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI
S33
S34
COMMUNICATIONS TO BE CONTINUED ?
NO
S42
YES
S35
REQUEST FOR SWITCH
DISCONNECTING COMMUNICATIONS
S36
SWITCHING PATH THROUGH MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUMK
S37
RESPONSE FROM THIRD SUBSCRIBER
S43
S38
CONNECTING PATH TO THIRD SUBSCRIBER
RELEASING CONNECTION THROUGH MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
REQUEST TO TERMINATE COMMUNICATIONS WITH THIRD SUBSCRIBER
S39
SWITCHING PATHS
S40
RELEASING CONNECTION THROUGH MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S41
TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 858

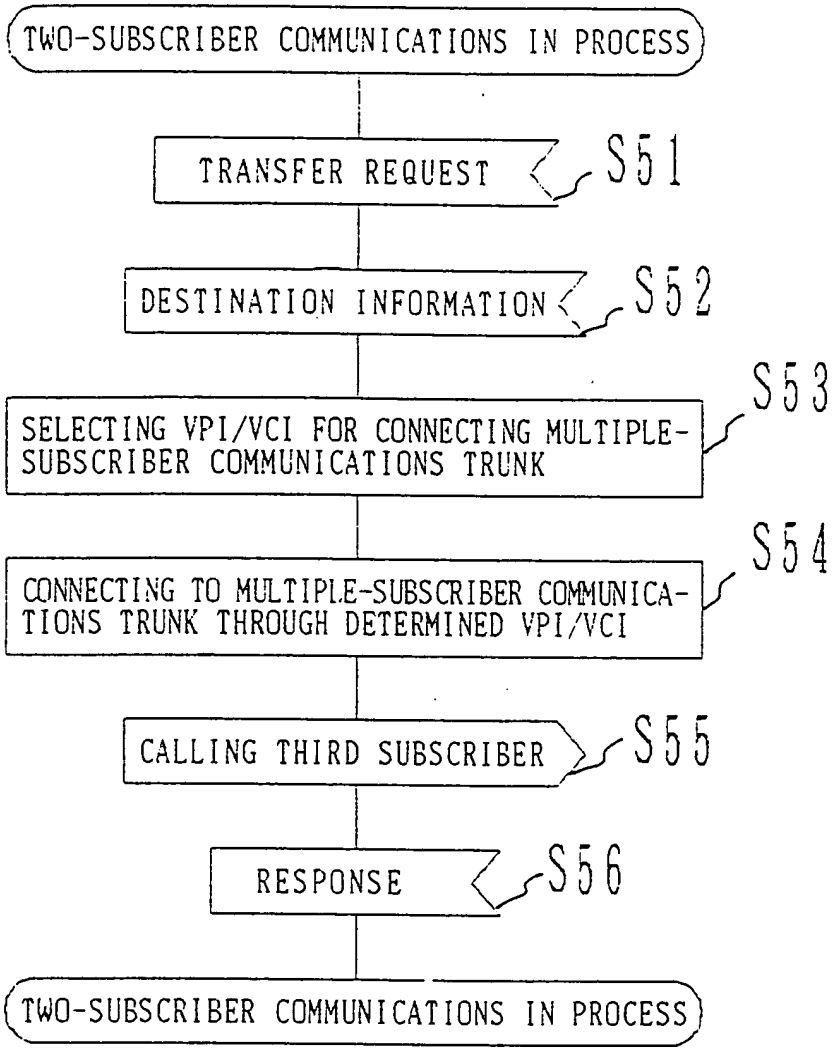

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
TRANSFER REQUEST
S51
DESTINATION INFORMATION
S52
SELECTING VPI/VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S53
CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI
S54
CALLING THIRD SUBSCRIBER
S55
RESPONSE
S56
TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 859

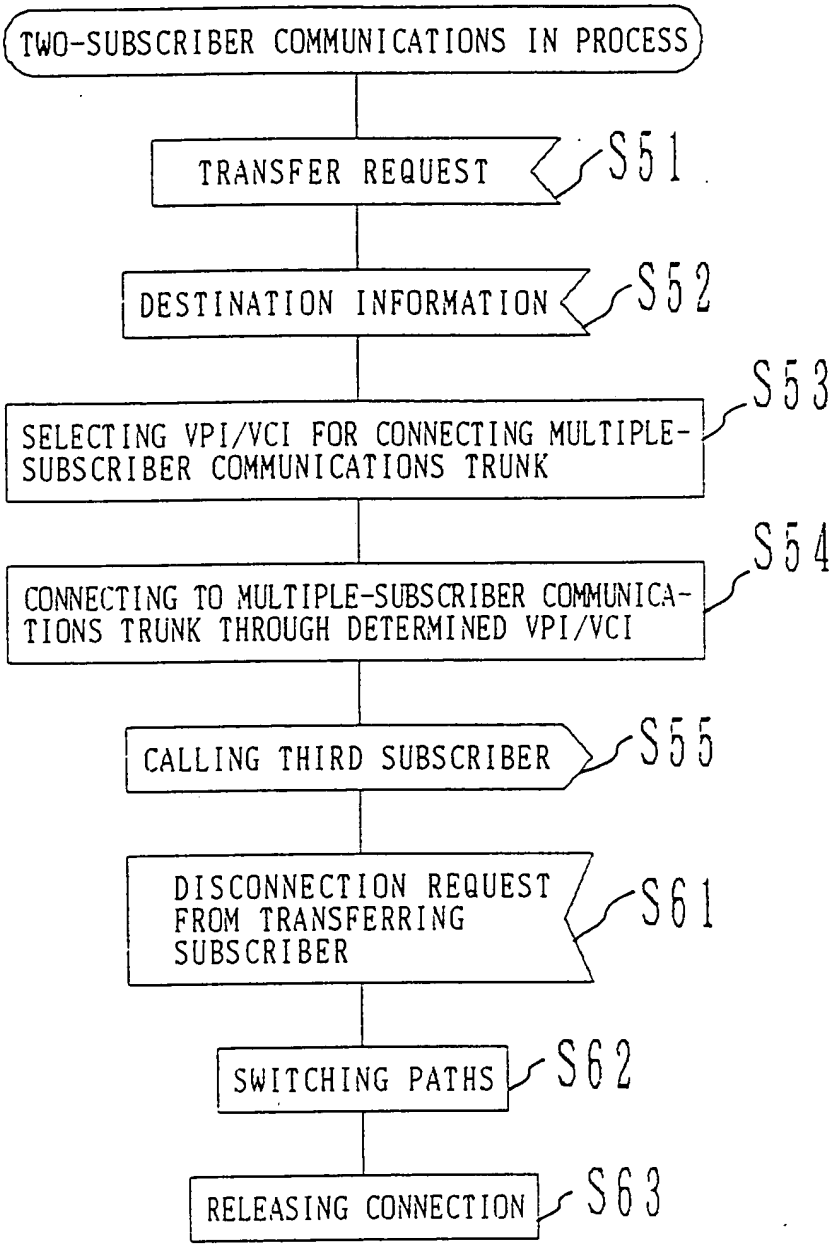

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
TRANSFER REQUEST
S51
DESTINATION INFORMATION
S52
SELECTING VPI/VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S53
CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI
S54
CALLING THIRD SUBSCRIBER
S55
DISCONNECTION REQUEST FROM TRANSFERRING SUBSCRIBER
S61
SWITCHING PATHS
S62
RELEASING CONNECTION
S63

FIG. 860

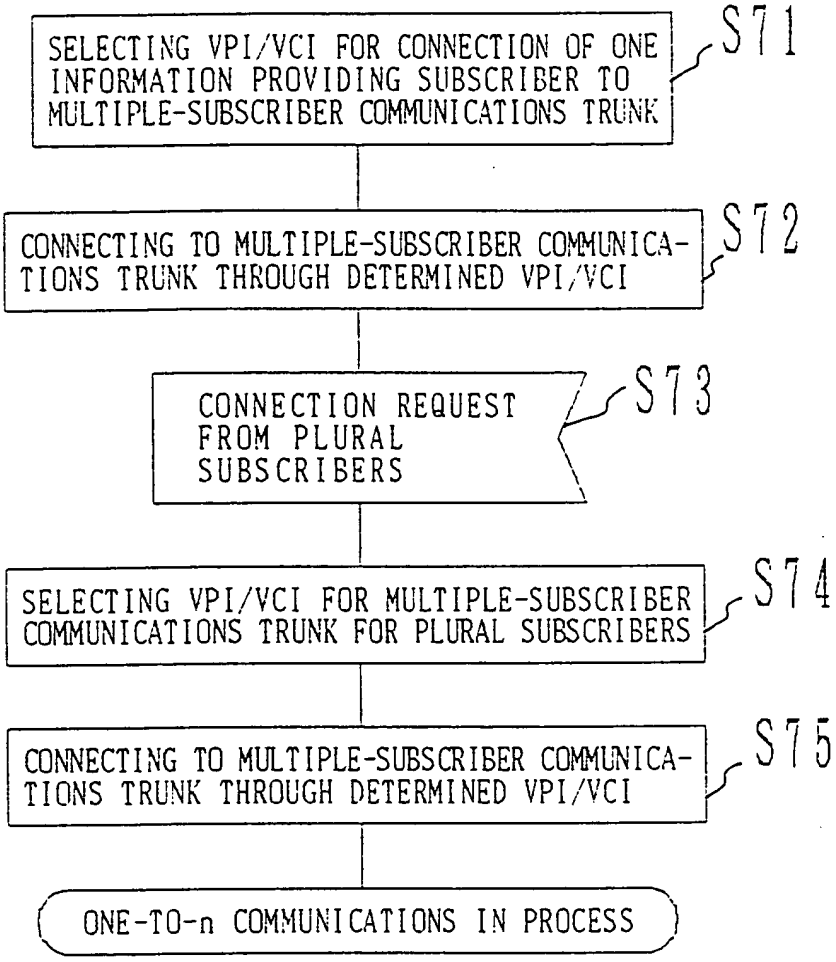

SELECTING VPI/VCI FOR CONNECTION OF ONE INFORMATION PROVIDING SUBSCRIBER TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK
S71
CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI
S72
CONNECTION REQUEST FROM PLURAL SUBSCRIBERS
S73
SELECTING VPI/VCI FOR MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK FOR PLURAL SUBSCRIBERS
S74
CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI
S75
ONE-TO-n COMMUNICATIONS IN PROCESS

FIG. 861

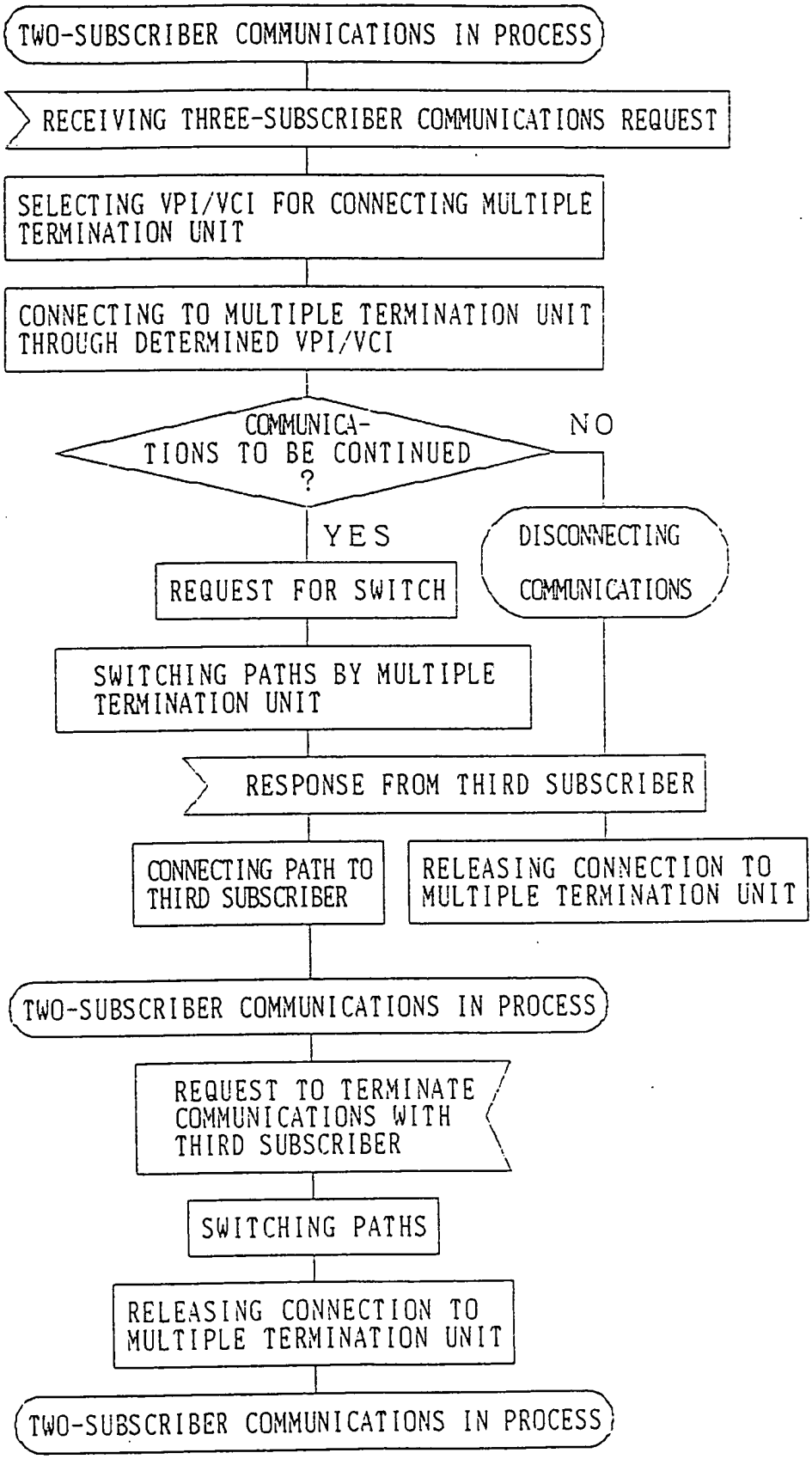

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
RECEIVING THREE-SUBSCRIBER COMMUNICATIONS REQUEST
SELECTING VPI/VCI FOR CONNECTING MULTIPLE TERMINATION UNIT
CONNECTING TO MULTIPLE TERMINATION UNIT THROUGH DETERMINED VPI/VCI
COMMUNICATIONS TO BE CONTINUED ?
NO
YES
DISCONNECTING COMMUNICATIONS
REQUEST FOR SWITCH
SWITCHING PATHS BY MULTIPLE TERMINATION UNIT
RESPONSE FROM THIRD SUBSCRIBER
CONNECTING PATH TO THIRD SUBSCRIBER
RELEASING CONNECTION TO MULTIPLE TERMINATION UNIT
TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
REQUEST TO TERMINATE COMMUNICATIONS WITH THIRD SUBSCRIBER
SWITCHING PATHS
RELEASING CONNECTION TO MULTIPLE TERMINATION UNIT
TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 862

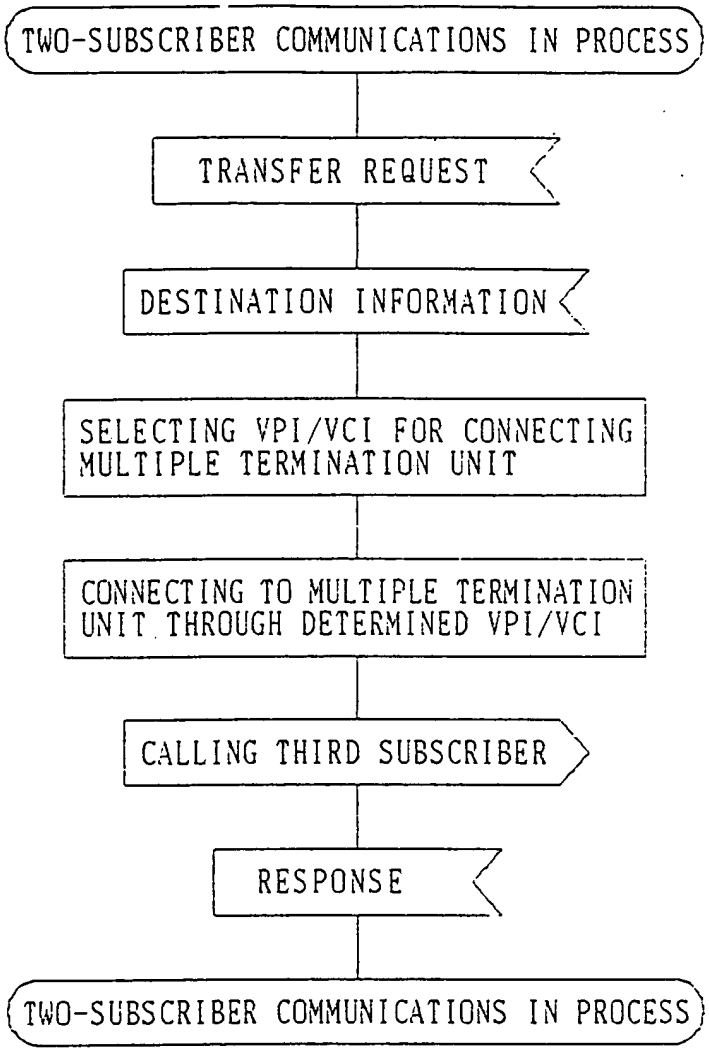

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
TRANSFER REQUEST
DESTINATION INFORMATION
SELECTING VPI/VCI FOR CONNECTING MULTIPLE TERMINATION UNIT
CONNECTING TO MULTIPLE TERMINATION UNIT THROUGH DETERMINED VPI/VCI
CALLING THIRD SUBSCRIBER
RESPONSE
TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 863

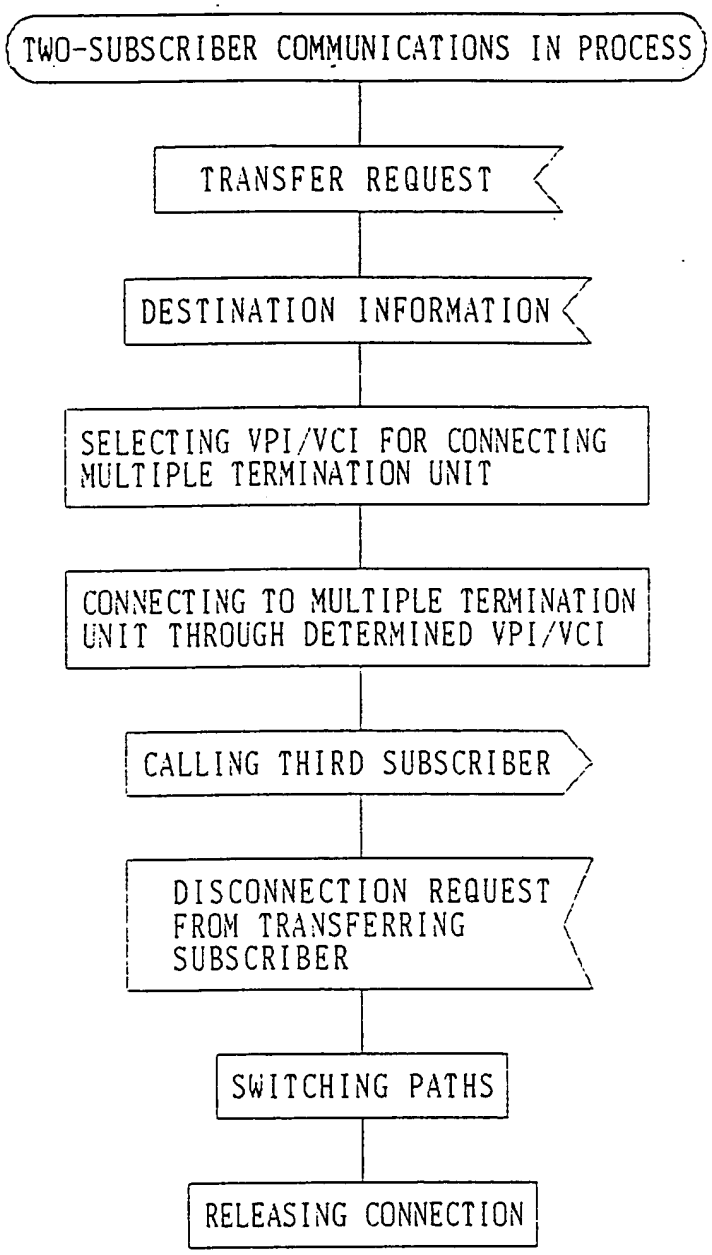

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS
TRANSFER REQUEST
DESTINATION INFORMATION
SELECTING VPI/VCI FOR CONNECTING MULTIPLE TERMINATION UNIT
CONNECTING TO MULTIPLE TERMINATION UNIT THROUGH DETERMINED VPI/VCI
CALLING THIRD SUBSCRIBER
DISCONNECTION REQUEST FROM TRANSFERRING SUBSCRIBER
SWITCHING PATHS
RELEASING CONNECTION

FIG. 864

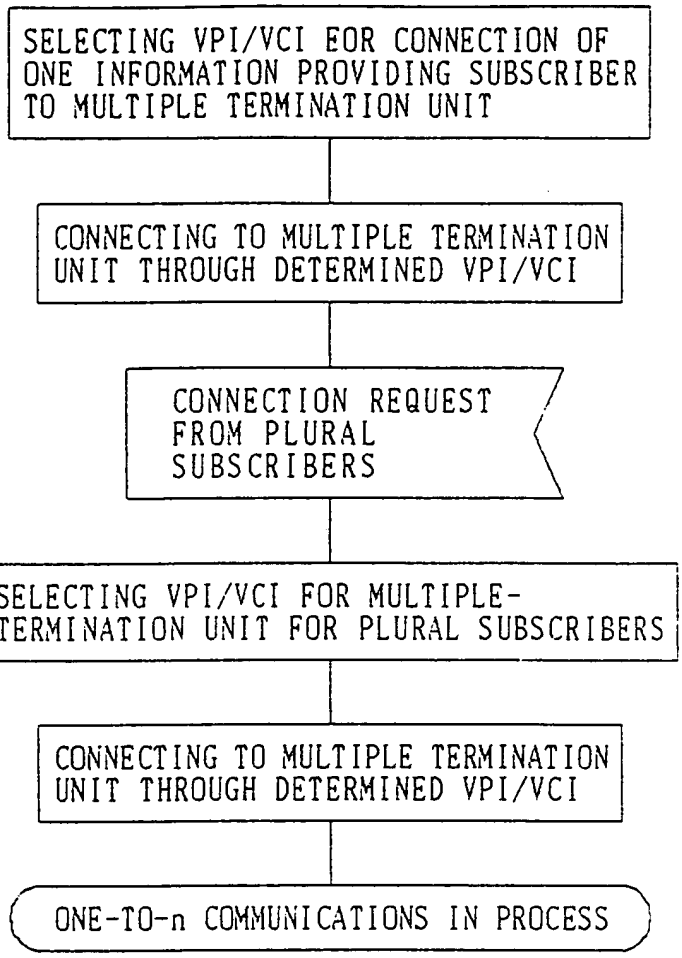


FIG. 865

5,526,345

5,526,350

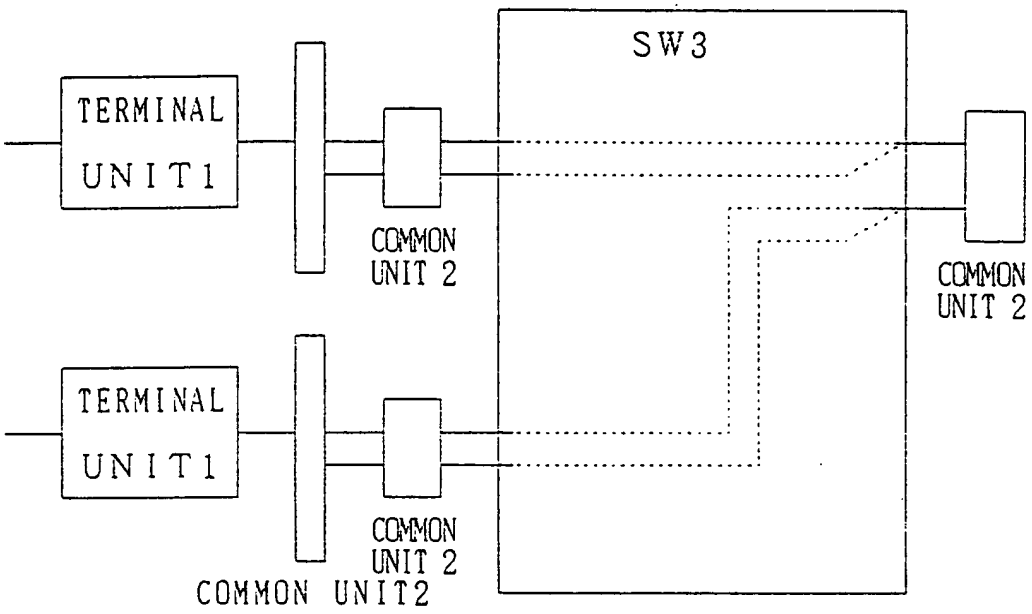


FIG. 866

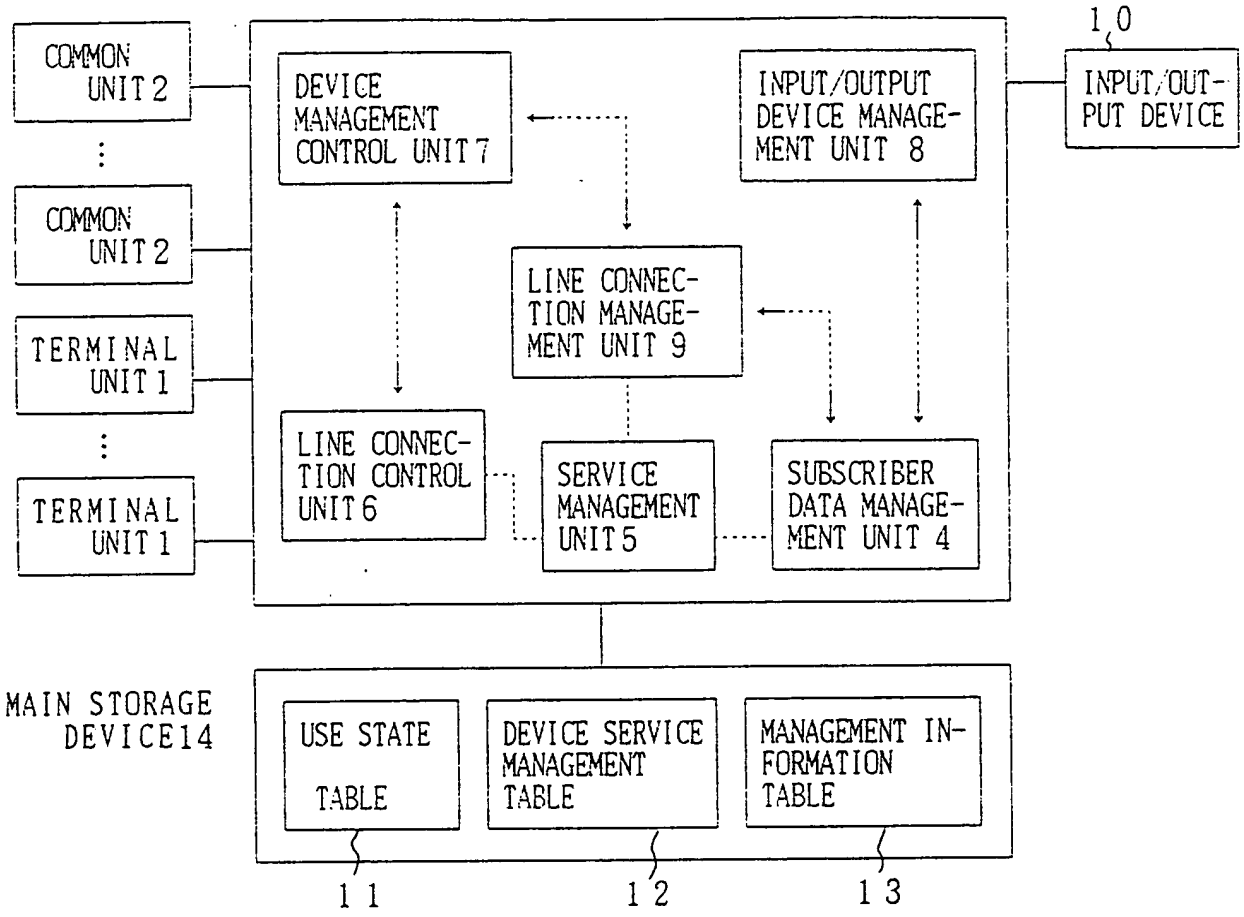
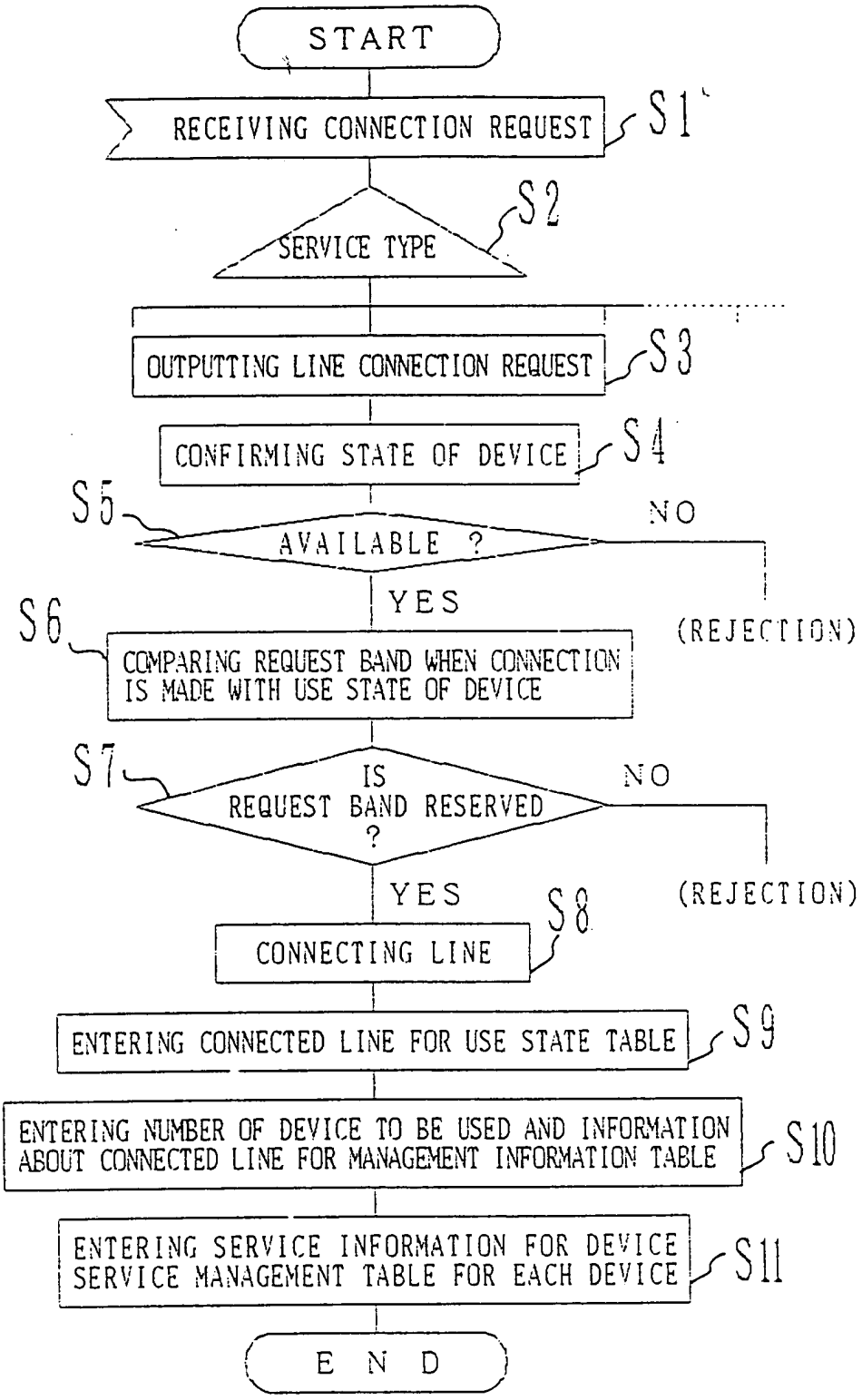

COMMON UNIT 2
COMMON UNIT 2
TERMINAL UNIT 1
TERMINAL UNIT 1
DEVICE MANAGEMENT CONTROL UNIT 7
INPUT/OUTPUT DEVICE MANAGEMENT UNIT 8
LINE CONNECTION MANAGEMENT UNIT 9
LINE CONNECTION CONTROL UNIT 6
SERVICE MANAGEMENT UNIT 5
SUBSCRIBER DATA MANAGEMENT UNIT 4
10
INPUT/OUTPUT DEVICE
MAIN STORAGE DEVICE 14
USE STATE TABLE
DEVICE SERVICE MANAGEMENT TABLE
MANAGEMENT INFORMATION TABLE
11
12
13

FIG. 867


START
RECEIVING CONNECTION REQUEST
S1
SERVICE TYPE
S2
OUTPUTTING LINE CONNECTION REQUEST
S3
CONFIRMING STATE OF DEVICE
S4
S5
AVAILABLE ?
NO
(REJECTION)
YES
S6
COMPARING REQUEST BAND WHEN CONNECTION IS MADE WITH USE STATE OF DEVICE
S7
IS REQUEST BAND RESERVED ?
NO
(REJECTION)
YES
S8
CONNECTING LINE
ENTERING CONNECTED LINE FOR USE STATE TABLE
S9
ENTERING NUMBER OF DEVICE TO BE USED AND INFORMATION ABOUT CONNECTED LINE FOR MANAGEMENT INFORMATION TABLE
S10
ENTERING SERVICE INFORMATION FOR DEVICE SERVICE MANAGEMENT TABLE FOR EACH DEVICE
S11
E N D

F I G. 8 6 8

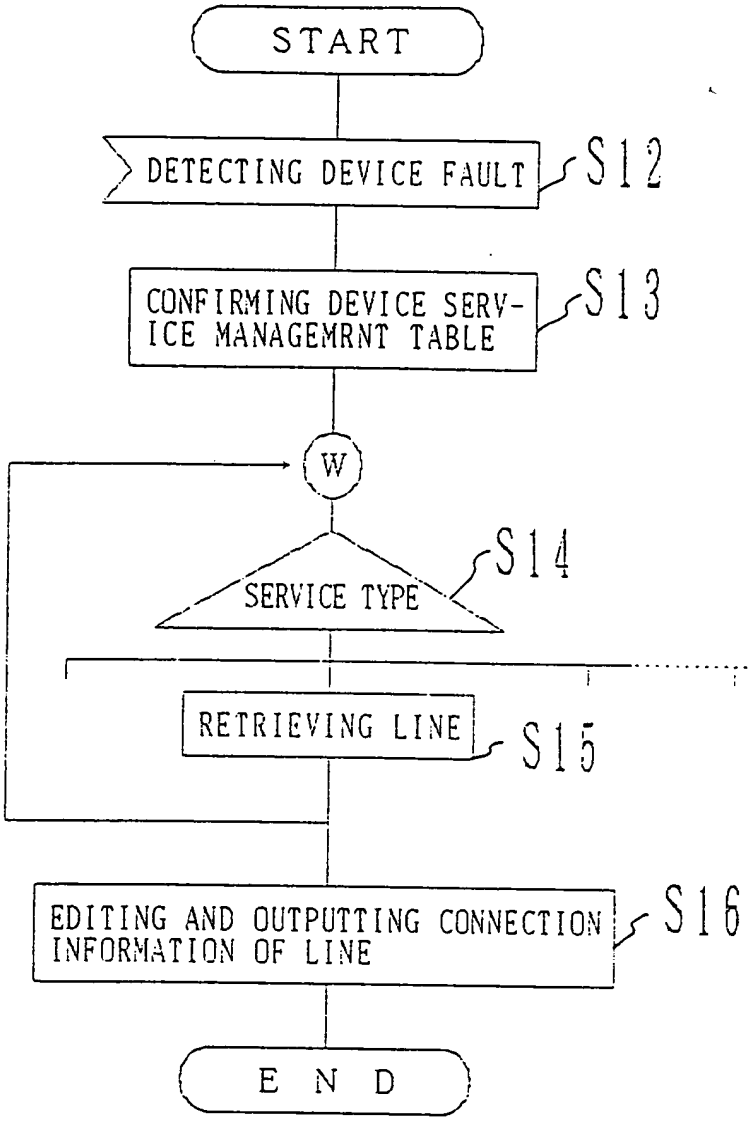

START
DETECTING DEVICE FAULT
S12
CONFIRMING DEVICE SERV-ICE MANAGEMRNT TABLE
S13
W
SERVICE TYPE
S14
RETRIEVING LINE
S15
EDITING AND OUTPUTTING CONNECTION INFORMATION OF LINE
S16
E N D

FIG. 869

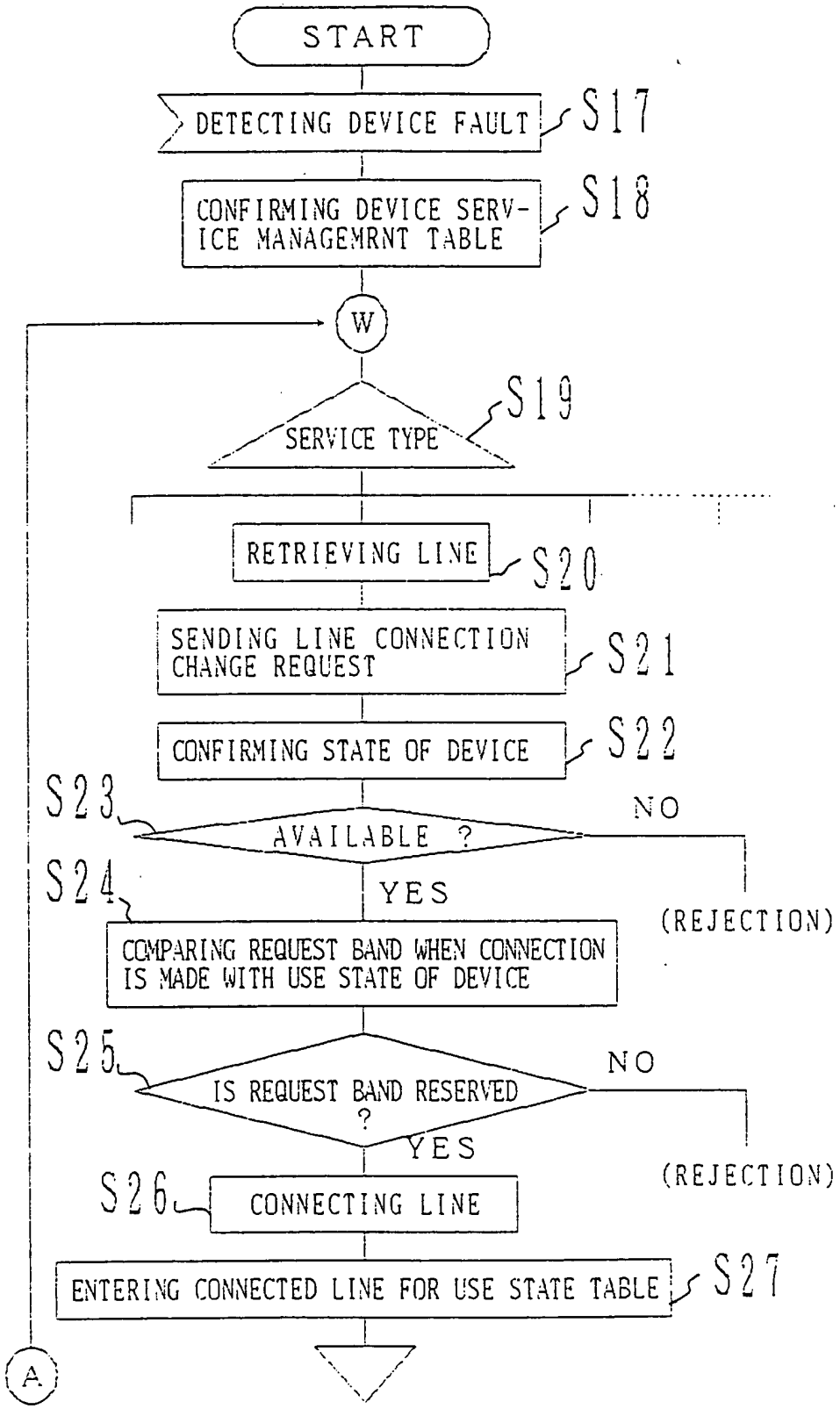

START
DETECTING DEVICE FAULT
S17
CONFIRMING DEVICE SERV-ICE MANAGEMRNT TABLE
S18
W
SERVICE TYPE
S19
RETRIEVING LINE
S20
SENDING LINE CONNECTION CHANGE REQUEST
S21
CONFIRMING STATE OF DEVICE
S22
S23
AVAILABLE ?
NO
YES
(REJECTION)
S24
COMPARING REQUEST BAND WHEN CONNECTION IS MADE WITH USE STATE OF DEVICE
S25
IS REQUEST BAND RESERVED ?
NO
YES
(REJECTION)
S26
CONNECTING LINE
ENTERING CONNECTED LINE FOR USE STATE TABLE
S27
A

FIG. 870

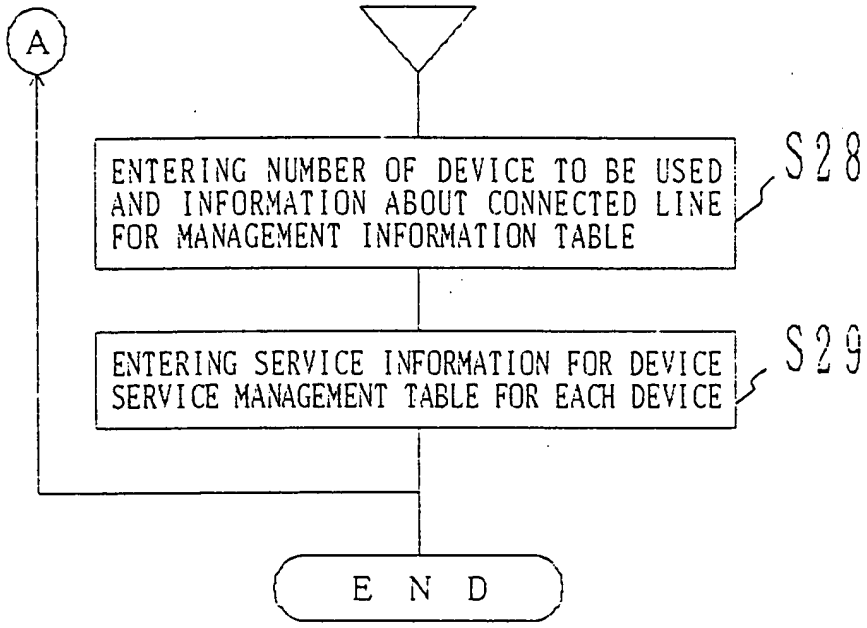

A
ENTERING NUMBER OF DEVICE TO BE USED AND INFORMATION ABOUT CONNECTED LINE FOR MANAGEMENT INFORMATION TABLE
S28
ENTERING SERVICE INFORMATION FOR DEVICE SERVICE MANAGEMENT TABLE FOR EACH DEVICE
S29
E N D

FIG. 871

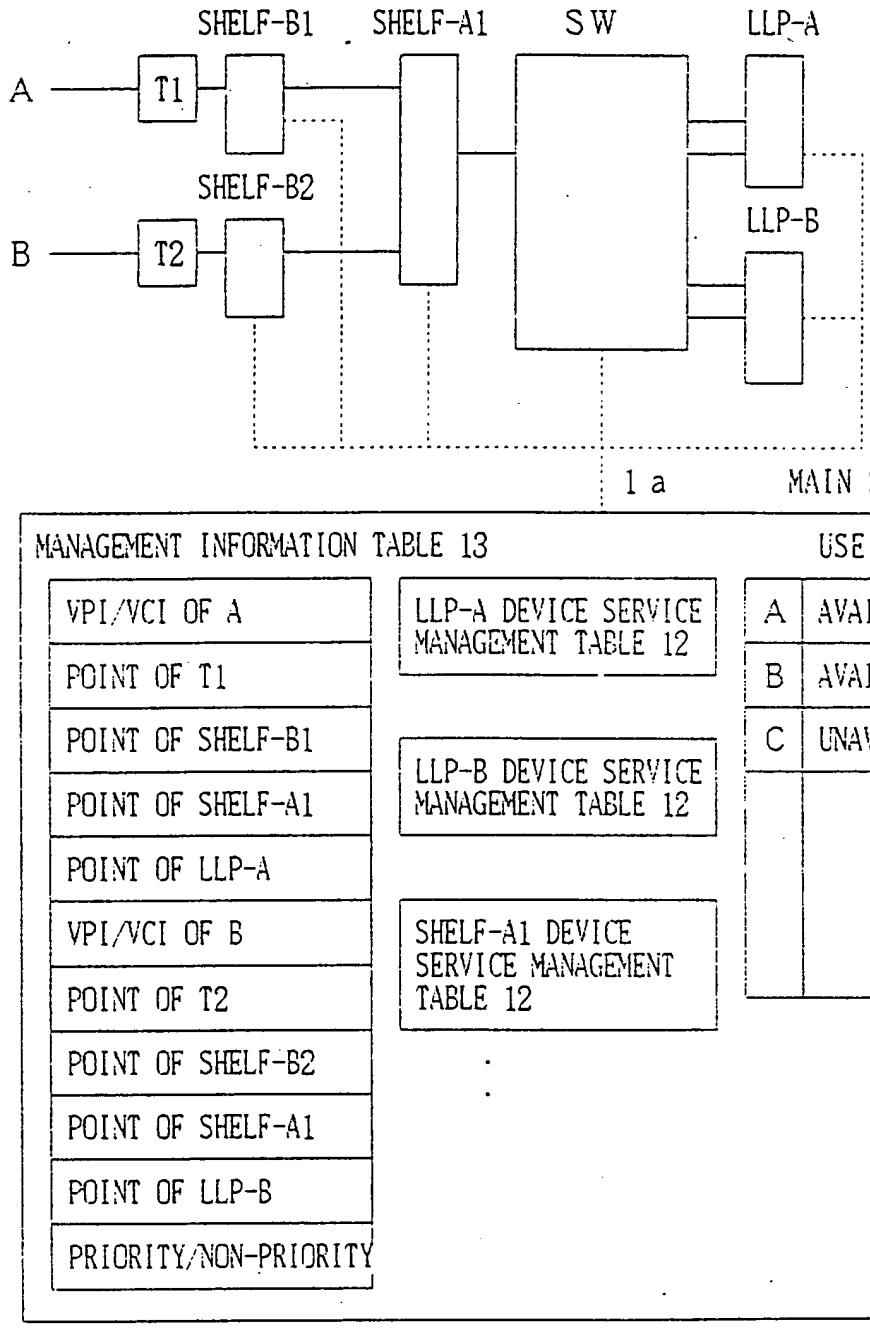
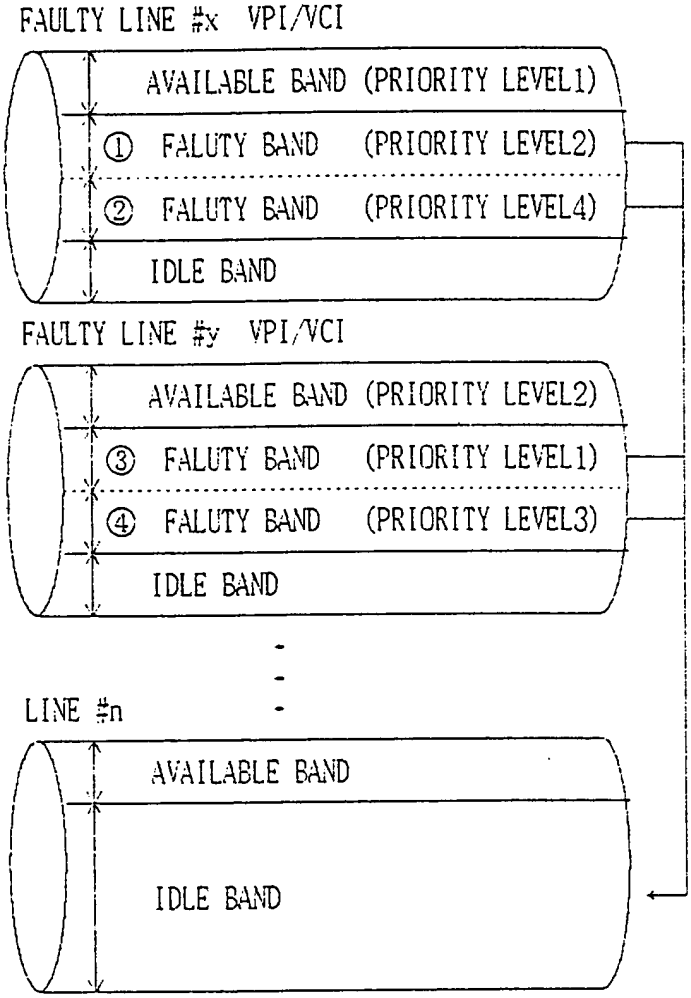

SHELF-B1
SHELF-A1
SW
LLP-A
A
T1
SHELF-B2
LLP-B
B
T2
1 a
MAIN STORAGE DEVICE 14
MANAGEMENT INFORMATION TABLE 13
USE STATE TABLE 11
VPI/VCI OF A
POINT OF T1
POINT OF SHELF-B1
POINT OF SHELF-A1
POINT OF LLP-A
VPI/VCI OF B
POINT OF T2
POINT OF SHELF-B2
POINT OF SHELF-A1
POINT OF LLP-B
PRIORITY/NON-PRIORITY
LLP-A DEVICE SERVICE MANAGEMENT TABLE 12
LLP-B DEVICE SERVICE MANAGEMENT TABLE 12
SHELF-A1 DEVICE SERVICE MANAGEMENT TABLE 12
A
AVAILABLE
30M USED
B
AVAILABLE
UNUSED
C
UNAVAILABLE
——

FIG. 872



SWITCHING CONDITION

LINE FAULT ON LAYER 1 OR LAYER 2 AND SUCCEEDING LAYERS WITH FAULTY BAND≦SUM OF IDLE BANDS IN EACH LINE

NON-FAULTY BAND OF FAULTY LINES #X AND #Y ARE USED AS IS.

VP/VC IS NOT REASSIGNED TO IDLE BAND IN FAULTY LINES #X AND #Y.

PRIORITY LEVEL IS ADDED TO CELL INFORMATION OF EACH AVAILABLE BAND, AND REASSIGNMENT IS PERFORMED IN ORDER OF 3→1→4→3 FROM HIGHEST PRIORITY LEVEL IN FAULTY BAND.

FIG. 873

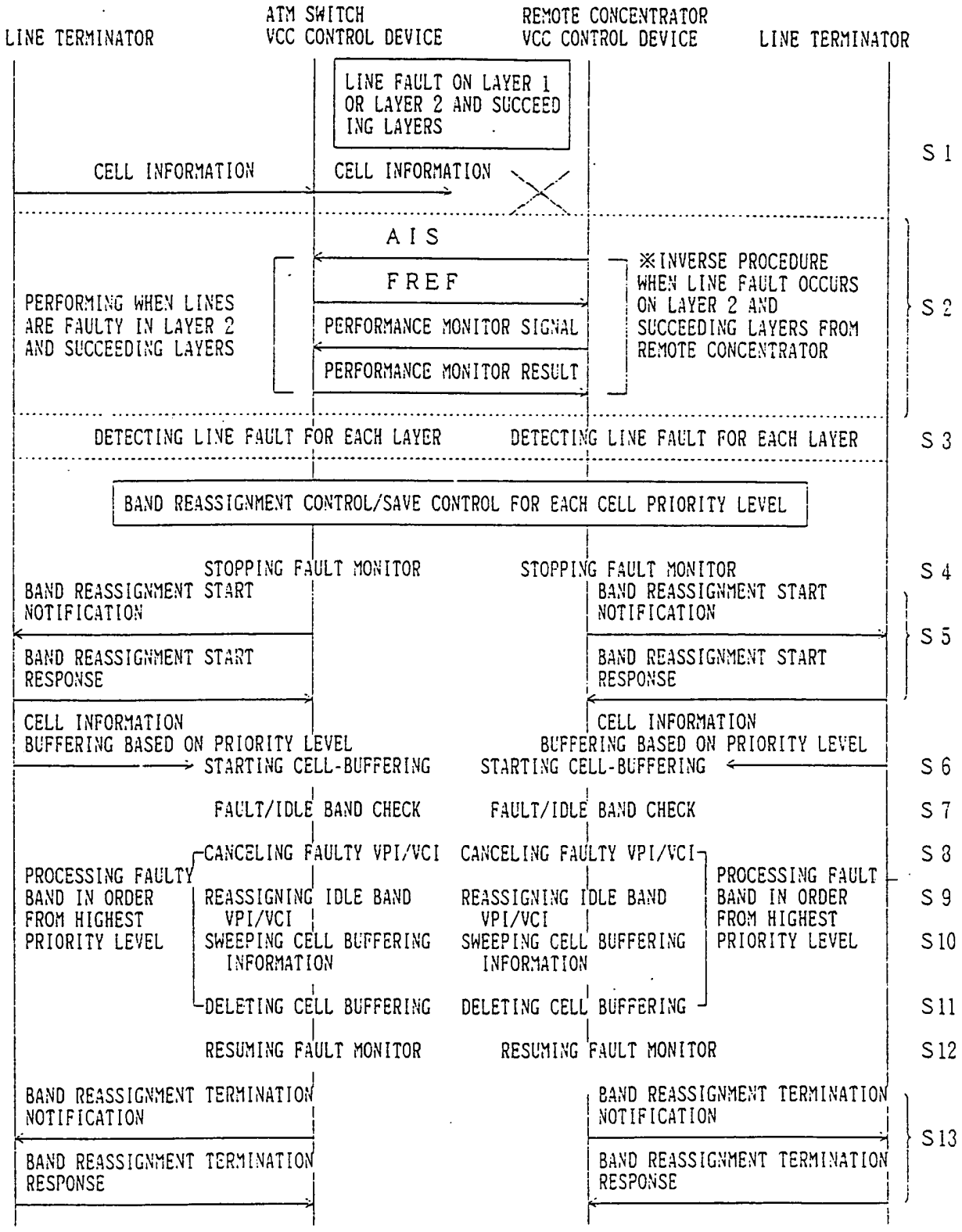
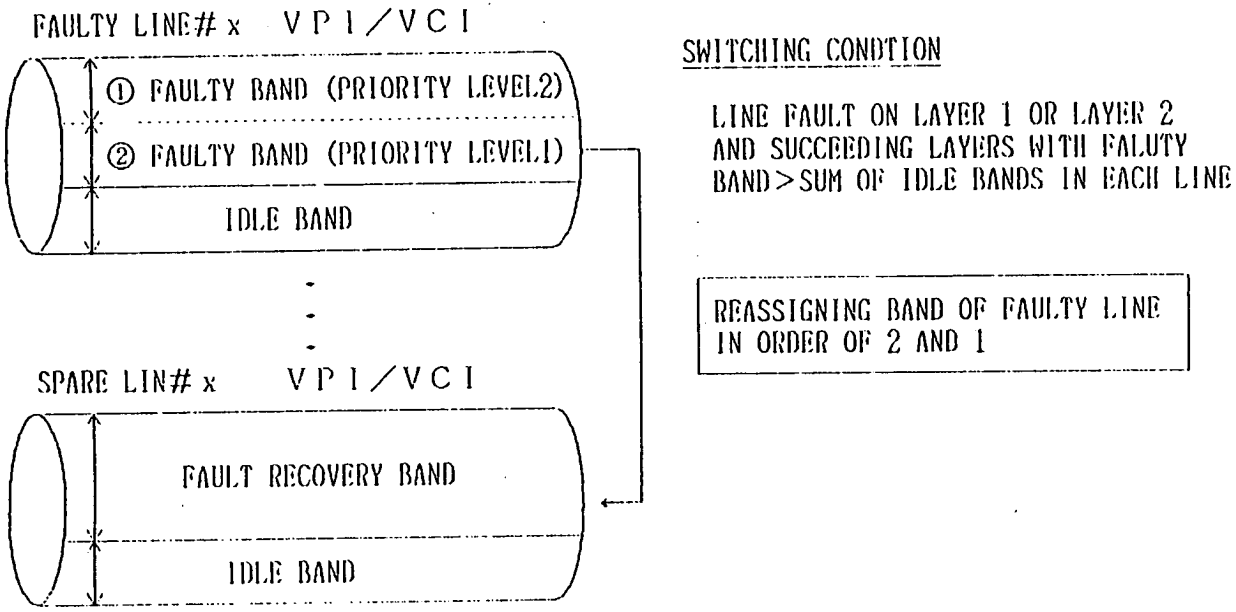

LINE TERMINATOR
ATM SWITCH VCC CONTROL DEVICE
REMOTE CONCENTRATOR VCC CONTROL DEVICE
LINE TERMINATOR
LINE FAULT ON LAYER 1 OR LAYER 2 AND SUCCEEDING LAYERS
S 1
CELL INFORMATION
CELL INFORMATION
AIS
FREF
PERFORMANCE MONITOR SIGNAL
PERFORMANCE MONITOR RESULT
PERFORMING WHEN LINES ARE FAULTY IN LAYER 2 AND SUCCEEDING LAYERS
※INVERSE PROCEDURE WHEN LINE FAULT OCCURS ON LAYER 2 AND SUCCEEDING LAYERS FROM REMOTE CONCENTRATOR
S 2
DETECTING LINE FAULT FOR EACH LAYER
DETECTING LINE FAULT FOR EACH LAYER
S 3
BAND REASSIGNMENT CONTROL/SAVE CONTROL FOR EACH CELL PRIORITY LEVEL
STOPPING FAULT MONITOR
STOPPING FAULT MONITOR
S 4
BAND REASSIGNMENT START NOTIFICATION
BAND REASSIGNMENT START NOTIFICATION
S 5
BAND REASSIGNMENT START RESPONSE
BAND REASSIGNMENT START RESPONSE
CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL
CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL
STARTING CELL-BUFFERING
STARTING CELL-BUFFERING
S 6
FAULT/IDLE BAND CHECK
FAULT/IDLE BAND CHECK
S 7
CANCELING FAULTY VPI/VCI
CANCELING FAULTY VPI/VCI
S 8
PROCESSING FAULTY BAND IN ORDER FROM HIGHEST PRIORITY LEVEL
REASSIGNING IDLE BAND VPI/VCI
SWEEPING CELL BUFFERING INFORMATION
REASSIGNING IDLE BAND VPI/VCI
SWEEPING CELL BUFFERING INFORMATION
PROCESSING FAULT BAND IN ORDER FROM HIGHEST PRIORITY LEVEL
S 9
S10
DELETING CELL BUFFERING
DELETING CELL BUFFERING
S11
RESUMING FAULT MONITOR
RESUMING FAULT MONITOR
S12
BAND REASSIGNMENT TERMINATION NOTIFICATION
BAND REASSIGNMENT TERMINATION NOTIFICATION
S13
BAND REASSIGNMENT TERMINATION RESPONSE
BAND REASSIGNMENT TERMINATION RESPONSE

FIG. 874



SWITCHING CONDTION

LINE FAULT ON LAYER 1 OR LAYER 2 AND SUCCEEDING LAYERS WITH FALUTY BAND > SUM OF IDLE BANDS IN EACH LINE

REASSIGNING BAND OF FAULTY LINE IN ORDER OF 2 AND 1

FIG. 875

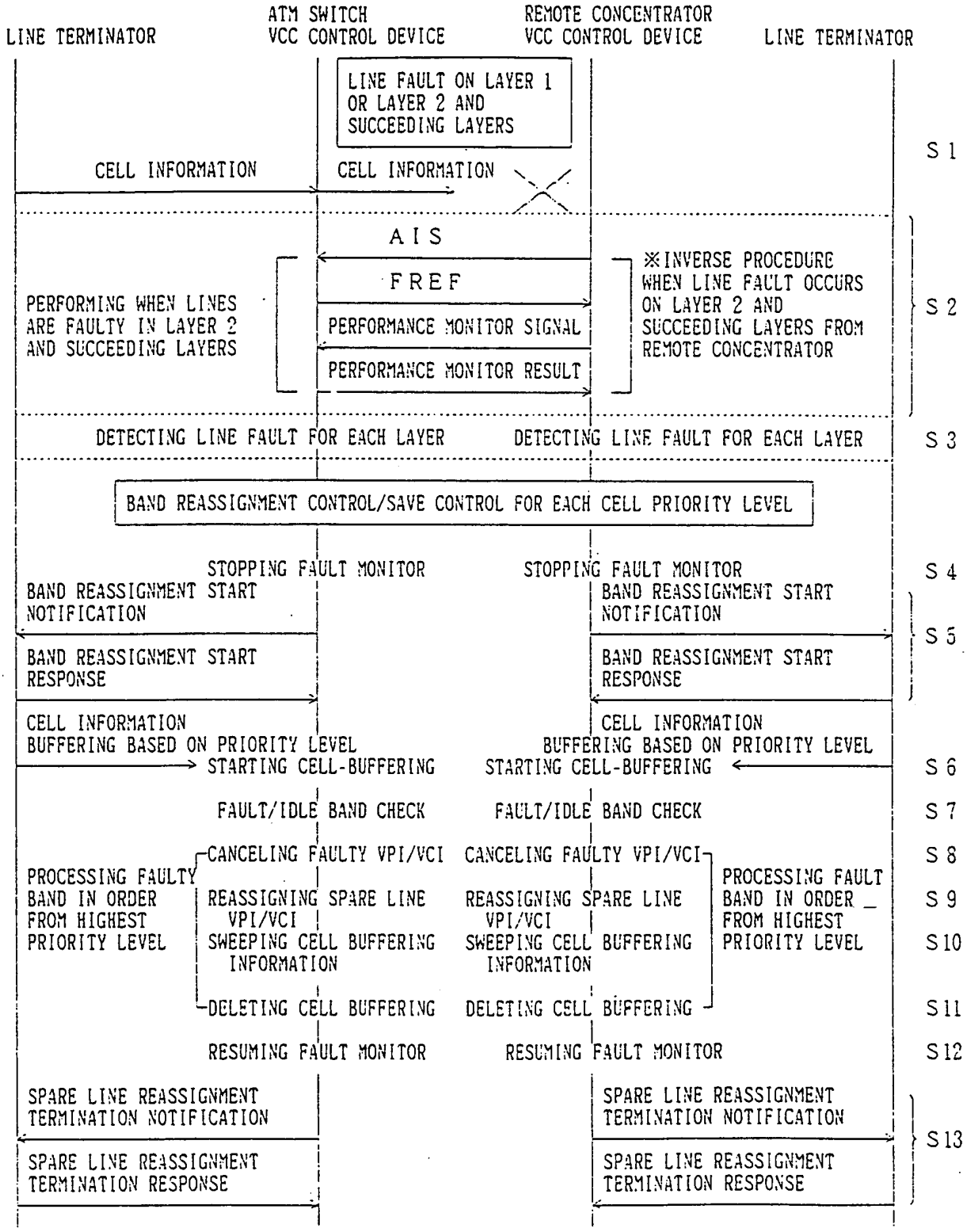

LINE TERMINATOR
ATM SWITCH VCC CONTROL DEVICE
REMOTE CONCENTRATOR VCC CONTROL DEVICE
LINE TERMINATOR
LINE FAULT ON LAYER 1 OR LAYER 2 AND SUCCEEDING LAYERS
S 1
CELL INFORMATION
CELL INFORMATION
AIS
FREF
PERFORMANCE MONITOR SIGNAL
PERFORMANCE MONITOR RESULT
PERFORMING WHEN LINES ARE FAULTY IN LAYER 2 AND SUCCEEDING LAYERS
※INVERSE PROCEDURE WHEN LINE FAULT OCCURS ON LAYER 2 AND SUCCEEDING LAYERS FROM REMOTE CONCENTRATOR
S 2
DETECTING LINE FAULT FOR EACH LAYER
DETECTING LINE FAULT FOR EACH LAYER
S 3
BAND REASSIGNMENT CONTROL/SAVE CONTROL FOR EACH CELL PRIORITY LEVEL
STOPPING FAULT MONITOR
BAND REASSIGNMENT START NOTIFICATION
STOPPING FAULT MONITOR
BAND REASSIGNMENT START NOTIFICATION
S 4
S 5
BAND REASSIGNMENT START RESPONSE
BAND REASSIGNMENT START RESPONSE
CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL
STARTING CELL-BUFFERING
CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL
STARTING CELL-BUFFERING
S 6
FAULT/IDLE BAND CHECK
FAULT/IDLE BAND CHECK
S 7
CANCELING FAULTY VPI/VCI
CANCELING FAULTY VPI/VCI
S 8
PROCESSING FAULTY BAND IN ORDER FROM HIGHEST PRIORITY LEVEL
REASSIGNING SPARE LINE VPI/VCI
SWEEPING CELL BUFFERING INFORMATION
REASSIGNING SPARE LINE VPI/VCI
SWEEPING CELL BUFFERING INFORMATION
PROCESSING FAULT BAND IN ORDER FROM HIGHEST PRIORITY LEVEL
S 9
S 10
DELETING CELL BUFFERING
DELETING CELL BUFFERING
S 11
RESUMING FAULT MONITOR
RESUMING FAULT MONITOR
S 12
SPARE LINE REASSIGNMENT TERMINATION NOTIFICATION
SPARE LINE REASSIGNMENT TERMINATION NOTIFICATION
S 13
SPARE LINE REASSIGNMENT TERMINATION RESPONSE
SPARE LINE REASSIGNMENT TERMINATION RESPONSE

FIG. 876

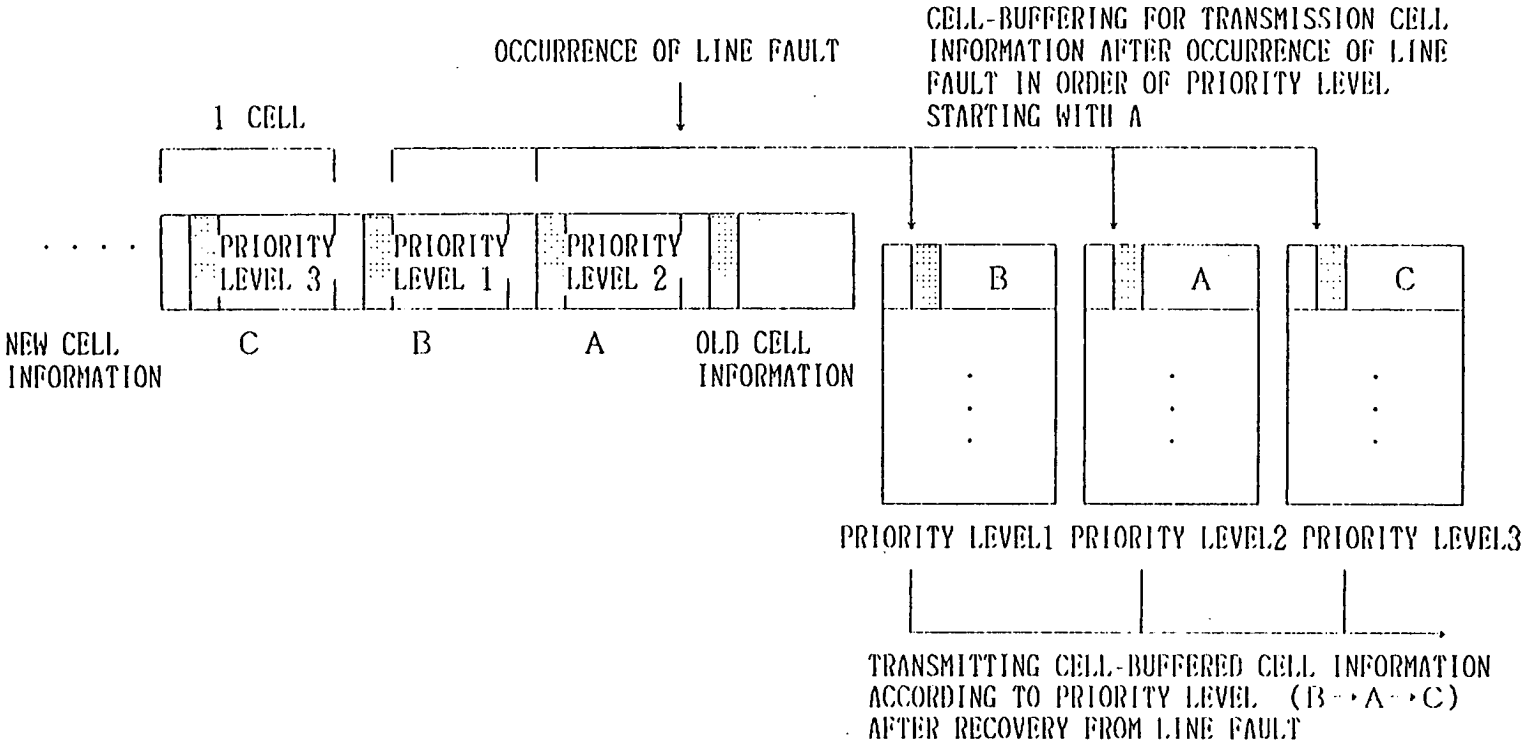
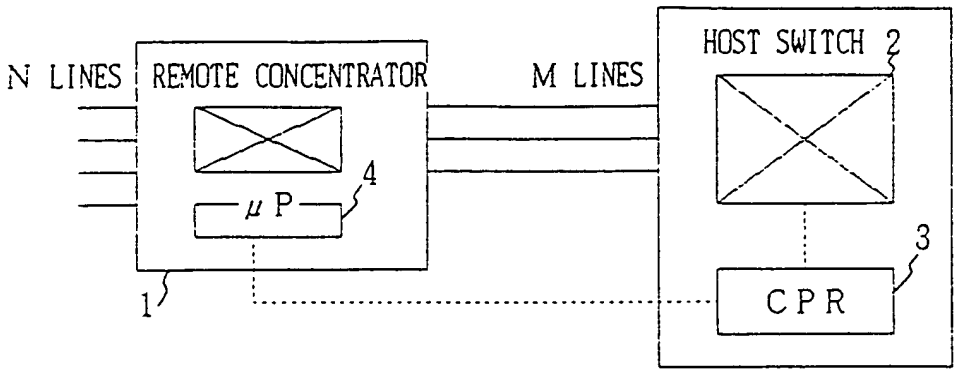

OCCURRENCE OF LINE FAULT
CELL-BUFFERING FOR TRANSMISSION CELL INFORMATION AFTER OCCURRENCE OF LINE FAULT IN ORDER OF PRIORITY LEVEL STARTING WITH A
1 CELL
PRIORITY LEVEL 3
PRIORITY LEVEL 1
PRIORITY LEVEL 2
NEW CELL INFORMATION
C
B
A
OLD CELL INFORMATION
B
A
C
PRIORITY LEVEL1 PRIORITY LEVEL2 PRIORITY LEVEL3
TRANSMITTING CELL-BUFFERED CELL INFORMATION ACCORDING TO PRIORITY LEVEL (B→A→C) AFTER RECOVERY FROM LINE FAULT

FIG. 877

(Ⅰ) CELL TYPE LEVEL ····· OAM CELL, INTRA-STATION LAP CELL, COMMON CELL, TEST CELL, ETC.
(Ⅱ) SERVICE LEVEL ····· FR, SMDS, CR, CE, ETC.
(Ⅲ) AVAILABLE BAND LEVEL··· DEFINING PRIORITY OR NON-PRIORITY DEPENDING ON SIZE OF AVAILABLE BAND.
(Ⅳ) LINE TYPE LEVEL ····· OC3, OC12, ETC.

CELL TYPE	CELL SIGNAL NAME	PRIORITY LEVEL
OAM CELL	AIS (WARNING DISPLAY SIGNAL) FERF (REMOTE TERMINAL RECEPTION FAULT) PERFORMANCE MONITOR SIGNAL etc	1
INTRA-STATION LAP CELL	TRAFFIC INFORMATION BILLING INFORMATION PERFORMANCE INFORMATION etc	2
COMMON CELL	PRIORITY BIT ON INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING SMALL AMOUNT OF INFORMATION OR SMALL NUMBER OF CELLS)	3
	PRIORITY BIT ON INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING LARGE AMOUNT OF INFORMATION OR LARGE NUMBER OF CELLS)	4
	PRIORITY BIT OFF INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING SMALL AMOUNT OF INFORMATION OR SMALL NUMBER OF CELLS)	5
	PRIORITY BIT OFF INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING LARGE AMOUNT OF INFORMATION OR LARGE NUMBER OF CELLS)	6
TEST CELL	CELL LOOPBACK TEST INFORMATION LOOPBACK TEST INFORMATION etc	7

FIG. 878



WHERE N > M

FIG. 879

6,563,836 5/13/2003

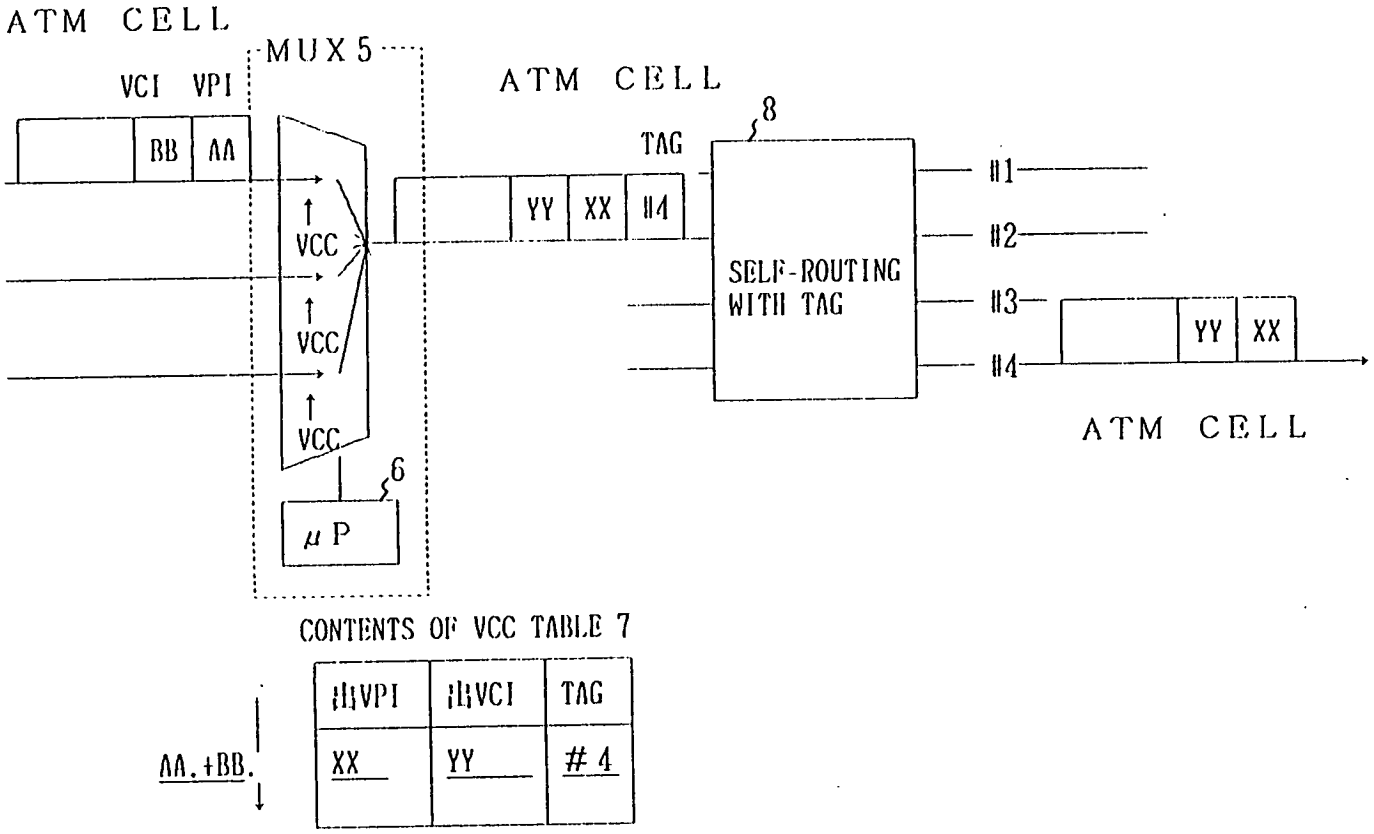
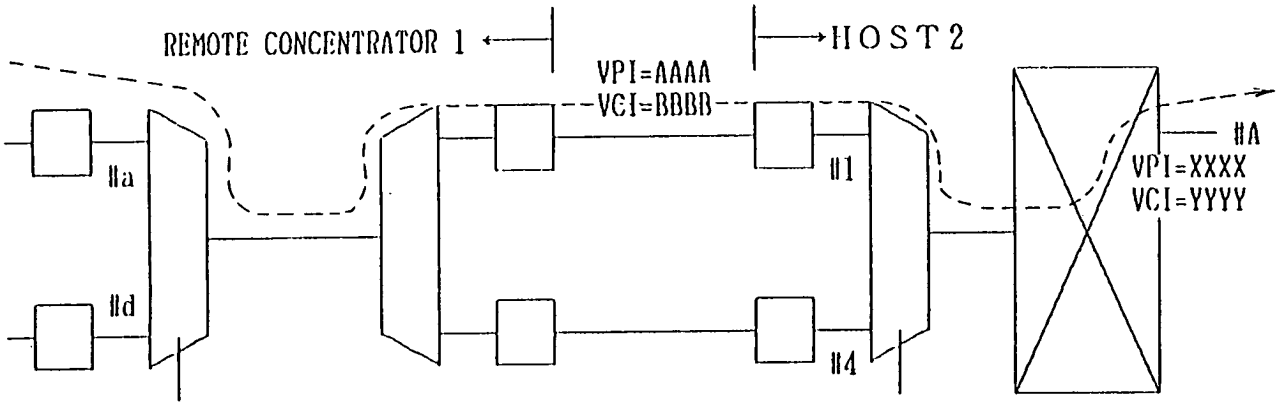

ATM CELL
MUX 5
VCI VPI
BB AA
VCC
VCC
VCC
6
μP
ATM CELL
TAG
8
YY XX #4
SELF-ROUTING WITH TAG
#1
#2
#3
#4
YY XX
ATM CELL
CONTENTS OF VCC TABLE 7
AA.+BB.
#4VPI
#4VCI
TAG
XX
YY
#4

FIG. 8 8 0



FIRST UPWARD VCC TABLE

#a	OUTPUT VPI	OUTPUT VCI	TAG
	AAAA	BBBB	#1

SECOND DOWNWARD VCC TABLE

FOR #1	OUTPUT VPI	OUTPUT VCI	TAG
AA.+BB. ↓	XXXX	YYYYY	#A

FIG. 881

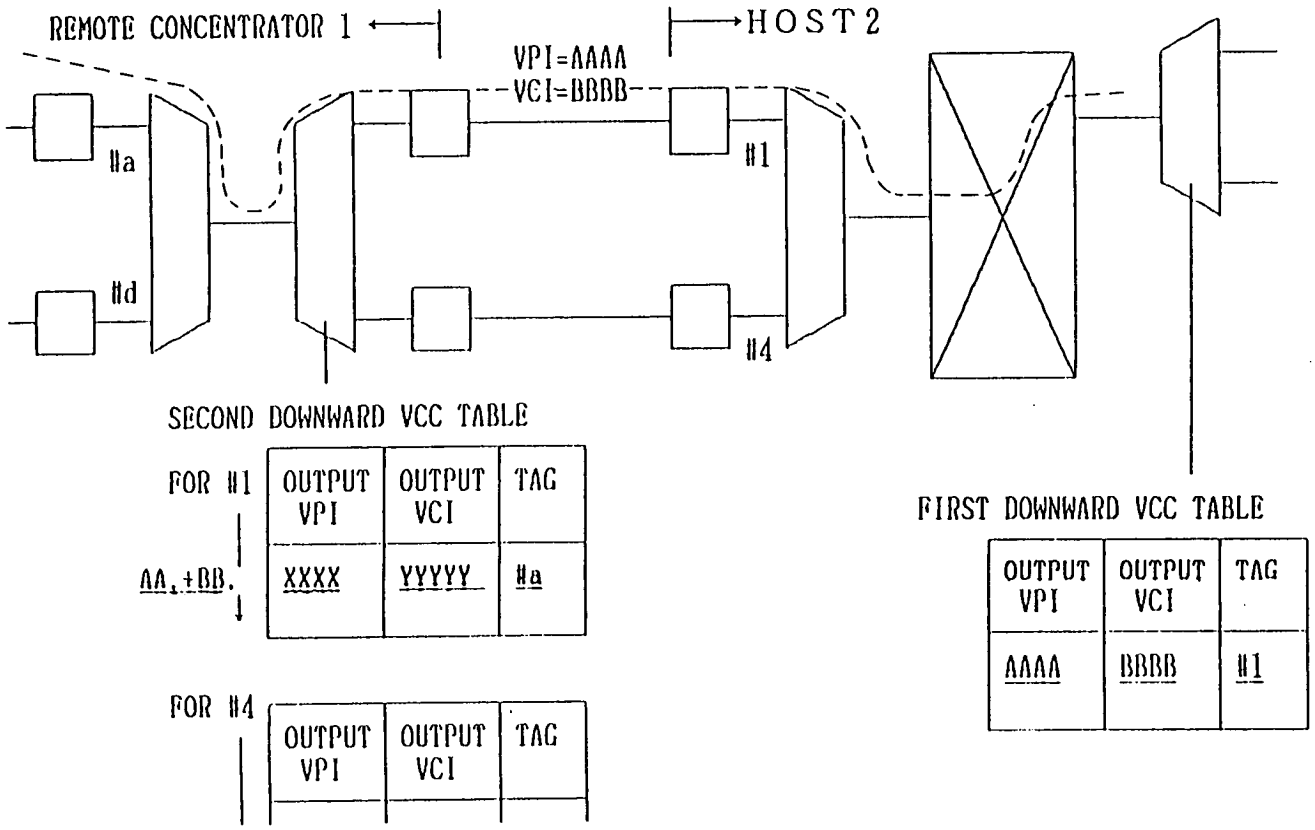

REMOTE CONCENTRATOR 1
HOST 2
VPI=AAAA
VCI=BBBB
#a
#d
#1
#4
SECOND DOWNWARD VCC TABLE
FOR #1
OUTPUT VPI
OUTPUT VCI
TAG
AA,+BB.
XXXX
YYYYY
#a
FOR #4
OUTPUT VPI
OUTPUT VCI
TAG
FIRST DOWNWARD VCC TABLE
OUTPUT VPI
OUTPUT VCI
TAG
AAAA
BBBB
#1

FIG. 882

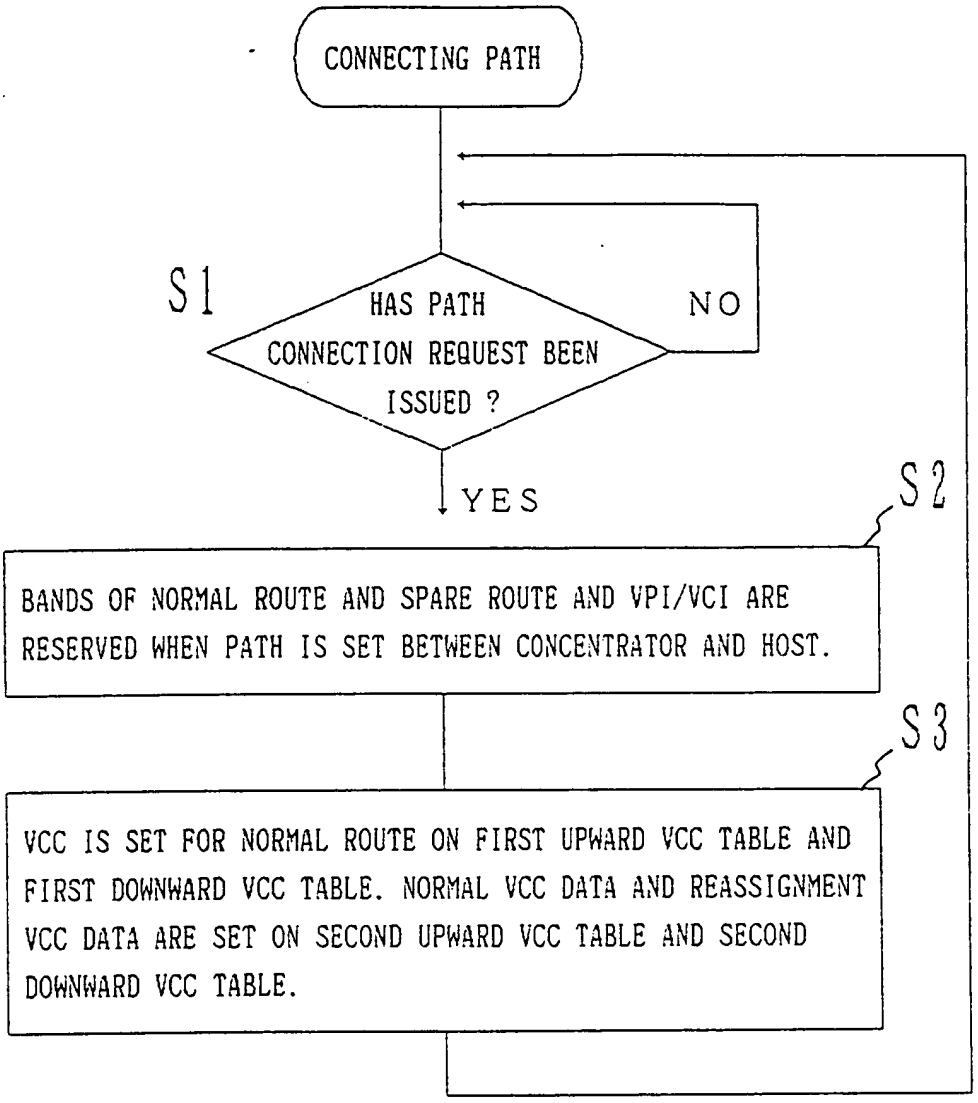

CONNECTING PATH
S1
HAS PATH CONNECTION REQUEST BEEN ISSUED ?
NO
YES
S2
BANDS OF NORMAL ROUTE AND SPARE ROUTE AND VPI/VCI ARE RESERVED WHEN PATH IS SET BETWEEN CONCENTRATOR AND HOST.
S3
VCC IS SET FOR NORMAL ROUTE ON FIRST UPWARD VCC TABLE AND FIRST DOWNWARD VCC TABLE. NORMAL VCC DATA AND REASSIGNMENT VCC DATA ARE SET ON SECOND UPWARD VCC TABLE AND SECOND DOWNWARD VCC TABLE.

FIG. 883

NORMAL VCC DATA			REASSIGNMENT VCC DATA		
OUTPUT VCC	OUTPUT VCI	TAG	OUTPUT VPI	OUTPUT VCI	TAG
AAAA	BBBB	#1	CCCC	DDDDD	#4

FIG. 884

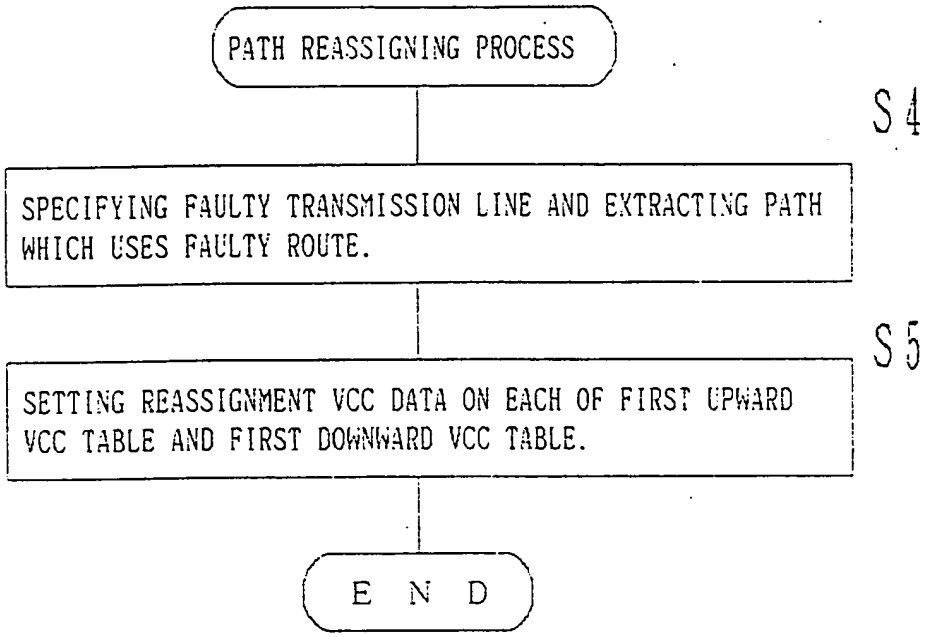
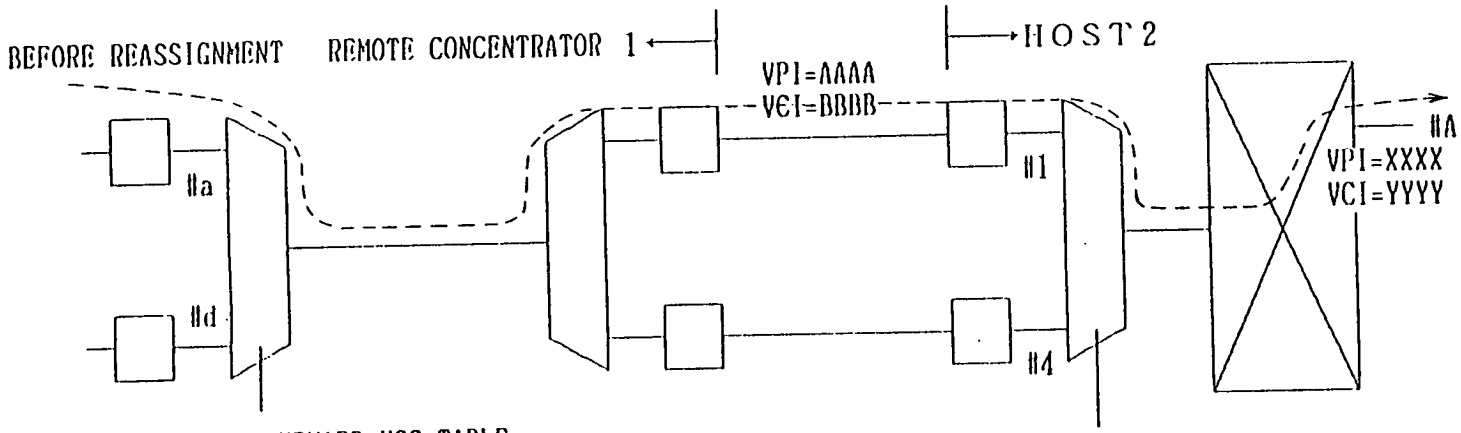

PATH REASSIGNING PROCESS
S4
SPECIFYING FAULTY TRANSMISSION LINE AND EXTRACTING PATH WHICH USES FAULTY ROUTE.
S5
SETTING REASSIGNMENT VCC DATA ON EACH OF FIRST UPWARD VCC TABLE AND FIRST DOWNWARD VCC TABLE.
E N D

FIG. 885



NORMAL VCC DATA | REASSIGNMENT VCC DATA

#a

	OUTPUT VPI	OUTPUT VCI	TAG	OUTPUT VPI	OUTPUT VCI	TAG
0	AAAA	BBBB	#1	CCCC	DDDDD	#4

0 : NORMAL VCC TABLE 1 : REASSIGNMENT VCC TABLE

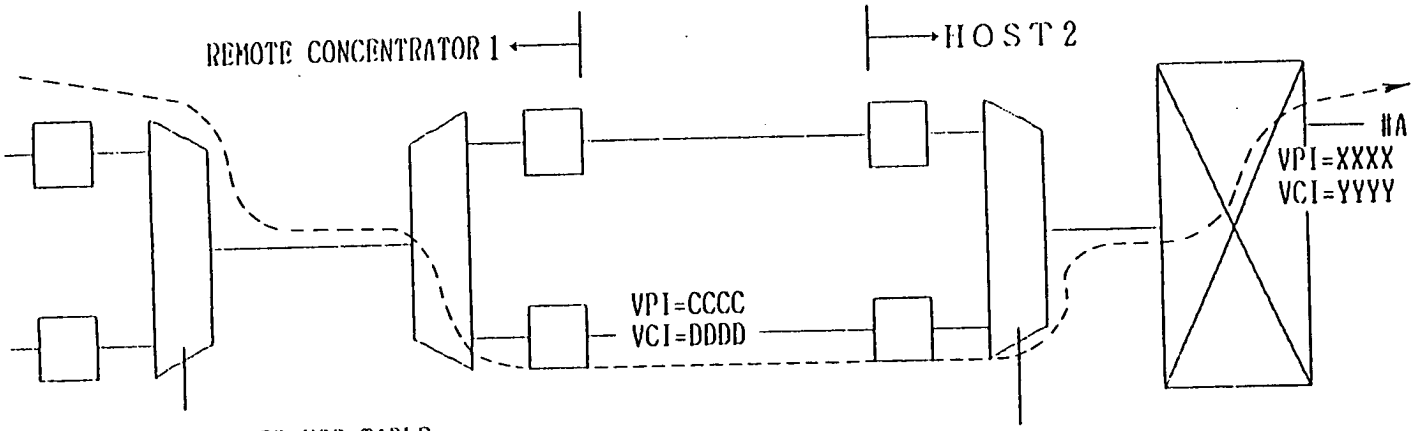
FOR #1 (AA.+BB.)

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#4

FOR #4 (CC.+DD.)

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#4

FIG. 886



NORMAL VCC DATA / REASSIGNMENT VCC DATA

S	OUTPUT VPI	OUTPUT VCI	TAG	OUTPUT VPI	OUTPUT VCI	TAG
1	AAAA	BBBB	#1	CCCC	DDDDD	#4

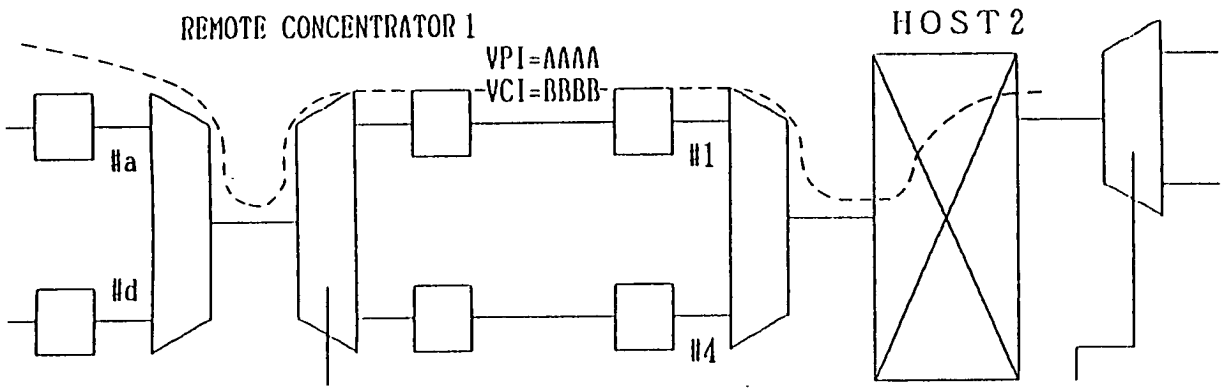
FOR #1

AA.+BB.	OUTPUT VPI	OUTPUT VCI	TAG
	XXXX	YYYYY	#4

FOR #4

CC.+DD.	OUTPUT VPI	OUTPUT VCI	TAG
	XXXX	YYYYY	#4

FIG. 887



SECOND DOWNWARD VCC TABLE

FOR #1

AA.+BB.

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#a

FOR #4

CC.+DD.

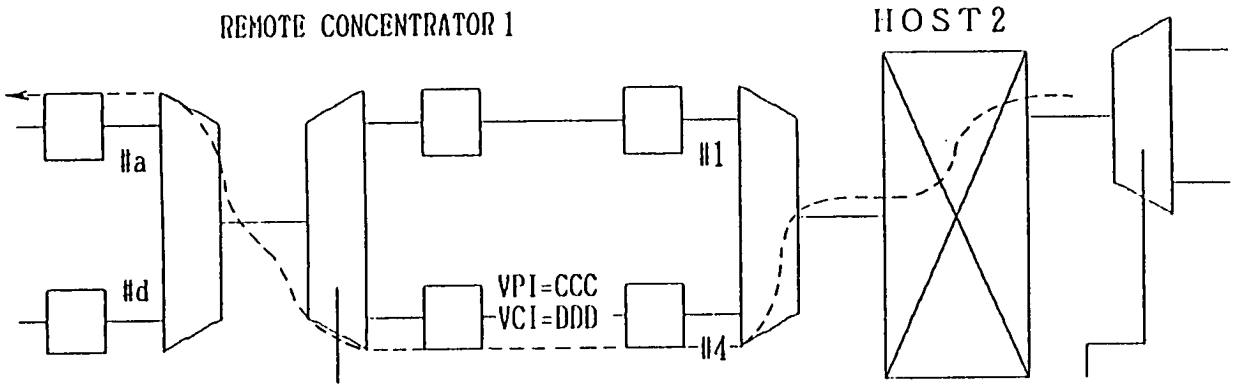
OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#a

FIRST DOWNWARD VCC TABLE

	NORMAL VCC DATA			REASSIGNMENT VCC DATA		
	OUTPUT VPI	OUTPUT VCI	TAG	OUTPUT VPI	OUTPUT VCI	TAG
0	AAAA	BBBB	#1	CCCC	DDDDD	#4

0 ; NORMAL VCC TABLE 1 ; REASSIGNMENT VCC TABLE

FIG. 888



SECOND DOWNWARD VCC TABLE

FOR #1

AA.+BB.

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#a

FOR #4

CC.+DD.

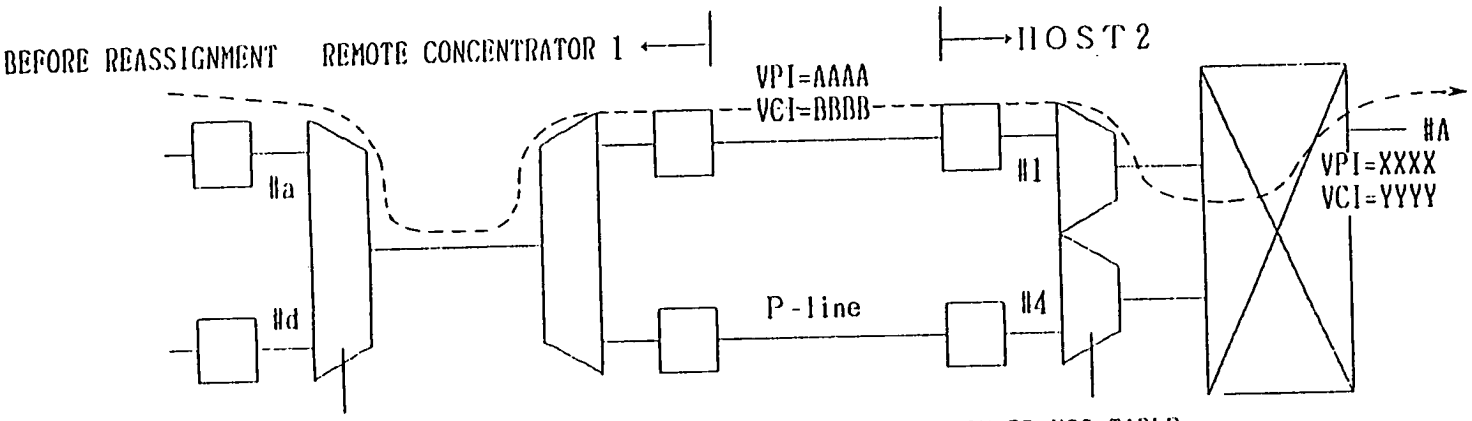
OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#a

FIRST DOWNWARD VCC TABLE

	NORMAL VCC DATA			REASSIGNMENT VCC DATA		
	OUTPUT VPI	OUTPUT VCI	TAG	OUTPUT VPI	OUTPUT VCI	TAG
1	AAAA	BBBB	#1	CCCC	DDDDD	#4

0 ; NORMAL VCC TABLE 1 ; REASSIGNMENT VCC TABLE

FIG. 889



FIRST UPWARD VCC TABLE

	OUTPUT VPI	OUTPUT VCI	TAG
#a	AAAA	BBBB	#1

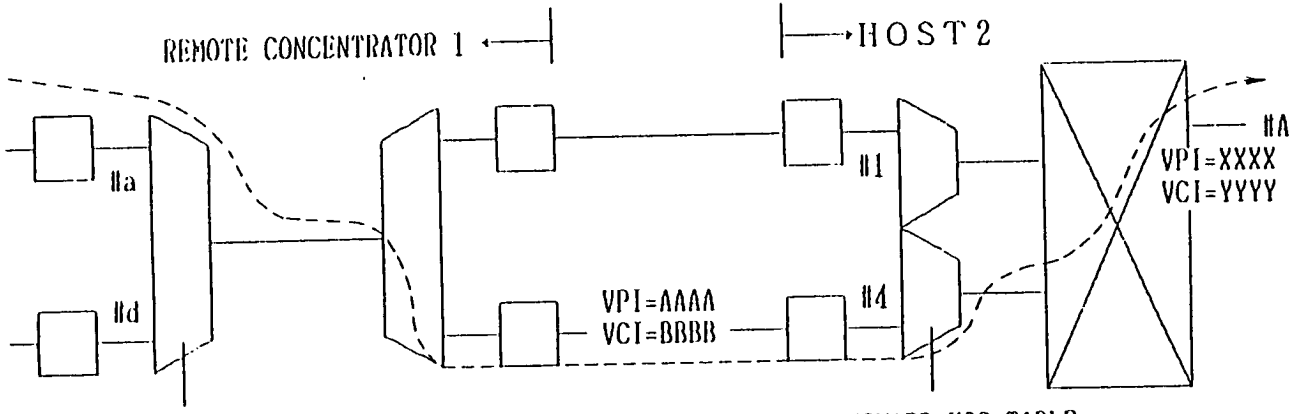
SECOND UPWARD VCC TABLE

	OUTPUT VPI	OUTPUT VCI	TAG
FOR #1 AA.+BB.	XXXX	YYYYY	#4

FOR #4

OUTPUT VPI	OUTPUT VCI	TAG
BLANK	BLANK	

FIG. 890



FIRST UPWARD VCC TABLE

OUTPUT VPI	OUTPUT VCC	TAG
AAAA	BBBB	#4

SECOND UPWARD VCC TABLE

FOR #1

AA.+BB.

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#4

FOR #4

AA.+BB.

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#4

FIG. 8 9 1

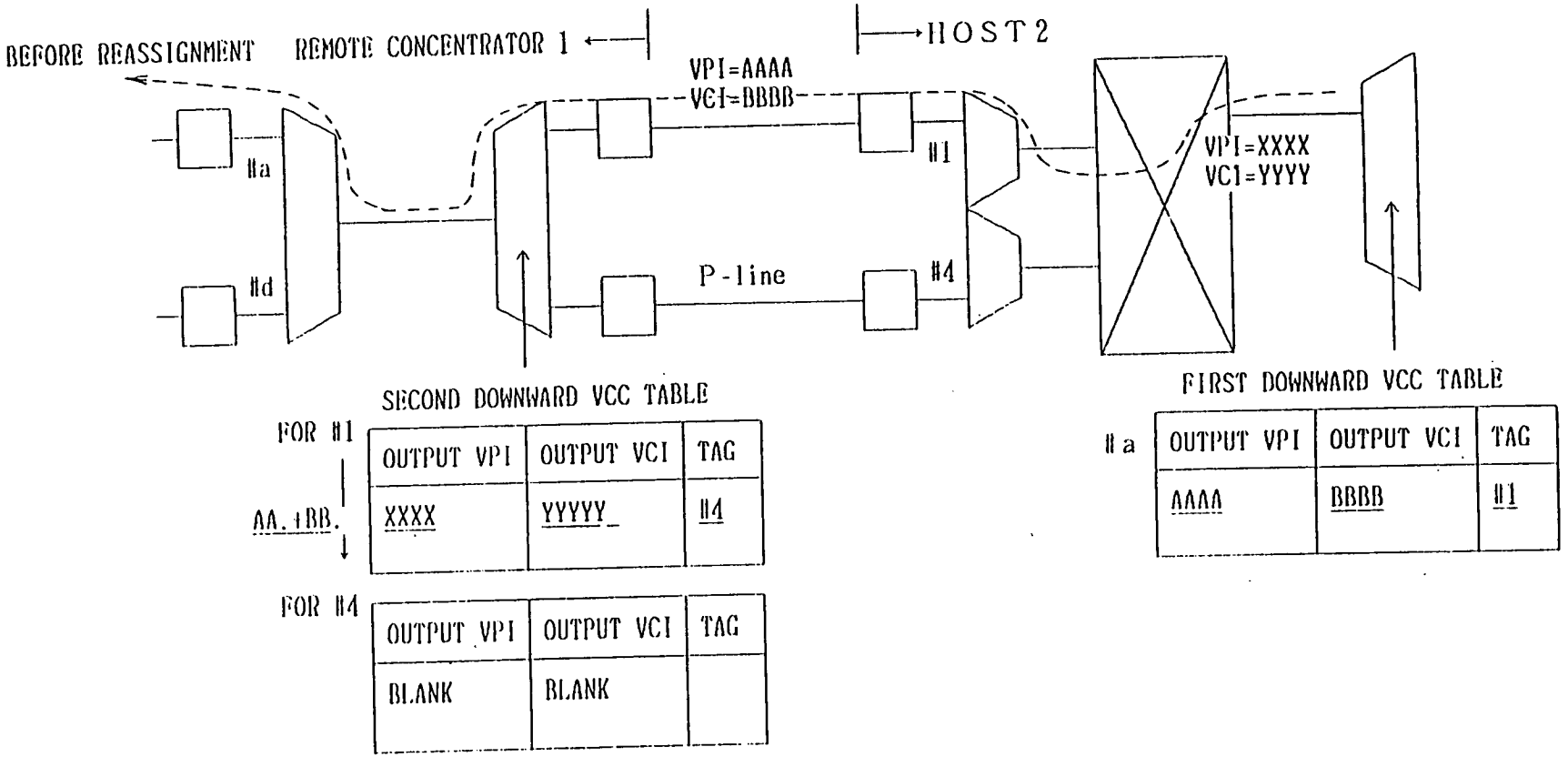
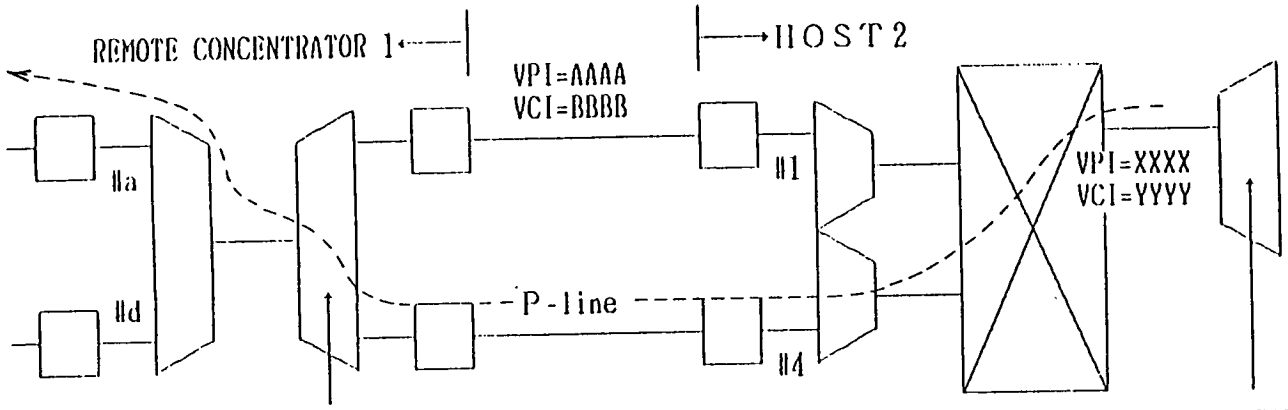

BEFORE REASSIGNMENT
REMOTE CONCENTRATOR 1
HOST 2
VPI=AAAA
VCI=BBBB
#a
#d
#1
#4
P-line
VPI=XXXX
VCI=YYYY
SECOND DOWNWARD VCC TABLE
FOR #1
AA.+BB.
OUTPUT VPI
OUTPUT VCI
TAG
XXXX
YYYYY
#4
FOR #4
OUTPUT VPI
OUTPUT VCI
TAG
BLANK
BLANK
FIRST DOWNWARD VCC TABLE
#a
OUTPUT VPI
OUTPUT VCI
TAG
AAAA
BBBB
#1

FIG. 892



SECOND DOWNWARD VCC TABLE

FOR #1

AA.+BB.

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#4

FOR #4

AA.+BB.

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#4

FIRST DOWNWARD VCC TABLE

#a

OUTPUT VPI	OUTPUT VPI	TAG
AAAA	BBBB	#4

FIG. 893

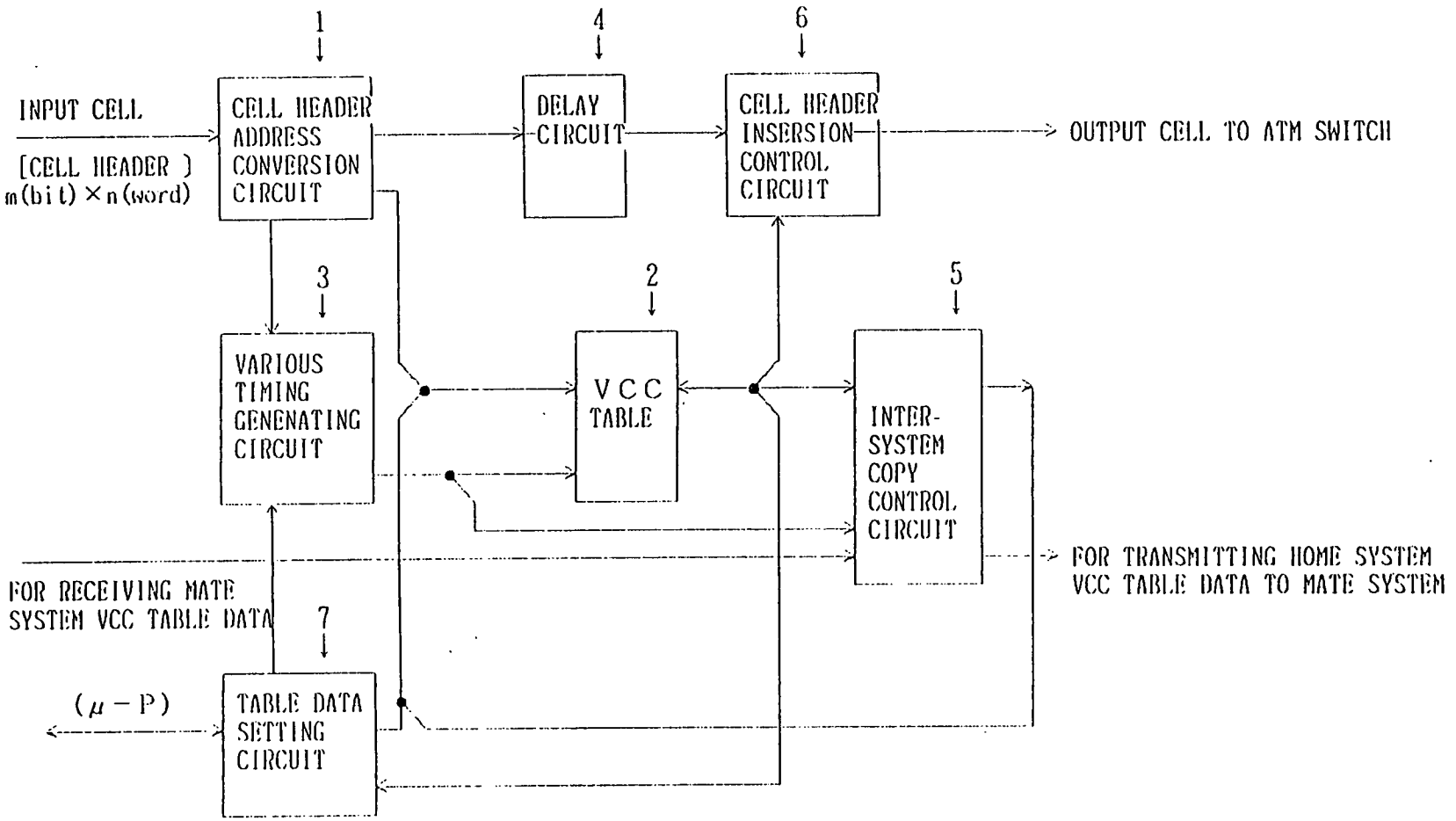

1
4
6
INPUT CELL
[CELL HEADER]
m(bit)×n(word)
CELL HEADER ADDRESS CONVERSION CIRCUIT
DELAY CIRCUIT
CELL HEADER INSERSION CONTROL CIRCUIT
OUTPUT CELL TO ATM SWITCH
3
2
5
VARIOUS TIMING GENENATING CIRCUIT
VCC TABLE
INTER-SYSTEM COPY CONTROL CIRCUIT
FOR TRANSMITTING HOME SYSTEM VCC TABLE DATA TO MATE SYSTEM
FOR RECEIVING MATE SYSTEM VCC TABLE DATA
7
(μ-P)
TABLE DATA SETTING CIRCUIT

FIG. 894

[VCC TABLE ACCESS TIMING USING INPUT CELL]

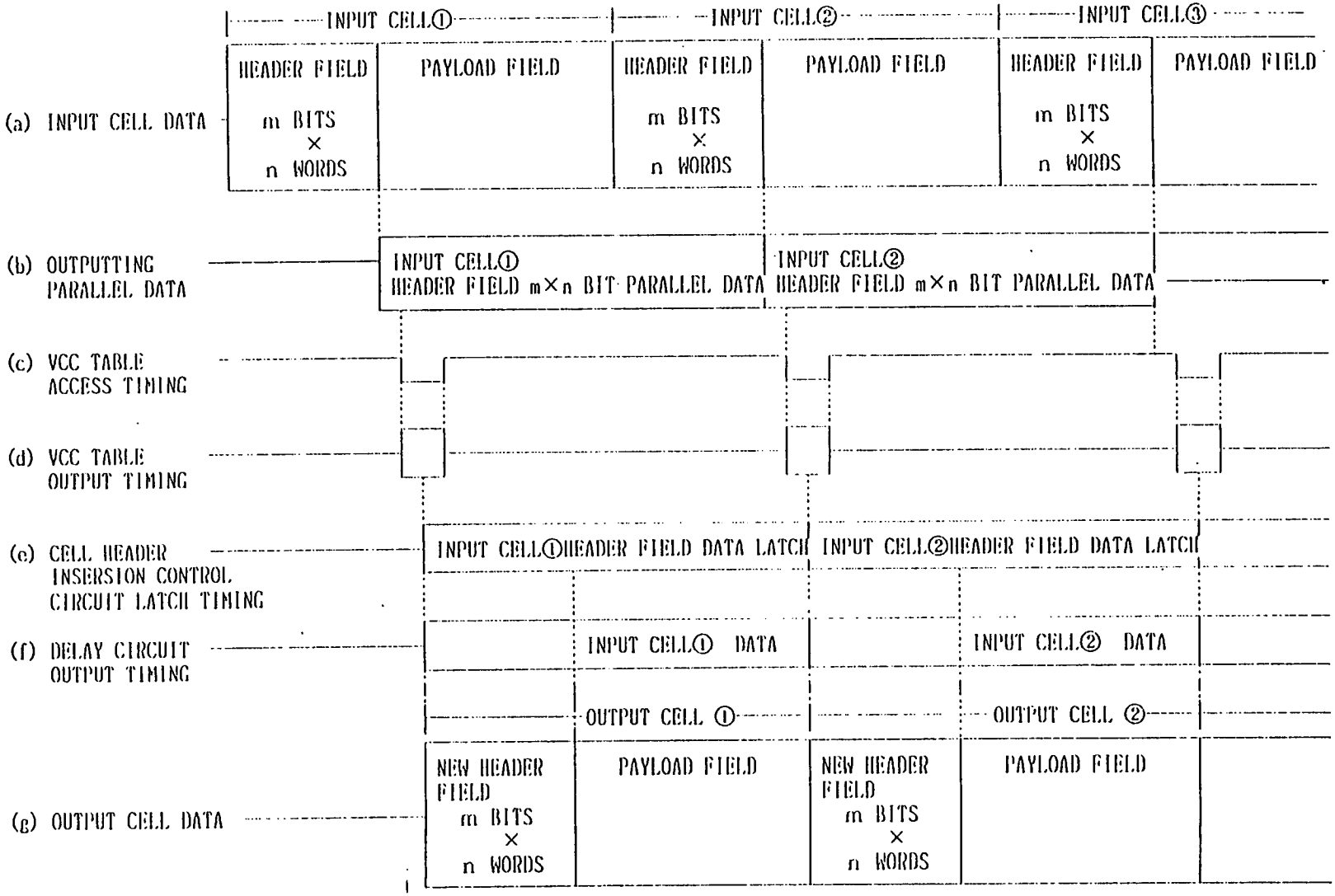


FIG. 895

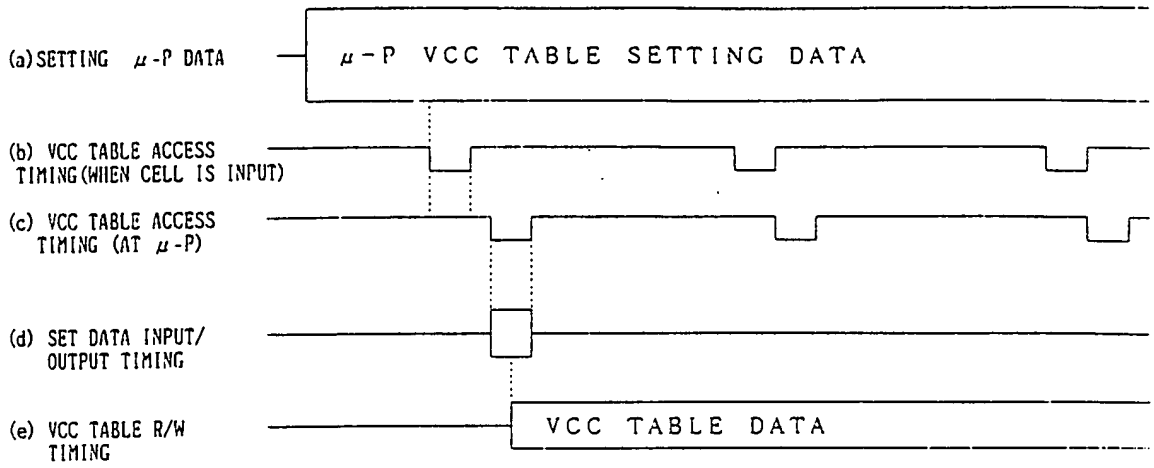


FIG. 896A

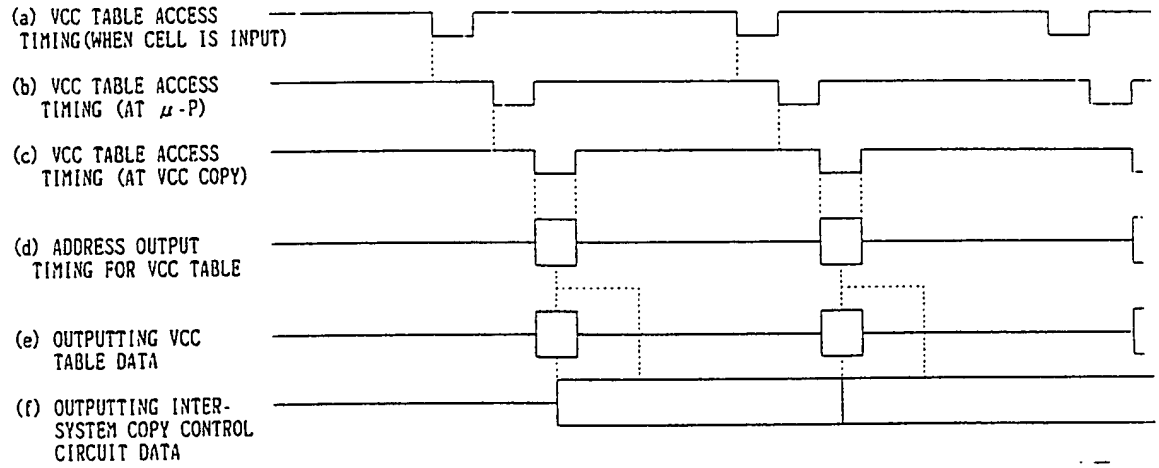


FIG. 896B

6692E0 "ET2Z260

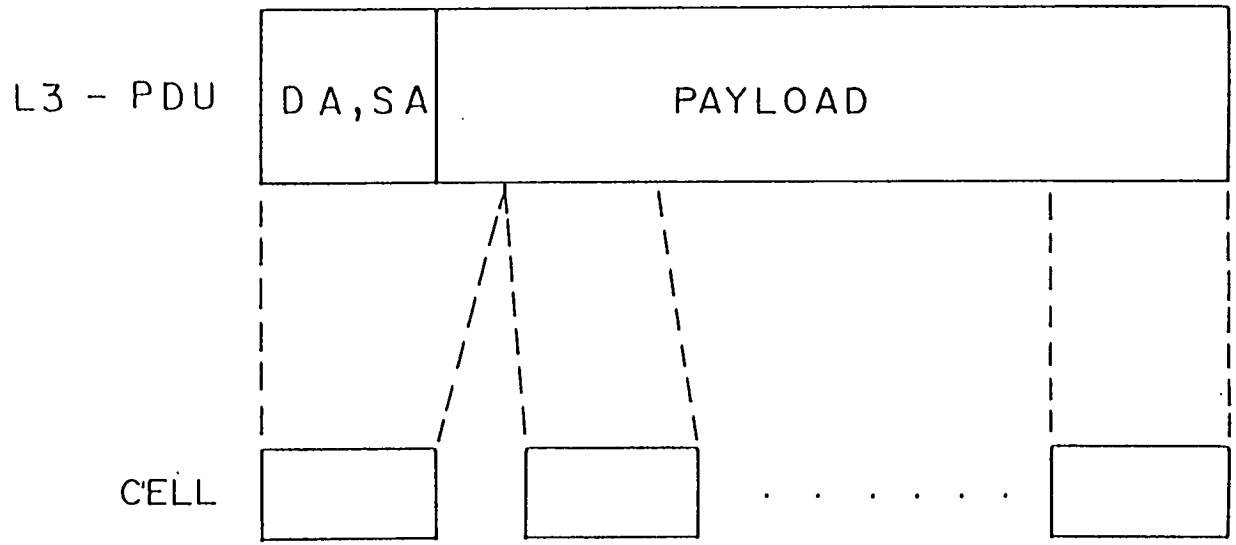


FIG. 897

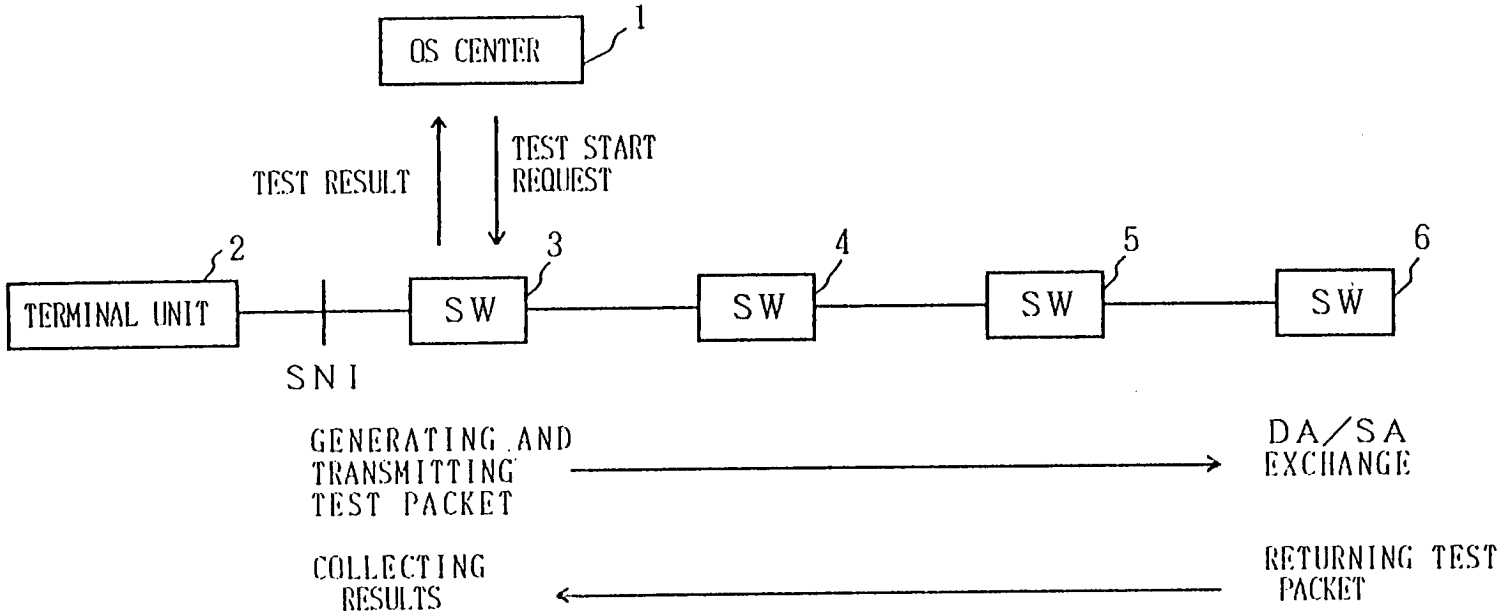

OS CENTER
1
TEST RESULT
TEST START REQUEST
2
3
4
5
6
TERMINAL UNIT
SW
SW
SW
SW
SNI
GENERATING AND TRANSMITTING TEST PACKET
DA/SA EXCHANGE
COLLECTING RESULTS
RETURNING TEST PACKET

FIG. 898

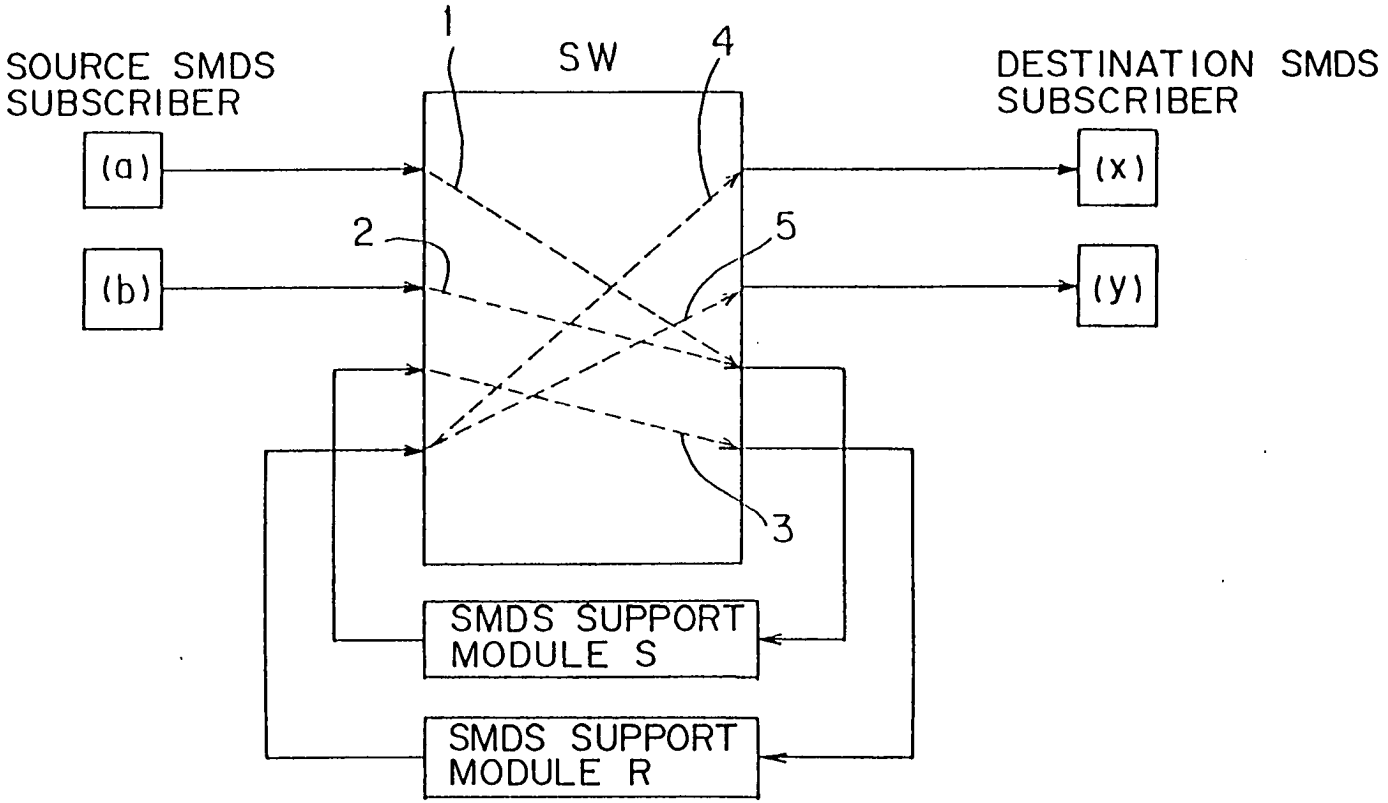

SOURCE SMDS SUBSCRIBER
(a)
(b)
1
SW
4
2
5
3
DESTINATION SMDS SUBSCRIBER
(x)
(y)
SMDS SUPPORT MODULE S
SMDS SUPPORT MODULE R

FIG. 899

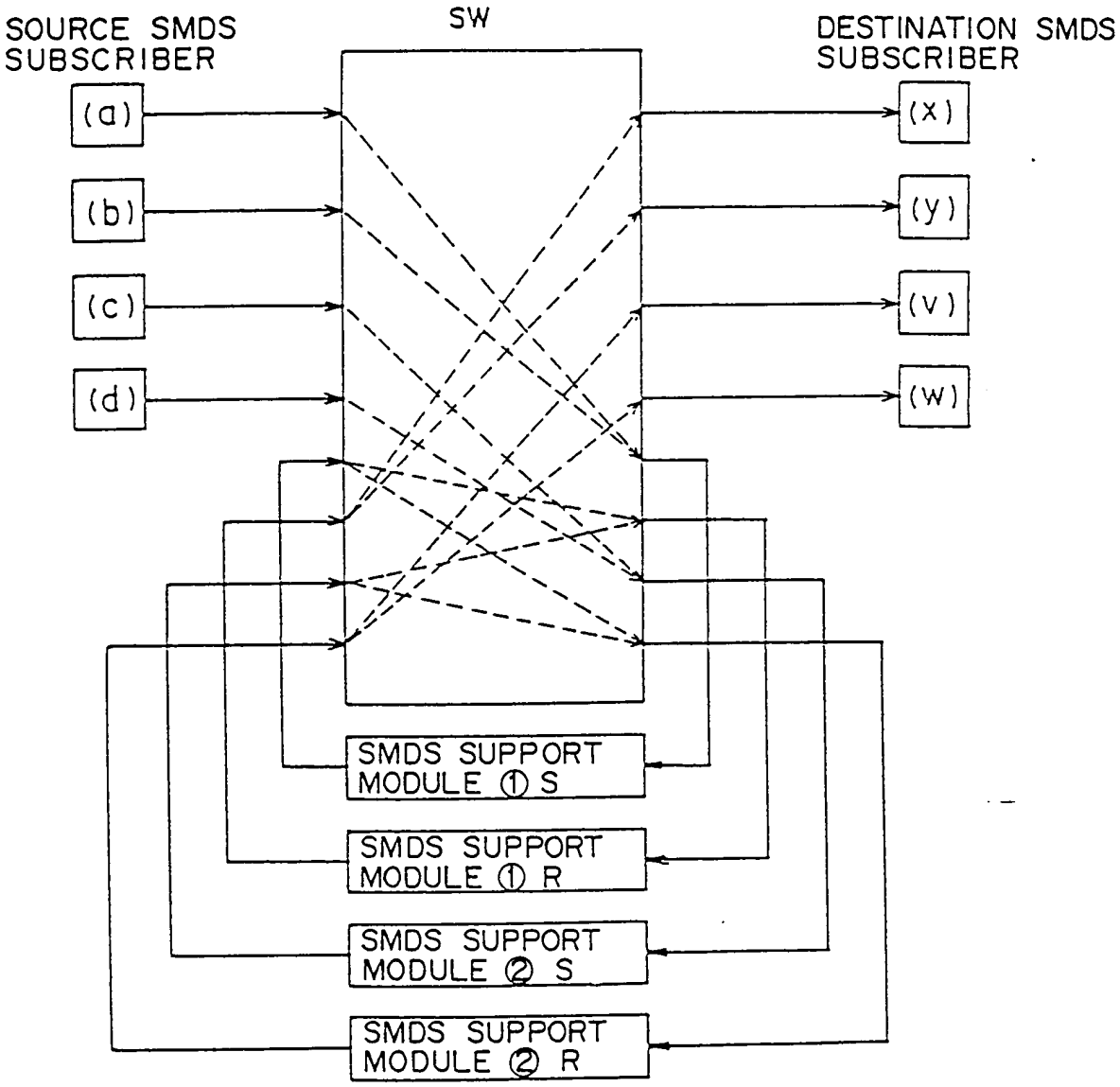

SOURCE SMDS SUBSCRIBER
SW
DESTINATION SMDS SUBSCRIBER
(a)
(b)
(c)
(d)
(x)
(y)
(v)
(w)
SMDS SUPPORT MODULE ① S
SMDS SUPPORT MODULE ① R
SMDS SUPPORT MODULE ② S
SMDS SUPPORT MODULE ② R

FIG. 900

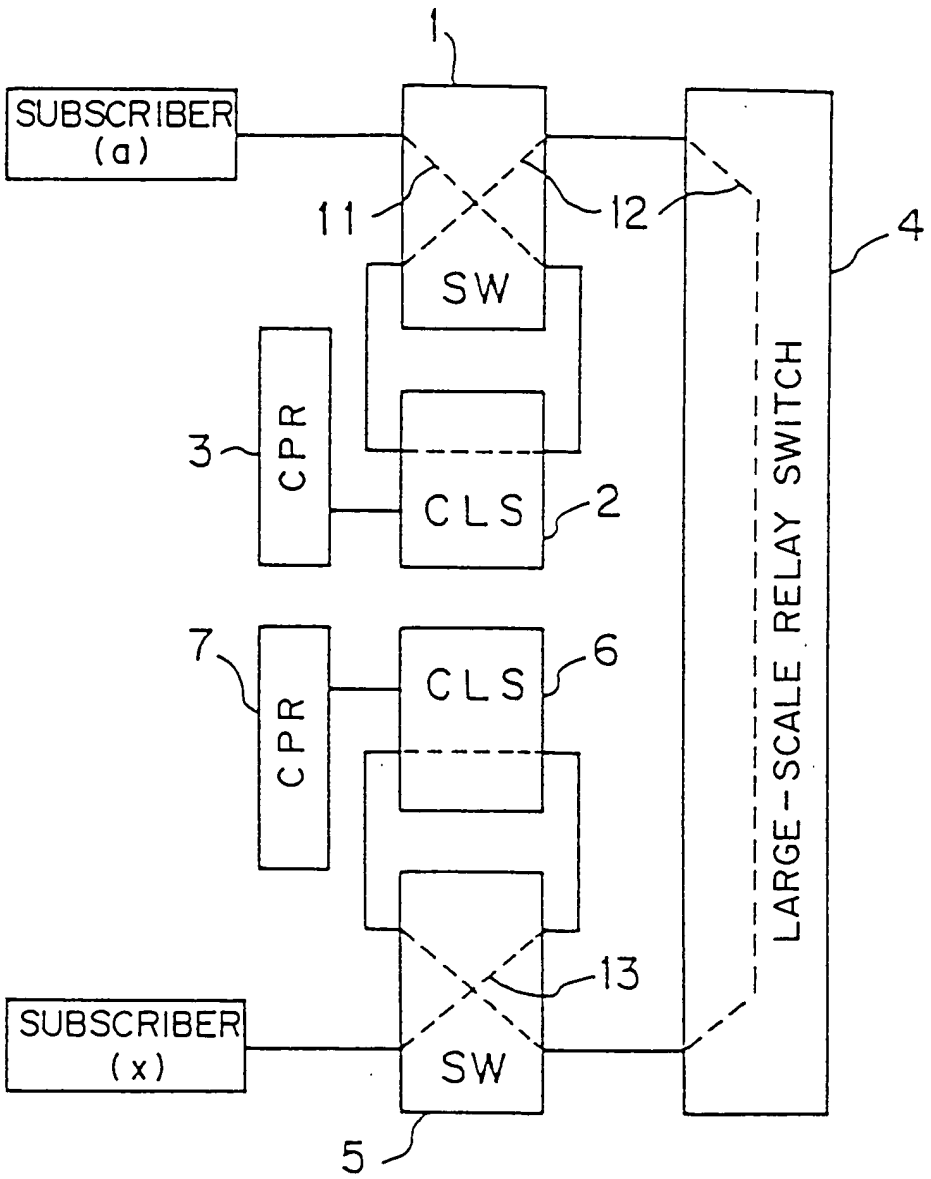

1
SUBSCRIBER
(a)
11
12
4
SW
3
CPR
CLS
2
7
CPR
CLS
6
LARGE-SCALE RELAY SWITCH
13
SUBSCRIBER
(x)
SW
5

FIG. 901

69260 EP 2 727 260

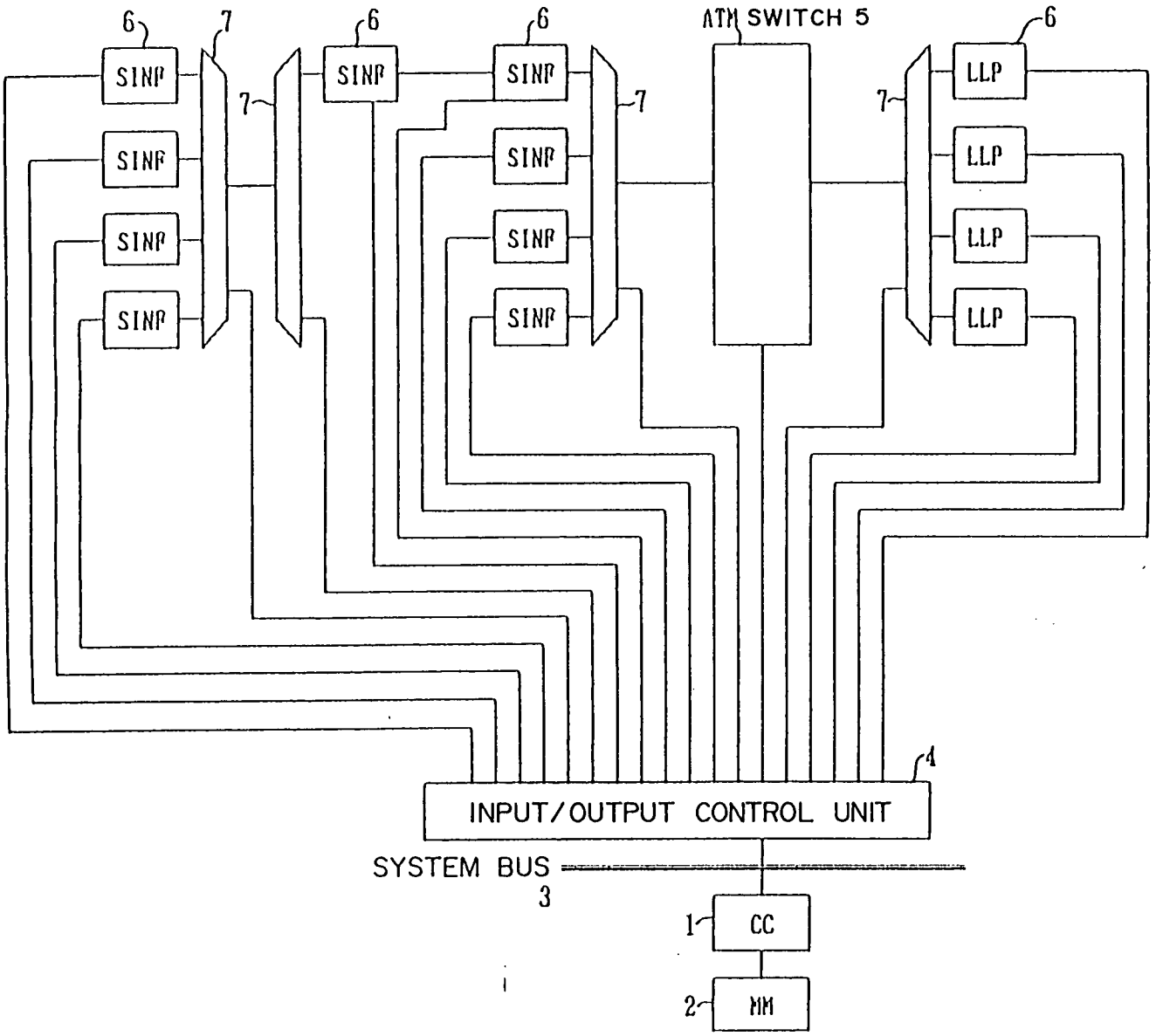


FIG. 902

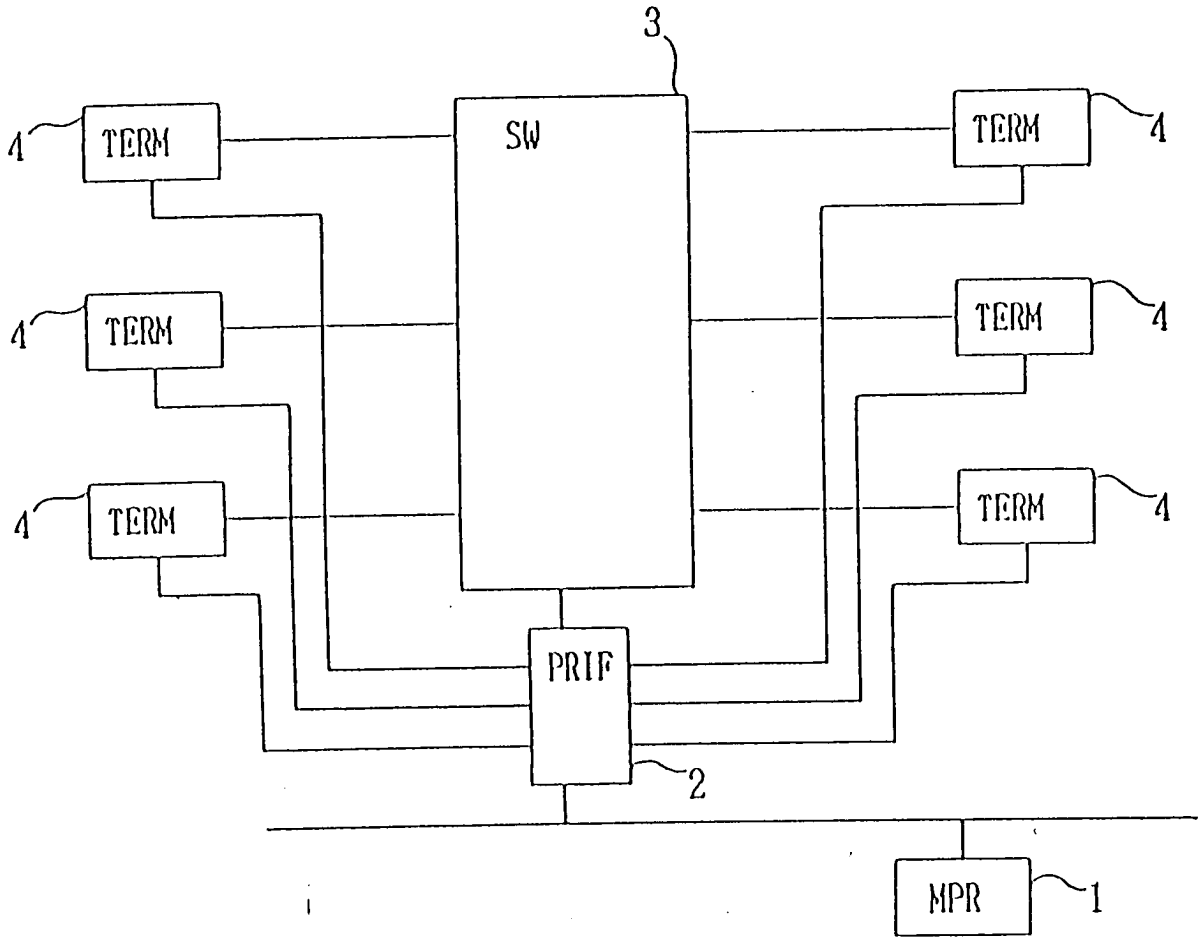


FIG. 903

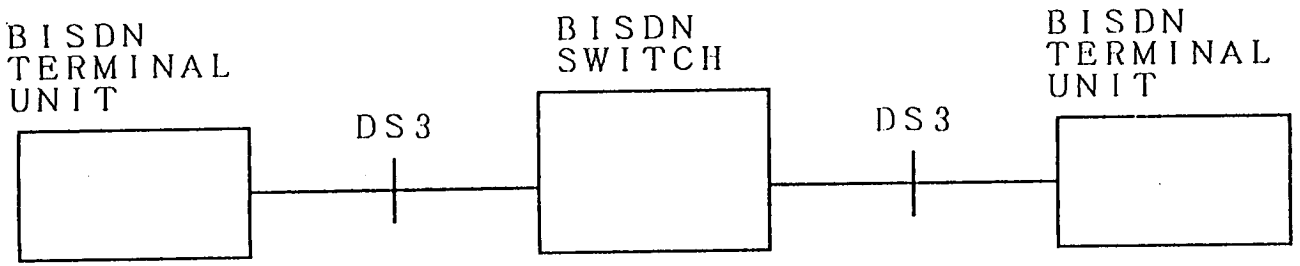

BISDN
TERMINAL
UNIT
DS3
BISDN
SWITCH
DS3
BISDN
TERMINAL
UNIT

FIG. 904

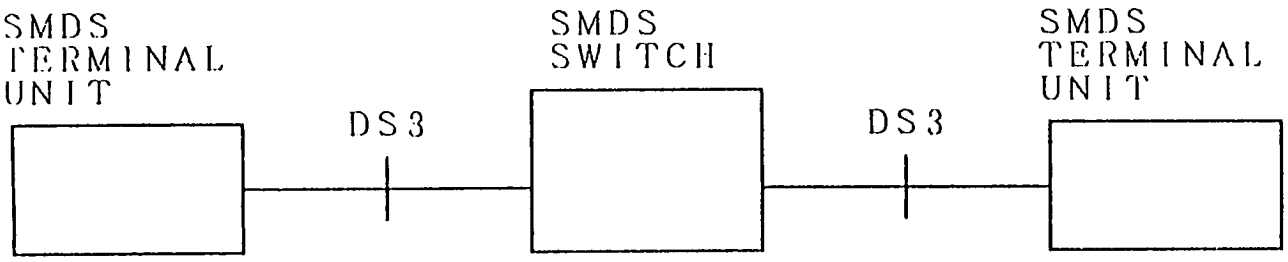
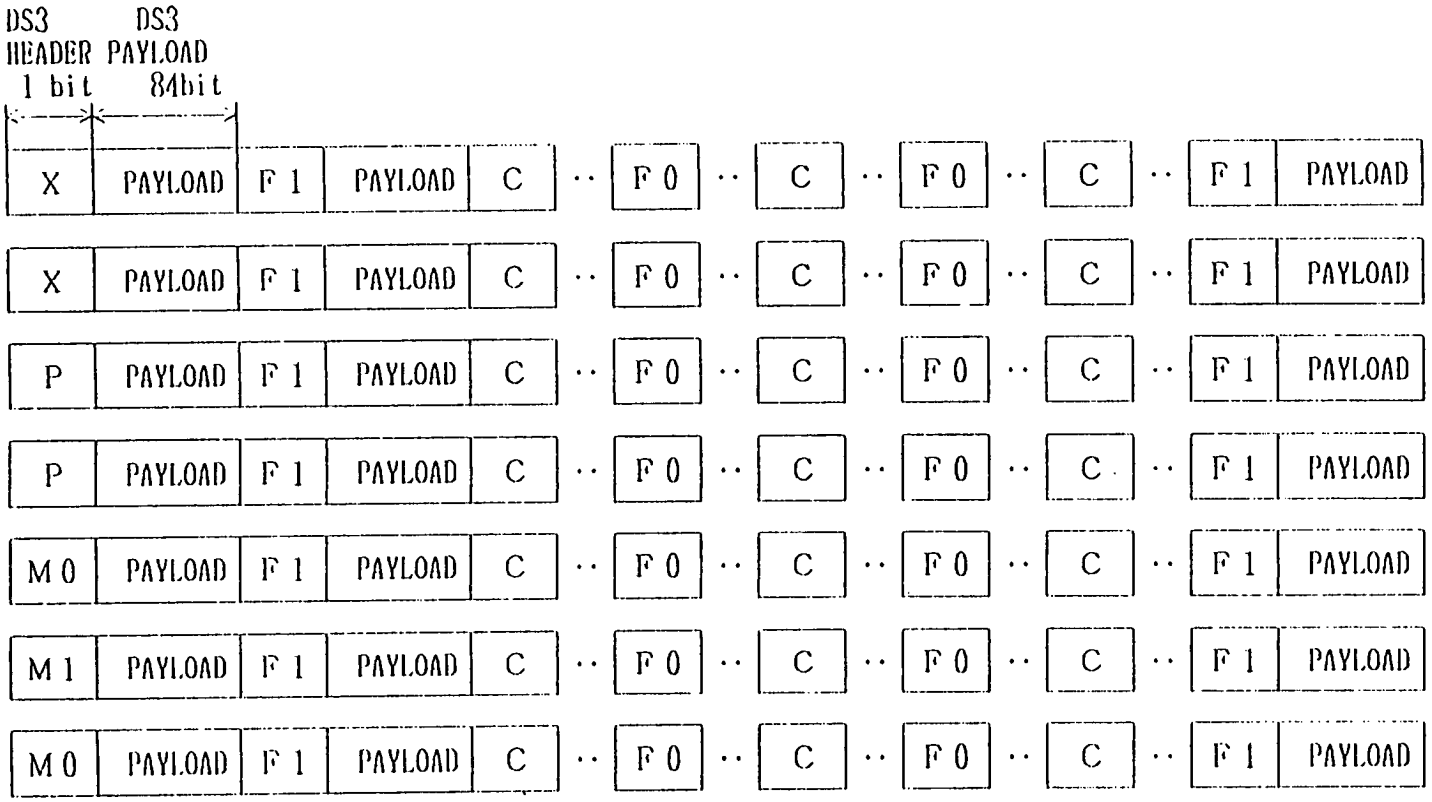


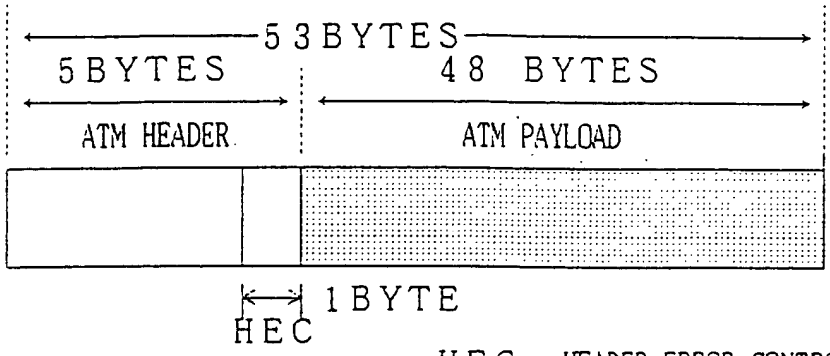
FIG. 905



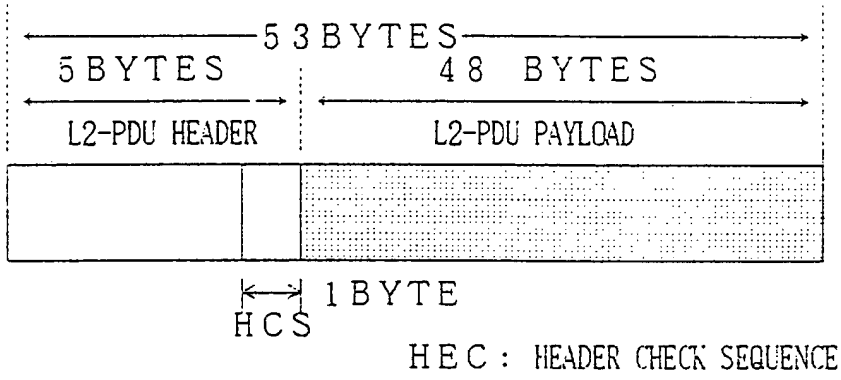
DS3 MULTIFRAME = 4760 BITS (85 BITS × 8 × 7)

F0, F1 : SUBFRAME ALIGNMENT BIT
M0, M1 : MULTIFRAME ALIGNMENT BIT
P : PARITY INFORMATION BIT
X : ERROR STATE DESIGNATION BIT
C (RESERVED)

FIG. 906



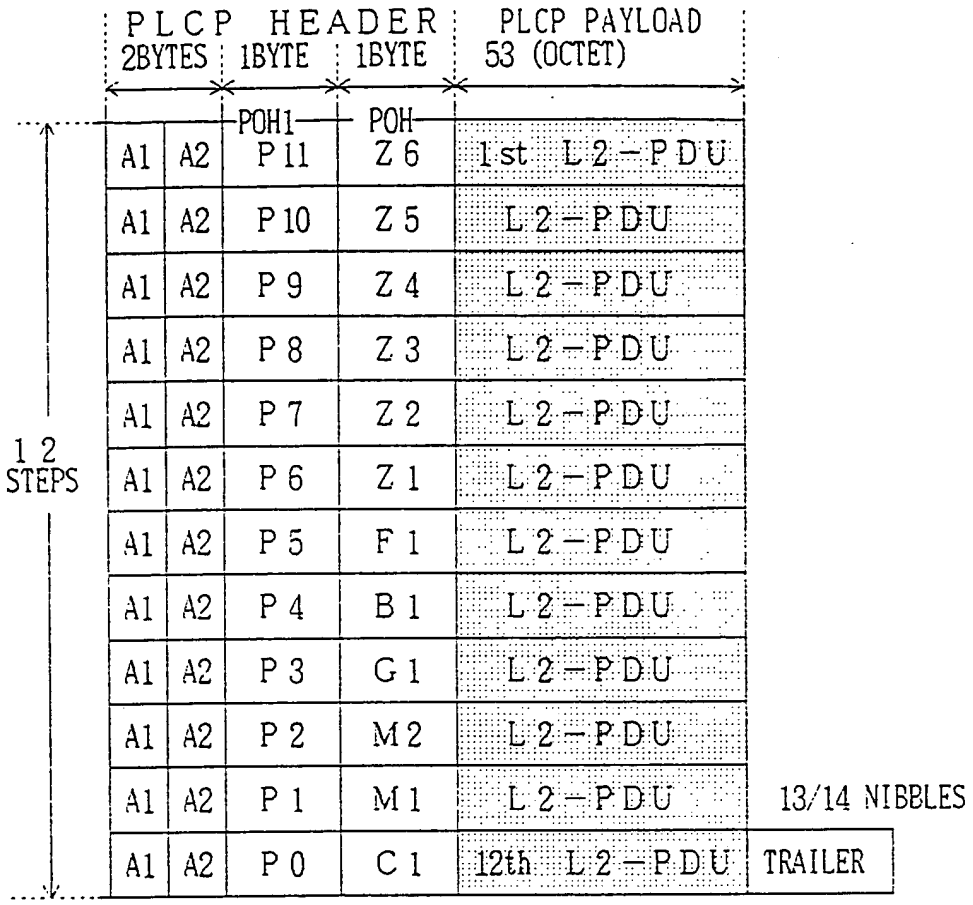
(a) CONFIGURATION OF ATM CELL



(b) CONFIGURATION OF SMDS CELL

FIG. 907

0353-5252-0868



A1, A2 : FRAME ALIGNMENT
POHI (P11~P0) : PATH OVERHEAD IDENTIFIER OCTET
POH : PATH OVERHEAD OCTET
Z6~Z1 : GROSS OCTET
F1 : PLCP PATH USER CHANNEL
B1 : BIT INTERVAL PARITY 8
G1 : PLCP PATH STATUS
M2~M1 : SIP LEVEL 1 CONTROL INFORMATION
C1 : CYCLE STUFF COUNTER

FIG. 908

ITEM		BIT PATTERN	REMARKS
C1	CYCLE STUFF COUNTER		TL IS REPRESENTED BY 4 TYPES OF C1 AS SHOWN BELOW BECAUSE TRAILER LENGTH TL PERIODICALLY CHANGES IN DS3 PLCP FRAME.
		11111111	⟹ FIRST TYPE (TL=13)
		00000000	⟹ SECOND TYPE (TL=14)
		01100110	⟹ THIRD TYPE (TL=13 : NO STUFF)
		10011001	⟹ THIRD TYPE (TL=14 : STUFF)
TRAILER		1100	LENGTH DEPENDS ON C1 BYTE VALUE.

FIG. 909

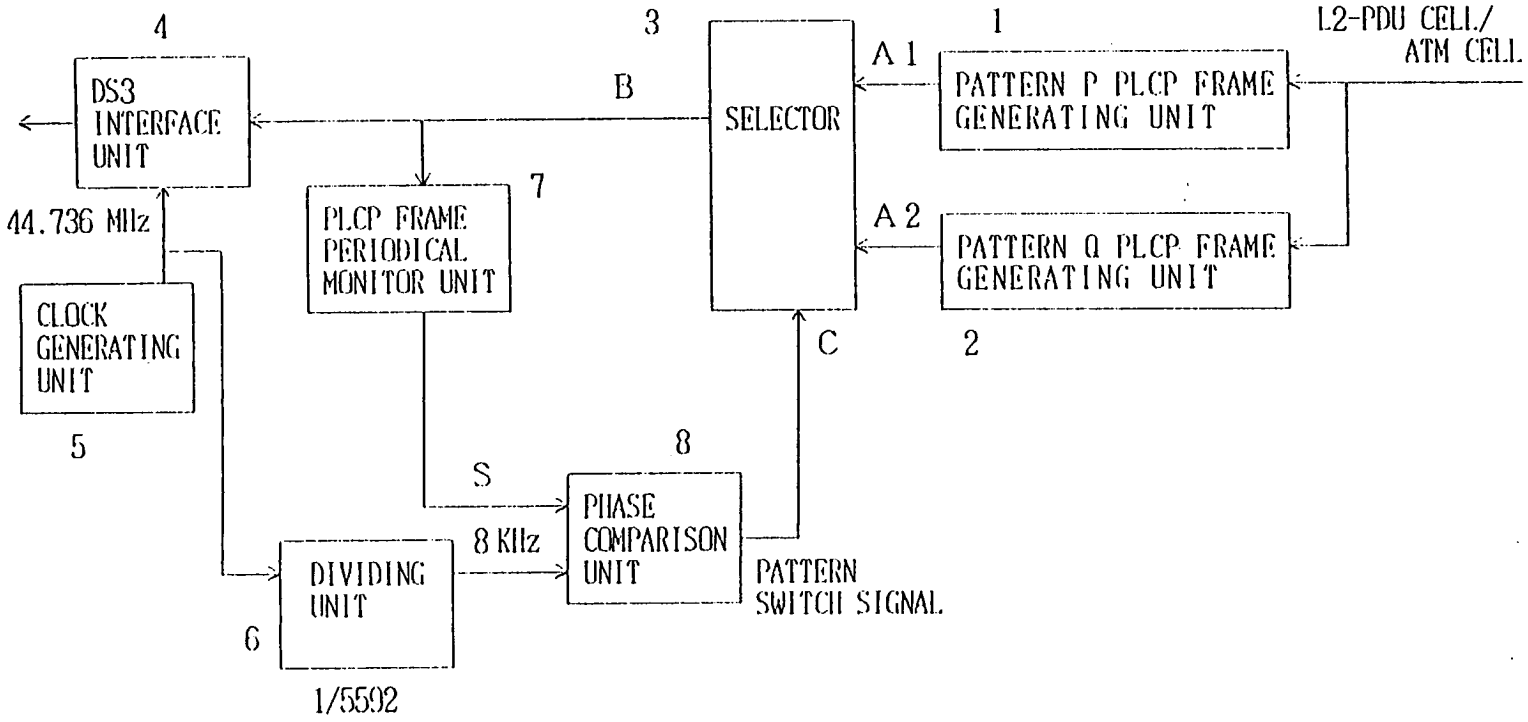

4
3
1
L2-PDU CELL/
ATM CELL
DS3
INTERFACE
UNIT
B
SELECTOR
A 1
PATTERN P PLCP FRAME
GENERATING UNIT
7
44.736 MHz
PLCP FRAME
PERIODICAL
MONITOR UNIT
A 2
CLOCK
GENERATING
UNIT
PATTERN Q PLCP FRAME
GENERATING UNIT
C
2
5
8
S
PHASE
COMPARISON
UNIT
8 KHz
DIVIDING
UNIT
PATTERN
SWITCH SIGNAL
6
1/5502

FIG. 910

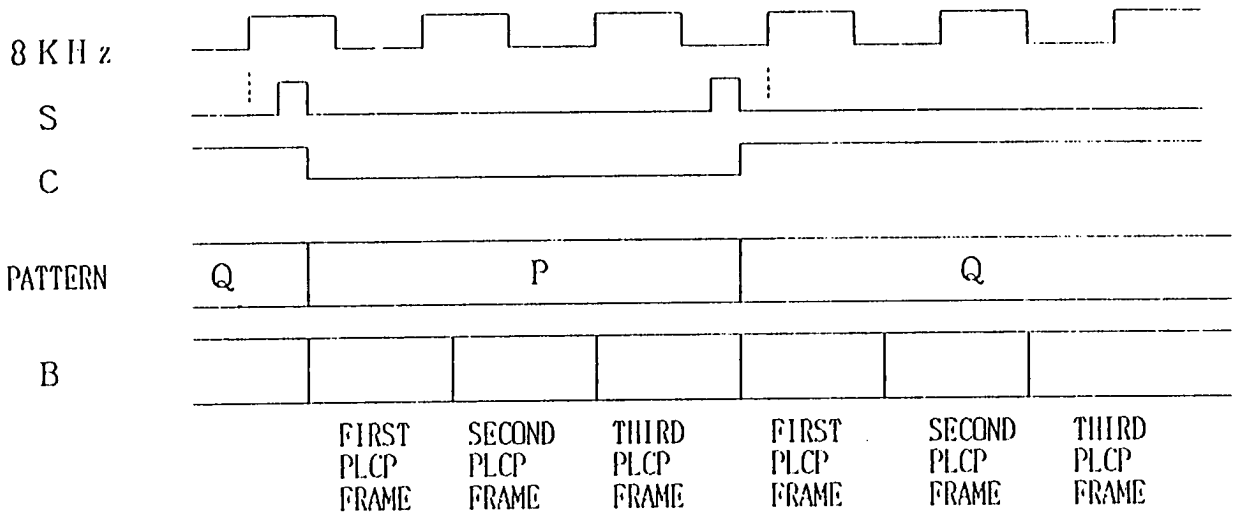
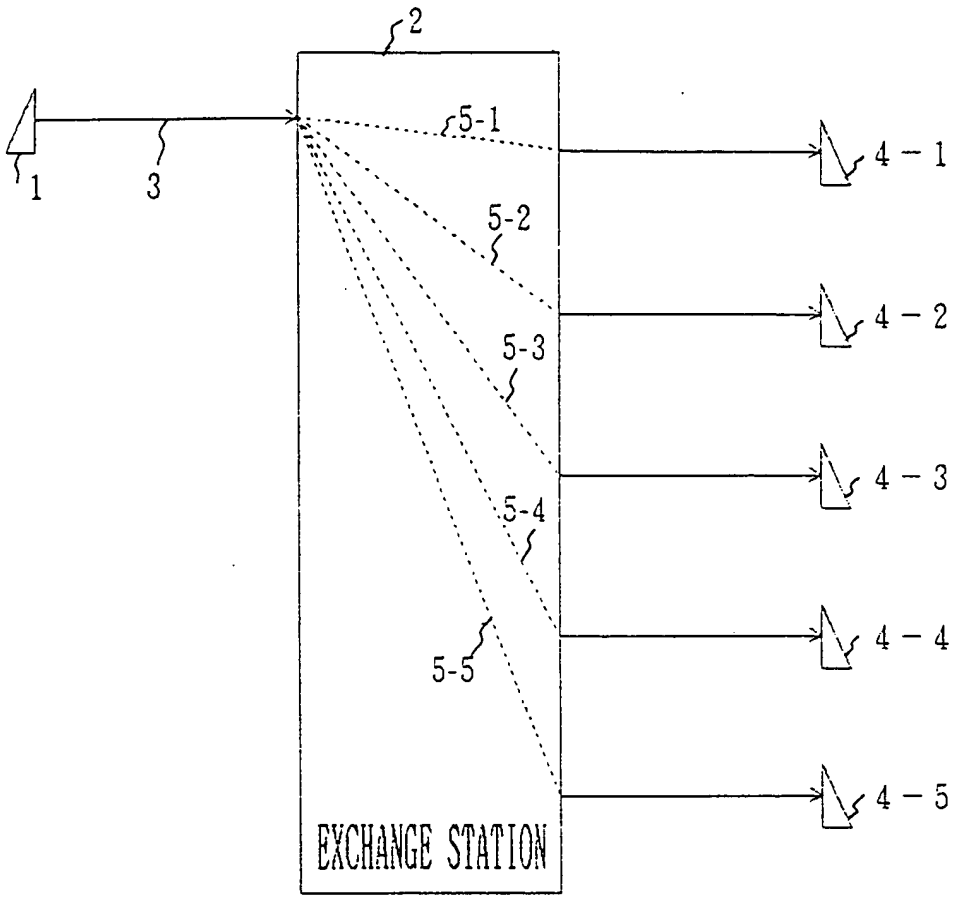

8 KHz
S
C
PATTERN
Q
P
Q
B
FIRST PLCP FRAME
SECOND PLCP FRAME
THIRD PLCP FRAME
FIRST PLCP FRAME
SECOND PLCP FRAME
THIRD PLCP FRAME

FIG. 911



F I G. 9 1 2

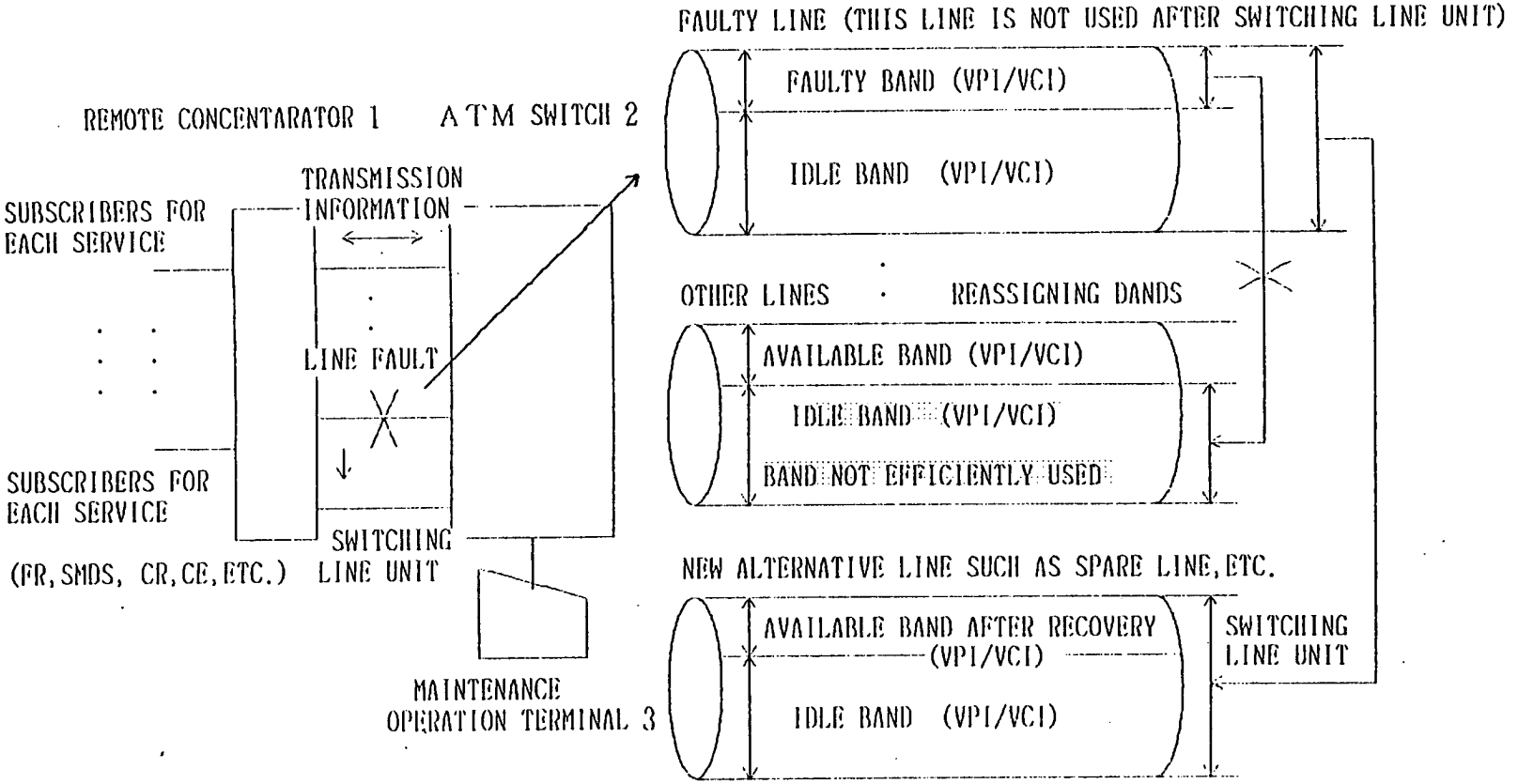

FAULTY LINE (THIS LINE IS NOT USED AFTER SWITCHING LINE UNIT)
FAULTY BAND (VPI/VCI)
IDLE BAND (VPI/VCI)
REMOTE CONCENTARATOR 1
ATM SWITCH 2
TRANSMISSION INFORMATION
SUBSCRIBERS FOR EACH SERVICE
LINE FAULT
SUBSCRIBERS FOR EACH SERVICE
(FR, SMDS, CR, CE, ETC.)
SWITCHING LINE UNIT
OTHER LINES
REASSIGNING BANDS
AVAILABLE BAND (VPI/VCI)
IDLE BAND (VPI/VCI)
BAND NOT EFFICIENTLY USED
NEW ALTERNATIVE LINE SUCH AS SPARE LINE, ETC.
AVAILABLE BAND AFTER RECOVERY (VPI/VCI)
IDLE BAND (VPI/VCI)
SWITCHING LINE UNIT
MAINTENANCE OPERATION TERMINAL 3

FIG. 913